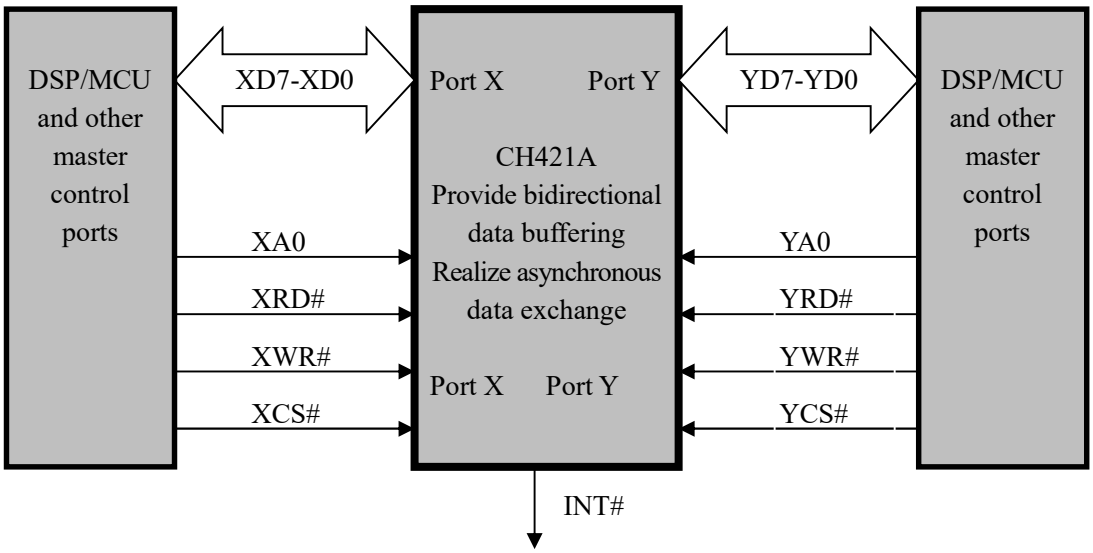
Bidirectional Buffer Interface Chip CH421

Datasheet
Version: 2A
http://wch.cn

1. Overview

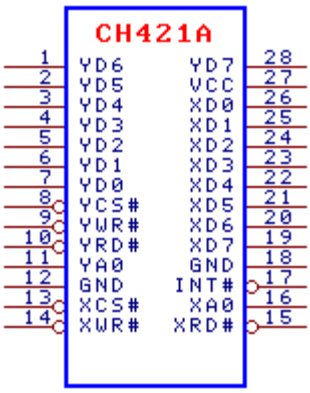
CH421A is an interface chip that provides bidirectional data buffering. CH421A has two 8-bit passive parallel ports X and Y, and realizes bidirectional asynchronous data exchange between ports X and Y by sharing a 66-byte dual-port data buffer. CH421A supports simultaneous operation of both ports. It is suitable for connecting MCU with MCU, MCU with DSP/MCU, and MCU with other master control ports with active parallel interfaces, such as the printer port of the computer or the local port of CH365. The figure below shows its general application block diagram.



2. Features

- The universal 8-bit bidirectional data bus can be directly connected to the system bus of DSP/MCU.
- Provide a 66-byte data buffer that can be shared to ports X and Y based on the dual-port SRAM.
- Respectively provide 1-byte unidirectional buffer to ports X and Y, that is, writable to one port and readable to two ports.
- Active low universal parallel interface control signals: chip selection control line, read strobe line, write strobe line.
- Only two address bits are used: index address port and data port. The internal index address automatically increases after the data port is read and written.
- Provide the interrupt output pin INT# with controllable software at both ends, active at low level.
- Asynchronous data exchange, supporting simultaneous read and write operation of ports X and Y, synchronization and waiting not required.
- The maximum data transmission speed is not less than 7M bytes per second.
- Support 5V or 3.3V supply voltage.
- Adopt SOP-28 chip lead-free package, and be compatible with RoHS.

3. Package



Package	Width of Plastic		Pitch of Pin		Instruction of Package	Ordering Information
SOP-28	7.62mm	300mil	1.27mm	50mil	Standard 28-pin patch	CH421A

Note: CH421A chip has different functions and different pins from the original CH421S.

4. Pins

Pin No.	Pin name	Type	Pin description
27	VCC	Power	Positive power
12,18	GND	Power	Common ground
19-26	XD7～XD0	Three-status output and input	Bidirectional data signal line on port X, weak pull-up resistor
16	XA0	Input	Address line input of port X, pointing to the index port if it is 0, pointing to the data port if it is 1
15	XRD#	Input	Read strobe/enable input of port X, active low
14	XWR#	Input	Write strobe/enable input of port X, active low
13	XCS#	Input	Chip selection control input of port X, active low
1-7,28	YD7～YD0	Three-state output and input	Bidirectional data signal line of port Y
11	YA0	Input	Address line input of port Y, pointing to the index port if it is 0, pointing to the data port if it is 1
10	YRD#	Input	Read strobe/enable input of port Y, active low
9	YWR#	Input	Write strobe/enable input of port Y, active low
8	YCS#	Input	Chip selection control input of port Y, active low
17	INT#	Output	Software controlled interrupt request output, active low

5. Principle description

The following figure shows the internal circuit diagram of CH421A chip (for function interpretation, for reference only).

CH421A has a built-in dual-port SRAM with two sets of bidirectional data lines, two sets of address lines and two sets of read-write control lines, which are connected to ports X and Y respectively. The capacity of the dual-port SRAM is 66 bytes, and the address range is 00H-41H.

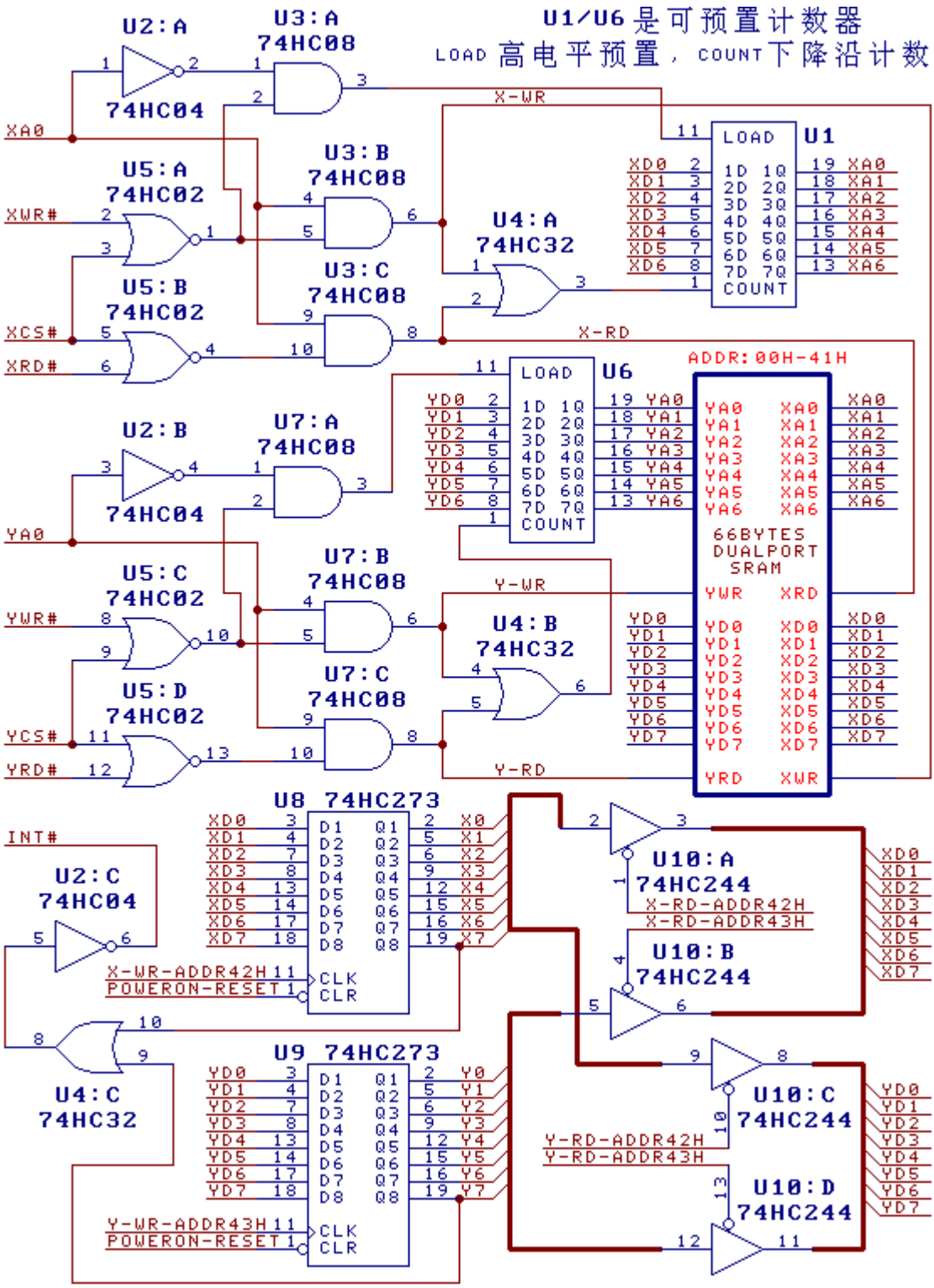
CH421A also has 1-byte unidirectional buffer respectively on both ports X and Y, namely, registers U8 and U9 in the figure, which are writable to one port and readable to two ports. The unidirectional buffer U8 is a unidirectional buffer on port X. It can only be written on port X, and its write address is 42H. The unidirectional buffer U9 is a unidirectional buffer on port Y. It can only be written on port Y, and its write address is 43H. The unidirectional buffer U8 on port X has a read address of 42H and the unidirectional buffer U9 on port Y has a read address of 43H. After power on reset, the data in the two unidirectional buffers will be automatically reset to 0.

INT# pin of CH421A is the software controlled interrupt request output, which is at high level by default. When the bit 7 of the unidirectional buffer U8 is set to 1 or the bit 7 of the unidirectional buffer U9 is set to 1, INT# pin outputs low level; otherwise, it outputs high level.

There is only one address line XA0 or YA0 outside CH421A, so index addressing is adopted for the built-in SRAM and the unidirectional buffer. The index address range is 00H-43H, which corresponds to 66 data units of SRAM and two unidirectional buffers respectively. Index addressing means that the 7-bit index address is written through the index port, and then the data is read and written to the SRAM unit or unidirectional buffer specified by the index address through the data port. When XA0 or YA0 is at low level, the write operation points to the index port, and it is meaningless to perform read operation to the index port. When XA0 or YA0 is at high level, read and write operation points to the data port.

The ports X and Y of CH421A support the automatic increment of index address, which can improve the efficiency of sequential data read and write. After each byte of data is read and written, the index address of the internal addressing will be automatically plus 1. If the data of the next addressing is to be read and written, it can be read and written directly through the data port, instead of inputting the index address of the next addressing through the index port. Refer to the figure above. U1 and U6 are 7-bit presettable counters. The index address written through the index port is preset to the counter. When a read/write operation is completed, the counter will be automatically plus 1, thus directly generating the index address of the next addressing.

The port Y speed of CH421A is relatively high, and the port X speed is relatively low, and the port Y has a higher priority than the port X.



The following is an example of data read and written from ports X and Y of CH421A:

① Write index address 26H when YA0 is 0, and write the data 94H when YA0 is 1. The result is that the data 94H is written to SRAM with address 26H.

② Write index address 25H when XA0 is 0, and write the data 6EH when XA0 is 1. The result is that the data 6EH is written to SRAM with the address of 25H;

③ If it is read again when XA0 is 1 (CH421A automatically adds the index address of the previous operation on the port X), the result will be that the SRAM address of 26H, namely, the data 94H written on the port Y at the earliest.

④ If it is read again when YA0 is 1 (CH421A automatically adds the index address of the previous

operation on the port Y), the result will be that the SRAM address of 27H is read.

With memory sharing of CH421A, 66 bytes of data blocks can be transmitted at one time, which is suitable for providing high-speed bidirectional data transmission between two master control ports with active parallel interfaces.

The following table is the truth table of the parallel port I/O operation (X in the table means that this bit is not concerned, and Z means that three states of CH421A are disabled).

CS#	WR#	RD#	A0	D7-D0	Actual operation on CH421A chip
1	X	X	X	X/Z	CH421A is not selected, and no any operation is made
0	1	1	X	X/Z	Although selected, no any operation is made
0	0	X	0	Input	Write the index address to CH421A, which is the starting address for subsequent reading and writing operations
0	0	X	1	Input	Write data to the specified address, and the index address will increase progressively after completion, facilitating continuous reading and writing
0	1	0	1	Output	Read data from the specified address. The index address will increase progressively after completion, facilitating the continuous reading and writing
0	1	0	0	Output	Undefined, results unknown, disabled

For MCU similar to the Intel parallel port timing sequence, RD# and WR# pins of CH421A chip can be connected to the read strobe output pin and write strobe output pin of MCU respectively. For MCU similar to Motorola parallel port time sequence, the RD# pin of CH421A shall be connected to the low level, and the WR# pin shall be connected to the reading and writing direction output pin R/-W of MCU.

6. Parameters

6.1. Absolute Maximum Value

Critical value or exceeding the absolute maximum value may cause the chip to work abnormally or even be damaged.

Name	Parameter description		Min.	Max.	Unit
TA	Ambient temperature during operation	VCC=5V	-40	85	℃
		VCC=3.3V	-40	65	
TS	Ambient temperature during storage		-55	125	℃
VCC	Supply voltage (VCC connects to power, GND to ground)		-0.5	6.0	V
VIO	Voltage on the input or output pins		-0.5	VCC+0.5	V

6.2. Electrical Parameters

Test Conditions: TA=25℃, VCC=5V

(If the supply voltage is 3.3V, all current parameters in the table need to be multiplied by a factor of 40%)

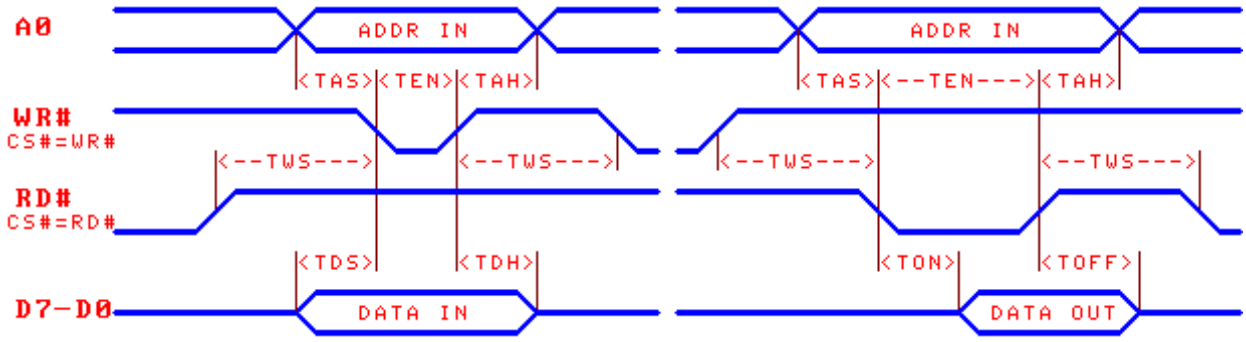
Name	Parameter description	Min.	Typ.	Max.	Unit
VCC	Power voltage	3.3	5	5.3	V
ICC	Supply current during working at 5V	0.2	1.5	10	mA
ICC3	Supply current during working at 3.3V	0.1	0.5	5	mA
VIL	Low level input voltage	-0.5		0.8	V

VIH	High level input voltage	2.0		VCC+0.5	V
VOL	Low level output voltage (4mA draw current)			0.5	V
VOH	High level output voltage (2mA output current)	VCC-0.5			V
IIN	Input current of input terminal with no pull-down resistor			10	uA
IUP1	Input current at the input terminal with the weak pull-up resistor	2	5	170	uA
VR	Voltage threshold of internal power on reset	2.4	2.7	3.0	V

6.3. Port X Timing parameters

Test Conditions: TA=25℃, VCC=5V, Parameter in Brackets VCC=3.3V, Refer to the attached figure below.
(RD means that RD# signal is valid and XCS# signal is valid; XWR#=1&XRD#=XCS#=0 performs read operation)
(WR means that WR# signal is valid and XCS# signal is valid; XWR#=XCS#=0 performs write operation)

Name	Parameter description	Min	Typ	Max	Unit
TEN	Width of effective RD or WR strobe pulse	70 (120)			nS
TWS	Interval width of RD or WR strobe pulse	70 (120)			nS
TAS	Address input setup time before RD or WR	5 (8)			nS
TAH	Address input maintaining time after RD or WR	5			nS
TDS	Data input setup time before write strobe WR	0			nS
TDH	Data input maintaining time after strobe writing WR	3			nS
TON	Effective strobe reading RD to effective data output		40	70 (100)	nS
TOFF	Ineffective strobe reading RD to ineffective data output			20 (35)	nS



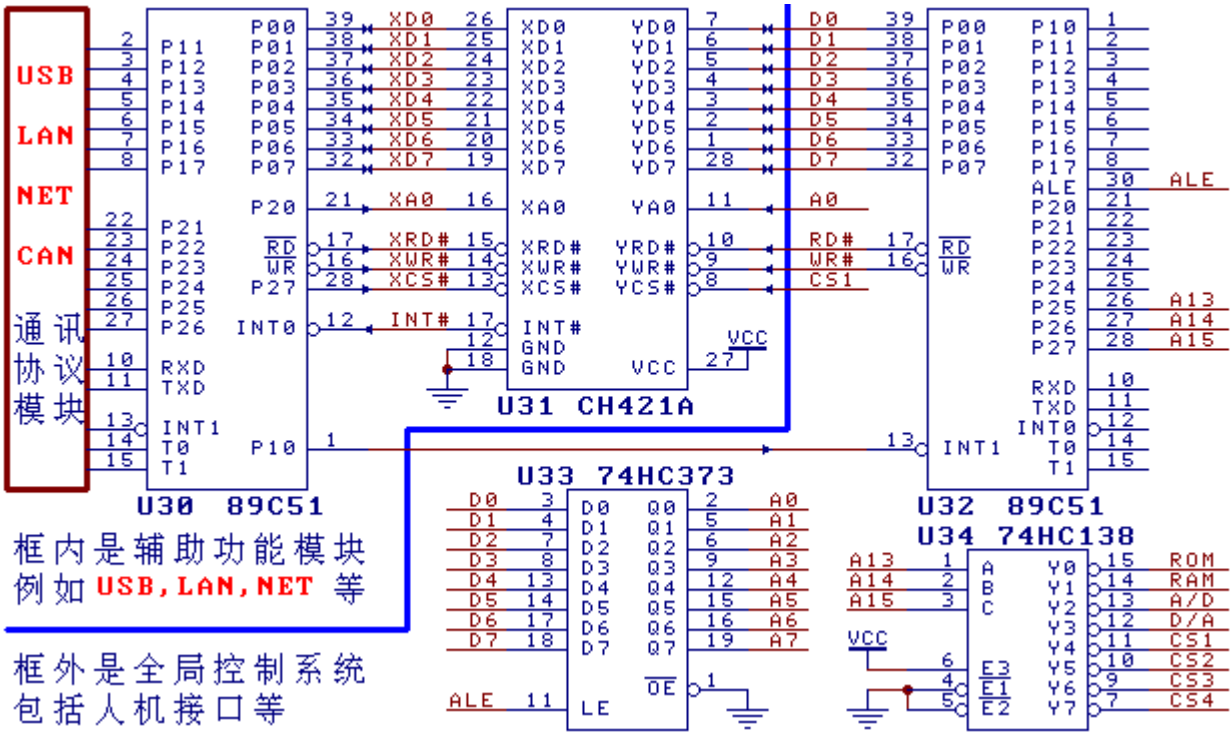
6.4. Port Y Timing Parameters

Test Conditions: TA=25℃, VCC=5V, the Parameter in Brackets VCC=3.3V, refer to the attached figure above.
(RD means that RD# signal is valid and YCS# signal is valid; perform read operation when YWR#=1&YRD#=YCS#=0)
(WR means that WR# signal is valid and YCS# signal is valid; perform write operation when YWR#=YCS#=0)

Name	Parameter description	Min.	Typ.	Max.	Unit
TEN	Width of effective RD or WR strobe pulse	40 (70)			nS
TWS	Interval width of RD or WR strobe pulse	70 (120)			nS
TAS	Address input setup time before RD or WR	5 (8)			nS
TAH	Address input hold time after RD or WR	5			nS
TDS	Data input setup time before write strobe WR	0			nS
TDH	Data input hold time after strobe writing WR	3			nS
TON	Read active to data output valid		30	40 (60)	nS
TOFF	Read inactive to data output invalid			20 (35)	nS

7. Applications

7.1. Connection of Two MCUs (Figure below)



U30 is an auxiliary DSP/MCU, which is specially used for handling complex network communication protocols or calculations. U32 is the master control MCU for global transactions, including providing human-computer interaction interface, etc. Its system bus is connected with a number of peripheral devices, addresses A7-A0 are provided by the latch U33, and U34 is used for global address decoding to generate the chip selection signals of each peripheral device. U30 is connected to the system bus of U32 through U31 (CH421A) and becomes a functional module of many peripherals for U32. As U30 is specialized in handling communication protocols, U32 is notified in interrupt mode only after data receipt and transmission are completed and verification is passed. Therefore, U32 only needs to consider transmitting and receiving data at the application layer, and does not need to consider various complex communication protocols.

In the actual circuit design, the circuit composed of U30 and U31 in the frame shown in the figure can independently become a circuit module with specific functions, and can be provided by a third-party manufacturer as a standardized function module and then connected to the system board where the main control MCU is located through a 16-pin or 20-pin socket.

The address line XA0 on the port X of CH421A in the figure is driven by the address line P20 of U30 to select the index port or data port.

When the parallel connection distance is far, crosstalk between signals shall be considered. It is suggested to add shielded ground wire between control signal lines such as CS# and RD#, or add RC integrating circuit to the control signal line. For example, respectively connect 30pF capacitor to the ground in parallel near RD# pin and CS# pin, and then connect 1KΩ resistor in series as a control signal input terminal. If the integrating circuit is added, a drop in parallel transmission speed will be caused, so the integrating circuit is not required for the application of single piece of PCB as long as PCB wiring is reasonable.

7.2. Connection of CH365 with MCU (Figure below)

CH365 is a universal interface chip for PCI bus. As the local port provided by CH365 is an active parallel interface, it is not convenient to directly connect it with MCU (8255 parallel port mode of CH352L chip can be used). In the figure, U21 (CH421A) is used to provide bidirectional data buffer between U20 (CH365) and U22 of MCU to realize asynchronous data exchange between them.

When the computer needs to be linked with MCU, first write data to CH421A, and then output the low level through the address line A15 of CH365, so that MCU enters the interrupt service program to get data from CH421A and process it.

In general PCI products, the computer is the initiator and master controller of all operations, and MCU just passively enters the interrupt service program and then processes the tasks assigned by the computer. As CH365 supports hardware interrupt, MCU can also be used as the initiator and master controller when required. When MCU needs to be linked to the computer, the input pin SYS_EX (INT_REQ) of CH365 is set to low level, then the computer enters the interrupt service program, and gets the data submitted by MCU from CH421A under the control of the program and processes it.

In order to enable the interrupt function of CH365, R20 is used as the pull-down resistor of CH365 data line D3 in the figure. When the interrupt function of CH365 is not used, the connection line between the resistor R20 as well as SYS_EX of CH365 and P10 of MCU can be removed.