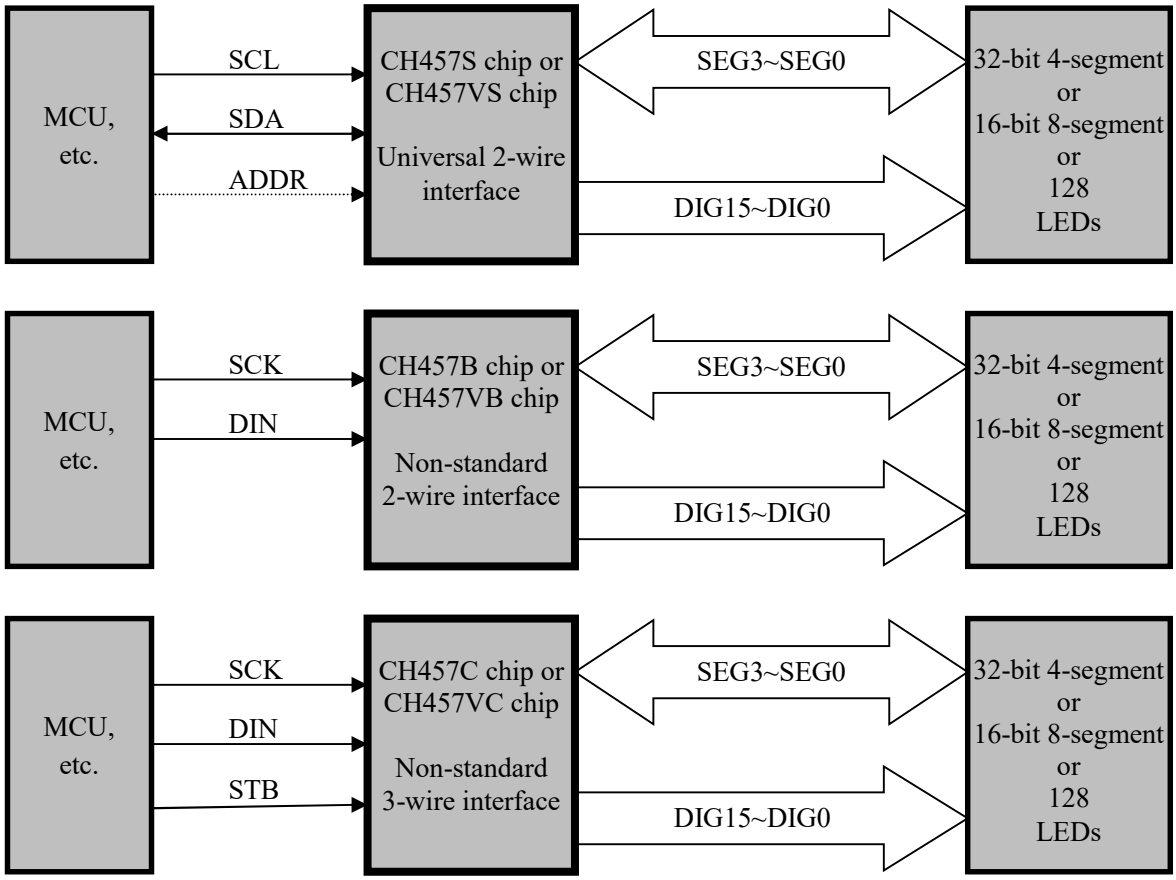
128 LED display driver chip CH457

Datasheet
Version: 2
http://wch.cn

1. Overview

CH457 is 128-LED display driver chip. CH457 has a built-in clock oscillation circuit, which can dynamically drive 128 LEDs with 32-bit 4-segment or 16-bit 8-segment structure. CH457 exchanges data with MCU via 2-wire or 3-wire serial interface.



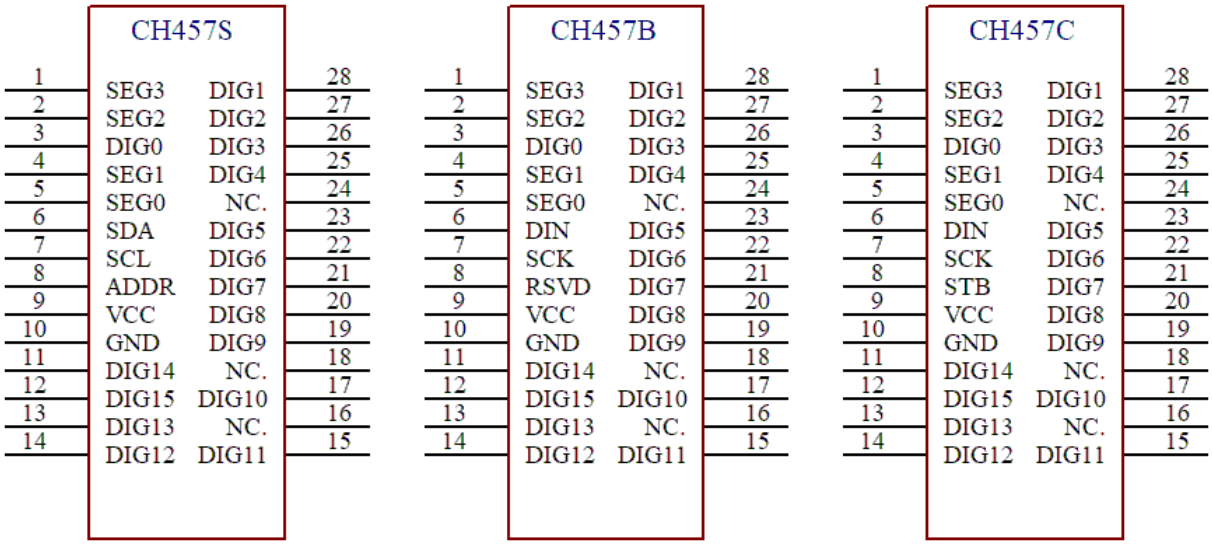
2. Features

- Built-in display current driving stage, segment current not less than 30mA, word current not less than 120mA.
- Dynamic display scanning control, direct drive of 128 LEDs with 32-bit 4-segment or 16-bit 8-segment structure.
- Internal current limiting, provide 8-level brightness control through duty ratio setting.
- High speed 2-wire or 3-wire serial interface, clock speed from 0 to 2MHz, the universal 2-wire compatible with two-line I^2C bus to save pins.
- Built-in clock oscillator circuit, no need to provide external clock or external oscillator components, more anti-interference.
- Automatic low power consumption sleep to save electricity.
- 8KV enhanced ESD performance.
- Support low cost single panel PCB wiring and full patch process.
- CH457S/B/C is used for 5V voltage, and can support 3.3V. CH457VS/VB/VC is used for 3.3V

voltage, and can support 2.8V.

- Package form: SOP28, lead-free package, and be compatible with RoHS.

3. Package



Package	Width		Pitch of Pin		Instruction of Package	Ordering information
SOP28	7.62mm	300mil	1.27mm	50mil	Standard 28-pin patch @5V	CH457S
SOP28	7.62mm	300mil	1.27mm	50mil	Standard 28-pin patch @3.3V	CH457VS
SOP28	7.62mm	300mil	1.27mm	50mil	Standard 28-pin patch @5V	CH457B
SOP28	7.62mm	300mil	1.27mm	50mil	Standard 28-pin patch @3.3V	CH457VB
SOP28	7.62mm	300mil	1.27mm	50mil	Standard 28-pin patch @5V	CH457C
SOP28	7.62mm	300mil	1.27mm	50mil	Standard 28-pin patch @3.3V	CH457VC

Notes: The pins and functions of CH457VS (VB, VC) and CH457S (B, C) correspond one to one, only the working voltage is different.

For customized versions of chips (pin customization, address customization, current customization, brightness locking, etc.), this manual is not completely applicable.

4. Pins

Pin No.	CH457S/VS Pin name	CH457B/VB Pin name	CH457C/VC Pin name	Type	Pin description
9	VCC			Power	Positive power supply, continuous current not less than 150mA
10	GND			Power	Common ground, continuous current not less than 150mA
5, 4, 2, 1	SEG0~SEG3			Output	Segment drive output

3, 28~25, 23~19, 17, 15~13, 11, 12	DIG0~DIG15			Output	Word drive output
7	SCL	SCK	SCK	Input	Clock input of serial interface
6	SDA			Open-drain output and input	Data input and response output of serial interface, Built-in pull-up resistor
		DIN	DIN	Input	Data input of serial interface
8	ADDR			Input	Address selection input for serial interface, corresponding to the bit 6 (address bit 5) of the first byte, which is used for 2 lines parallel connection with double CH457S/VS separately controlled, with built-in weak pull-up resistor
		RSVD		Reserved	Reserved pin. Do not connect it
			STB	Input	Chip selection input of serial interface, active at low level, Built-in weak pull-up resistor
16, 18, 24	NC.			Idle pin	Idle pin

5. Functional Specification

(Partly compatible with existing chips)

6. Operation Commands

(Partly compatible with existing chips)

6.1. CH457S/VS Setting System Parameter Commands

When the command is transmitted, the high bit is in front, byte 1 is 01001000B, i.e. 48H. Byte 2 is 0[INTENS]000[DISP]B.

This command is used to set system-level parameters of CH457S/VS: display driver enable DISP, and display driver brightness control INTENS.

Bit 0 is DISP, allow display output when is 1, turn off display driver and automatically sleep in low power consumption when is 0.

Bit 6 ~ Bit 4 is INTENS, which is used to control the brightness of the display driver, which contains 3-bit data and has 8 combinations: data 000B, 001B, 010B, 011B, 100B, 101B and 110B respectively set the duty cycle of the display driver to 8/8, 1/8, 2/8, 3/8, 4/8, 5/8 and 6/8, and enable the internal segment drive current limiter. Data 111B sets the duty cycle of the display drive to 8/8, but the internal segment drive current limiter is disabled, so the external segment pin is required to be connected with the current limiting resistor R0 in series.

This command does not affect the data in the internal data buffer.

6.2. CH457S/VS Word-data loading command

The command is transmitted with the higher bit in front. The byte 1 is 011[DIG_ADDR]0B, i.e. 60H, 62H, 64H, 66H, 68H, 6AH, 6CH, 6EH, 70H, 72H, 74H, 76H, 78H, 7AH, 7CH and 7EH. Byte 2 is [DIG_DATA]B, i.e. the value between 00H and 0FFH.

"Word-data loading command" is used to write the word data DIG_DATA to the data register at the specified address DIG_ADDR. DIG_ADDR specifies the address of the data register through 4-bit data. Data 0000B~1111B specify the addresses 0~15 respectively, corresponding to 16 LED Nixie tubes driven by the pins DIG0~DIG15. DIG_DATA is 8-bit word data. For example, command data 01100000B and 01111001B means that word data 79H is written into the first data register so that the LED Nixie tube driven by the pin DIG0 will display E.

The command can also have subsequent bytes that are loaded separately into the data register of the subsequent address.

6.3. CH457B/VB and CH457C/VC System Control Command

The data byte of the command is 1000[DISP][INTENS]. Since the low bit is in front during the interface transmission of CH457B/VB and CH457C/VC, the actual time sequence is as follows: INTENS[0], INTENS[1], INTENS[2], DISP, 0, 0, 0 and 1.

This command is used to control CH457B/VB and CH457C/VC: display driver enable DISP, and display driver brightness control INTENS.

Bit 3 is DISP, allow display output when is 1, turn off display driver and automatically sleep in low power consumption when is 0.

Bit 2 ~ Bit 0 are INTENS, which is used to control the brightness of the display driver, which contains 3-bit data and has 8 combinations: data 111B, 000B, 001B, 010B, 011B, 100B, 101B and 110B respectively set the duty cycle of the display driver to 8/8, 1/8, 2/8, 3/8, 4/8, 5/8, 6/8 and 7/8, and enable the internal segment drive current limiter.

Notes: Some customized versions lock the duty cycle of the display driver as 8/8 and will ignore the data for adjusting brightness.

This command does not affect the data in the internal data buffer.

7. Parameters

7.1. Absolute Maximum Value

Critical value or exceeding the absolute maximum value may cause the chip to work abnormally or even be damaged.

Name	Parameter description	Min.	Max.	Unit
TA	Ambient temperature during operation	-40	85	℃
TS	Ambient temperature during storage	-55	125	℃
VCC5	CH457S/B/C supply voltage (VCC is connected to the power, GND is grounded)	-0.5	7.0	V
VCC3	CH457VS/VB/VC supply voltage (VCC is connected to the power, GND is grounded)	-0.5	4.5	V
VIO	Voltage on the input or output pins	-0.5	VCC+0.5	V
IMdig	Continuous drive current of single DIG pin	0	200	mA

IMseg	Continuous drive current of single SEG pin	0	50	mA
IMall	Total continuous drive current of all SEG pins	0	200	mA

7.2. CH457S/B/C Electrical Parameters

Test Conditions: TA=25℃, VCC5=5V

Name	Parameter description	Min.	Typ.	Max.	Unit
VCC5	Power supply voltage	3.3	5.0	5.5	V
ICC	Current of power supply		100	160	mA
ICCs	Quiescent current (all interface input pins are at high level)			0.1	mA
VIL	Interface input pin low level input voltage	0		0.8	V
VIH	Interface input pin high level input voltage	2.0		VCC5	V
VOLdig	Low level output voltage of DIG pin (-120mA)			0.7	V
VOHdig	High level output voltage of DIG pin (120mA)	VCC5-0.7			V
VOLseg	Low level output voltage of SEG pins (-30mA)			0.5	V
VOHseg	High level output voltage of SEG pin (30mA)	VCC5-0.5			V
IUP1	Input leakage current of SCL or SCK or DIN pin	-5	0	5	uA
IUP2	Input (or output) pull-up current of SDA pin		280	400	uA
IUP3	Input pull-up current of ADDR or STB pin		2	160	uA
VR	Default voltage threshold of power on reset	2.3	2.6	2.8	V

7.3. CH457VS/VB/VC Electrical Parameters

Test Conditions: TA=25℃, VCC3=3.3V

Name	Parameter description	Min.	Typ.	Max.	Unit
VCC3	Power supply voltage	2.5	3.3	3.6	V
ICC	Current of power supply		100	160	mA
ICCs	Quiescent current (all interface input pins are at high level)			0.1	mA
VIL	Interface input pin low level input voltage	0		0.8	V
VIH	Interface input pin high level input voltage	2.0		VCC3	V
VOLdig	Low level output voltage of DIG pin (-120mA)			0.7	V
VOHdig	High level output voltage of DIG pin (120mA)	VCC3-0.7			V
VOLseg	Low level output voltage of SEG pins (-30mA)			0.5	V
VOHseg	High level output voltage of SEG pin (30mA)	VCC3-0.5			V
IUP1	Input leakage current of SCL or SCK or DIN pin	-5	0	5	uA
IUP2	Input (or output) pull-up current of SDA pin		280	400	uA
IUP3	Input pull-up current of ADDR or STB pin		2	160	uA
VR	Default voltage threshold of power on reset	2.1	2.3	2.5	V

7.4. Internal Timing Parameters

Test Conditions: TA=25℃, VCC5=5V or VCC3=3.3V

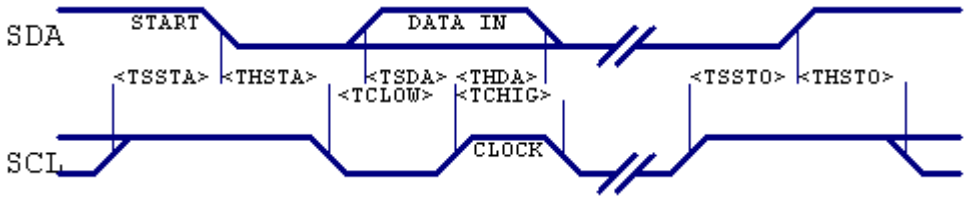
(Note: The timing parameters in this table are multiples of the built-in clock periods, and the frequency of the built-in clock decreases with the decrease of the supply voltage)

Name	Parameter description	Min.	Typ.	Max.	Unit
TPR	Reset time generated during power on detection	5	8	30	mS
TDP	Display scan period		8		mS

7.5. Interface Timing Parameters

Test Conditions: TA=25℃, VCC5=5V or VCC3=3.3V, refer to the attached figure above

(Note: The unit of measurement in this table is nanosecond, namely, 10^{-9} seconds. If the maximum value is not indicated, the theoretical value can be infinite.)



Name	Parameter description	Min.	Typ.	Max.	Unit
TSSTA	Setup time of SDA/DIN falling edge start signal	100			nS
THSTA	Hold time of SDA/DIN falling edge start signal	100			nS
TSSTO	Setup time of SDA/DIN rising edge stop signal	100			nS
THSTO	Hold time of SDA/DIN rising edge stop signal	100			nS
TCLOW	Low level width of SCL/SCK clock signal	100			nS
TCHIG	High level width of SCL/SCK clock signal	100			nS
TSDA	SDA/DIN input data to SCL/SCK rising edge Setup time	30			nS
THDA	SDA/DIN input data to SCL/SCK rising edge Holding time	10			nS
Rate	Average data transmission rate	0		2M	bps

8. Application

8.1. Application Circuit

(Refer to the evaluation board, partly compatible with existing chips, and provide single panel PCB of various styles, such as single-row/double-row/three-row display, etc.)