8-bit Enhanced USB MCU CH547/CH546

Datasheet

Version: 1F

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1. Overview

CH547 chip is an enhanced E8051 core microcontroller compatible with the MCS51 instruction set. 79% of its instructions are single-byte, single-cycle instructions, with an average instruction speed of 8 to 15 times faster than the standard MCS51.

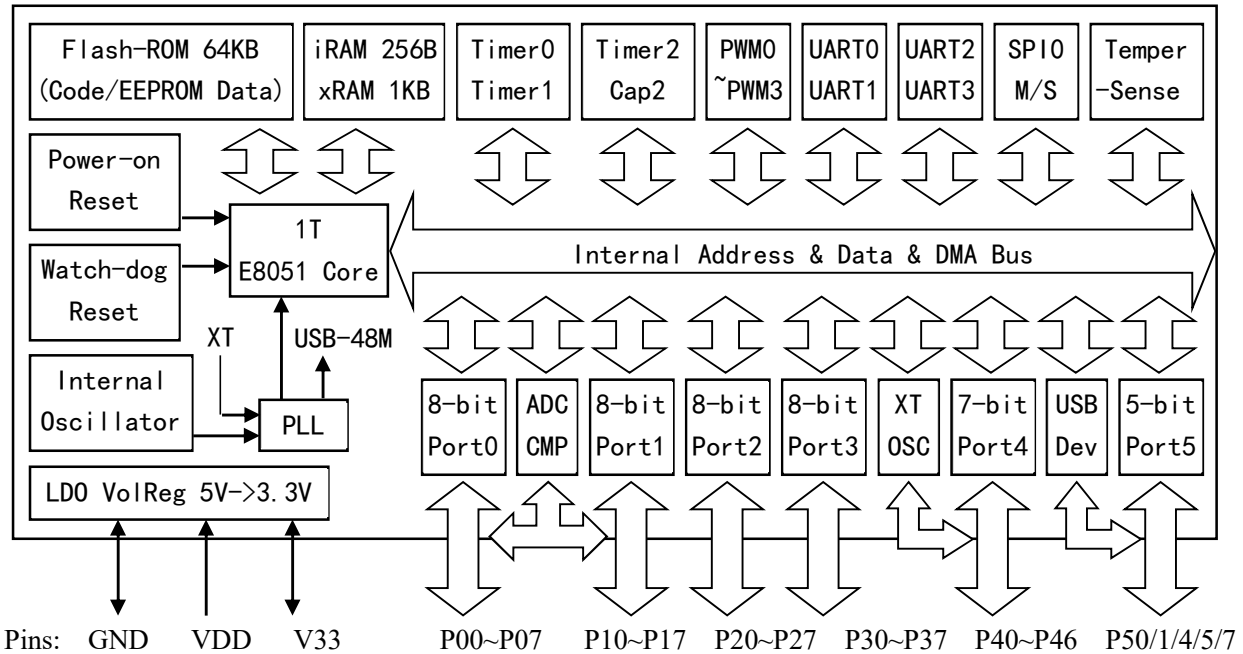
CH547 has a built-in 64K program memory Flash-ROM and 256 bytes of internal iRAM and 2K bytes of on-chip xRAM. xRAM supports DMA direct memory access.

CH547 has a built-in 12-bit ADC, capacitive touch key detection module, temperature sensor (TS), built-in clock, 3 sets of timers and 1 signal capture, 4-channel PWM, 4 UARTs, SPI and other function modules, and supports both full-speed and low-speed USB-Device modes.

CH546 is a simplified version of CH547, program memory ROM is only 32KB, asynchronous serial port only provides UART0, ADC and touch key detection only provides 8 channels, PWM only provides 2 channels, other than that, it is the same as CH547, you can directly refer to CH547 manual and information.

Model	Flash-ROM Boot ROM	xRAM iRAM	Nonvolatile EEPROM	USB device	TS	Timer	Signal capture	8-bit PWM	UART	SPI Master/ slave	12-bit ADC	Capacitive Touch key
CH547	60KB+3KB	1024 +256	1KB	Full- /low- speed	√	3	1- channel	4-channel	4	1	12-channel	12-channel
CH546	32KB+3KB							2-channel	1		8-channel	8-channel

The internal block diagram of the CH547 is shown below for reference only.

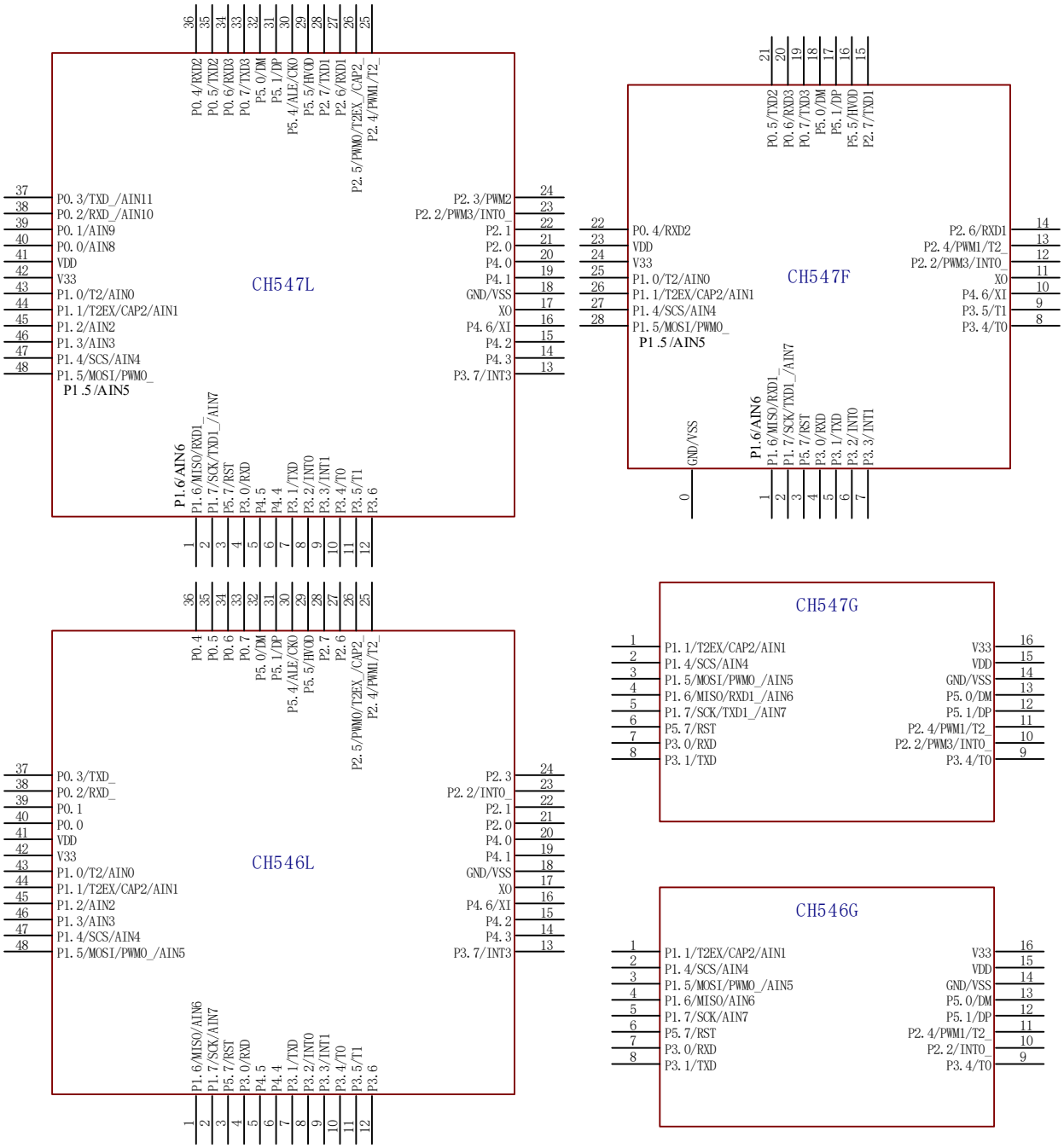


2. Features

- Core: Enhanced E8051 core, compatible with MCS51 instruction set, 79% of its instructions are single byte single cycle instructions, average instruction speed is 8 to 15 times faster than standard MCS51, unique XRAM data fast copy instruction, double DPTR pointer.
- ROM: 64KB non-volatile memory Flash-ROM, supports 10K erasures, can be used entirely for program storage space; or can be divided into 60KB program storage area and 1KB data storage area EEPROM and 3KB boot code BootLoader/ISP program area.
- EEPROM: 1K bytes of data storage area EEPROM, divided into 16 separate blocks, supports single byte read, single byte write, block write (1 to 64 bytes), block erase (64 bytes) operations, generally supports 100K erases in typical environments (non-guaranteed).
- OTP: one-time programmable data storage area OTP of 32 bytes in total, supports double word reads (4 bytes), single byte writes.
- RAM: 256 bytes internal iRAM for fast data staging as well as stacking; 1KB on-chip xRAM for large data staging as well as DMA direct memory access.
- USB: Embedded USB device controller and USB transceiver, supports USB 2.0 full speed 12Mbps or low speed 1.5Mbps. Supports up to 64-byte packets, internal FIFO, DMA support.
- Timer: 3 sets of timers, T0/T1/T2 are standard MCS51 timers.
- Capture: Timer T2 supports 1 way signal capture.
- PWM: 4 PWM outputs, supporting standard 8-bit data or fast 6-bit data.
- UART: 4 sets of asynchronous serial ports, UART0 is standard MCS51 serial port; UART1/2/3 comes with communication baud rate setting register.
- SPI: SPI controller supports Master/Slave master/slave mode, built-in FIFO, clock frequency can be up to half of the system master frequency Fsys, supports serial data input and output simplex multiplexing.
- ADC: 12-channel 12-bit A/D analog-to-digital converter, supports various combinations of voltage comparisons.
- Touch-Key: 12-channel capacitive touch-key detection support, with each ADC channel supporting touch-key detection.
- TS: Simple built-in temperature sensor.
- GPIO: supports up to 44 GPIO pins (including XI and RST and USB pins), supports MCS51-compatible quasi-bidirectional mode, new high resistance input, push-pull output, and open-drain output modes, with one pin supporting 12V high-voltage open-drain output.
- Interrupt: supports 16 groups of interrupt signal sources, including 6 groups of interrupts compatible with standard MCS51 (INT0, T0, INT1, T1, UART0, T2), and 10 groups of extended interrupts (SPI0, INT3, USB, ADC/UART2, UART1, PWMX/UART3 GPIO, WDOG), where GPIO interrupts can be selected from 7 pins.
- Watch-Dog: 8-bit programmable watchdog timer WDOG, supports timed interrupts.
- Reset: Supports 5 reset signal sources, built-in power-on reset and multi-level adjustable power low voltage detection reset module, supports software reset and watchdog overflow reset, optional pin external input reset.
- Clock: Built-in 24MHz clock source, external crystal support via multiplexed GPIO pins, built-in PLL for USB clock generation and system master Fsys at the required frequency.
- Power: Built-in 5V to 3.3V low dropout voltage regulator for modules such as USB, supporting 5V or 3.3V or even 6V or 2.8V supply voltages.
- Sleep: supports low power sleep, USB, UART0, UART1, SPI0, comparator and some GPIO external wake-ups.
- The chip has a built-in unique ID number and supports ID numbers and checksums.

3. Package

Package Form	Shaping Width		Pin Spacing		Package Description	Order Model
LQFP-48	7*7mm		0.5mm	19.7mil	Low-profile Quad Flat Package	CH547L
QFN28_4X4	4*4mm		0.4mm	15.7mil	Quad Flat No-Lead Package	CH547F
SOP-16	3.9mm	150mil	1.27mm	50mil	Small Outline Package	CH547G
LQFP-48	7*7mm		0.5mm	19.7mil	Low-profile Quad Flat Package	CH546L
SOP-16	3.9mm	150mil	1.27mm	50mil	Small Outline Package	CH546G



4. Pin Definitions

Pin No.			Pin name	Other function names (Left function with the highest priority)	Description
SOP16	QFN28	LQFP48			
15	23	41	VDD	VCC	I/O power input and external power input of internal USB power regulator, requires an external 0.1uF decoupling capacitor.
16	24	42	V33	V3	Internal voltage regulator output and internal USB power input, When supply voltage is less than 3.6V, connect VDD to input the external power supply. When supply voltage is greater than 3.6V, an external 0.1uF decoupling capacitor is required.
14	0	18	GND	VSS	Common ground terminal.
-	-	40	P0.0	AIN8	AIN8 ~ AIN11: 4-channel ADC analog signal/touch-key input. RXD_, TXD_: RXD, TXD pin mapping. RXD2, TXD2: UART2 serial data input, serial data output. RXD3, TXD3: UART3 serial data input, serial data output.
-	-	39	P0.1	AIN9	
-	-	38	P0.2	RXD_/AIN10	
-	-	37	P0.3	TXD_/AIN11	
-	22	36	P0.4	RXD2	
-	21	35	P0.5	TXD2	
-	20	34	P0.6	RXD3	
-	19	33	P0.7	TXD3	
-	25	43	P1.0	T2/AIN0	AIN0 ~ AIN7: 8-channel ADC analog signal/touch-key input. T2: Timer/counter2 external count input/clock output. T2EX: Timer/counter2 reload/capture input. CAP2: Timer/counter2 capture input. SCS, MOSI, MISO, SCK: SPI0 interfaces. SCS is chip select input, MOSI is master output/slave input, MISO is master input/slave output, SCK is serial clock. PWM0_, RXD1_, TXD1_: PWM0/RXD1/TXD1 pin mapping.
1	26	44	P1.1	T2EX/CAP2/AIN1	
-	-	45	P1.2	AIN2	
-	-	46	P1.3	AIN3	
2	27	47	P1.4	SCS/AIN4	
3	28	48	P1.5	MOSI/PWM0_/AIN5	
4	1	1	P1.6	MISO/RXD1_/AIN6	
5	2	2	P1.7	SCK/TXD1_/AIN7	
-	-	21	P2.0		PWM0~PWM3: 4-channel PWM outputs. INT0_: INT0 pin mapping. T2_: T2 pin mapping. T2EX_/CAP2_: T2EX/CAP2 pin mapping. RXD1, TXD1: UART1 serial data input, serial data output.
-	-	22	P2.1		
10	12	23	P2.2	PWM3/INT0_	
-	-	24	P2.3	PWM2	
11	13	25	P2.4	PWM1/T2_	
-	-	26	P2.5	PWM0/T2EX_/CAP2_	
-	14	27	P2.6	RXD1	
-	15	28	P2.7	TXD1	
7	4	4	P3.0	RXD	RXD, TXD: UART0 serial data input, serial data

8	5	7	P3.1	TXD	output. INT0, INT1: External interrupt0, external interrupt1 input. T0, T1: Timer0, timer1 external input. INT3: External interrupt3.
-	6	8	P3.2	INT0	
-	7	9	P3.3	INT1	
9	8	10	P3.4	T0	
-	9	11	P3.5	T1	
-	-	12	P3.6		
-	-	13	P3.7	INT3	
-	-	20	P4.0		XI, XO: External crystal oscillator input, inverted output.
-	-	19	P4.1		
-	-	15	P4.2		
-	-	14	P4.3		
-	-	6	P4.4		
-	-	5	P4.5		
-	10	16	P4.6	XI	
-	11	17	XO		
13	18	32	P5.0	DM/UDM	DM, DP: D- and D+ signals of USB device. The resistors are all built-in, and it is recommended that no external resistors be connected in series.
12	17	31	P5.1	DP/UDP	
-	-	30	P5.4	ALE/CKO	ALE/CKO: Address latch signal output or clock output. HVOD: Support 12V high voltage open-drain output.
-	16	29	P5.5	HVOD	
6	3	3	P5.7	RST	External reset input, built-in pull-down resistor.

5. Special Function Register (SFR)

Abbreviations and descriptions in this datasheet:

Abbreviation	Description
RO	Indicates access type: read-only
WO	Indicates access type: write only, read values are invalid
RW	Indicates access type: read and write
H	End with it to indicate a hexadecimal number
B	End with it to indicate a binary number

5.1 SFR Introduction and Address Distribution

The CH547 uses the special function registers SFR and xSFR to control and manage the device and to set the operating mode.

The SFR occupies the address range 80h-FFh of the internal data storage and can only be accessed by direct address mode instructions. Registers with addresses x0h or x8h are addressable by bit, which prevents access to a specific bit from modifying the value of other bits; other registers with addresses other than multiples of 8 can only be accessed by byte.

Some SFRs can only write data in safe mode and are read-only in non-safe mode, e.g. GLOBAL_CFG, CLOCK_CFG, WAKE_CTRL, POWER_CFG.

Some SFRs have one or more aliases, e.g. SPI0_CK_SE/SPI0_S_PRE, ROM_ADDR_L/ROM_DATA_LL,

ROM_ADDR_H/ROM_DATA_LH, ROM_DATA_HL/ROM_DAT_BUF, ROM_DATA_HH/ROM_BUF _MOD. Some addresses correspond to multiple independent SFRs, e.g. SAFE_MOD/CHIP_ID, ROM_CTRL/ROM_STATUS.

The CH547 contains all the registers of the standard 8051 SFR, with the addition of other device control registers. The specific SFRs are shown in the table below.

Table 5.1 Table of special function registers

SFR	0、8	1、9	2、A	3、B	4、C	5、D	6、E	7、F
0xF8	SPI0_STAT	SPI0_DATA	SPI0_CTRL	SPI0_CK_SE SPI0_S_PRE	SPI0_SETUP		RESET_KEEP	WDOG_COUNT
0xF0	B	TKEY_CTRL	ADC_CTRL	ADC_CFG	ADC_DAT_L	ADC_DAT_H	ADC_CHAN	ADC_PIN
0xE8	IE_EX	IP_EX	UEP4_1_MOD	UEP2_3_MOD	UEP0_DMA_L	UEP0_DMA_H	UEP1_DMA_L	UEP1_DMA_H
0xE0	ACC	USB_INT_EN	USB_CTRL	USB_DEV_AD	UEP2_DMA_L	UEP2_DMA_H	UEP3_DMA_L	UEP3_DMA_H
0xD8	USB_INT_FG	USB_INT_ST	USB_MIS_ST	USB_RX_LEN	UEP0_CTRL	UEP0_T_LEN	UEP4_CTRL	UEP4_T_LEN
0xD0	PSW	UDEV_CTRL	UEP1_CTRL	UEP1_T_LEN	UEP2_CTRL	UEP2_T_LEN	UEP3_CTRL	UEP3_T_LEN
0xC8	T2CON	T2MOD	RCAP2L	RCAP2H	TL2	TH2		
0xC0	P4		P4_MOD_OC	P4_DIR_PU	P0_MOD_OC	P0_DIR_PU		
0xB8	IP	CLOCK_CFG	POWER_CFG		SCON1	SBUF1	SBAUD1	SIF1
0xB0	P3	GLOBAL_CFG	GPIO_IE	INTX	SCON2	SBUF2	SBAUD2	SIF2
0xA8	IE	WAKE_CTRL	PIN_FUNC	P5	SCON3	SBUF3	SBAUD3	SIF3
0xA0	P2	SAFE_MOD CHIP_ID	XBUS_AUX	PWM_DATA3				
0x98	SCON	SBUF	PWM_DATA2	PWM_DATA1	PWM_DATA0	PWM_CTRL	PWM_CK_SE	PWM_CTRL2
0x90	P1	USB_C_CTRL	P1_MOD_OC	P1_DIR_PU	P2_MOD_OC	P2_DIR_PU	P3_MOD_OC	P3_DIR_PU
0x88	TCON	TMOD	TL0	TL1	TH0	TH1	ROM_DATA_HL ROM_DAT_BUF	ROM_DATA_HH ROM_BUF_MOD
0x80	P0	SP	DPL	DPH	ROM_ADDR_L ROM_DATA_LL	ROM_ADDR_H ROM_DATA_LH	ROM_CTRL ROM_STATUS	PCON

Notes: (1) Those in red text can be accessed by bits;

(2) The following table shows the corresponding description of different color boxes.

	Register address
	SPI0 register
	ADC register
	USB register
	Timer/counter2 register
	Port setting register
	PWMX register
	UART1/2/3 register
	Timer/counter 0 and 1 register
	Flash-ROM register

5.2 SFR Classification and Reset Value

Table 5.2 Description and reset value of SFR and xSFR

Function	Name	Address	Description	Reset value
System setting registers	B	F0h	B register	0000 0000b
	ACC	E0h	Accumulator	0000 0000b
	PSW	D0h	Program status register	0000 0000b
	GLOBAL_CFG	B1h	Global configuration register (CH547 Bootloader)	0110 0000b
			Global configuration register (CH547 application)	0100 0000b
			Global configuration register (CH546 Bootloader)	0010 0000b
			Global configuration register (CH546 application)	0000 0000b
	CHIP_ID	A1h	CH547 chip ID (read only)	0100 0111b
			CH546 chip ID (read only)	0100 0110b
	SAFE_MOD	A1h	Safe mode control register (write only)	0000 0000b
	DPH	83h	Data address pointer high 8 bits	0000 0000b
	DPL	82h	Data address pointer low 8 bits	0000 0000b
	DPTR	82h	16-bit SFR consists of DPL and DPH	0000h
	SP	81h	Stack pointer	0000 0111b
Clock, sleep and power supply control registers	WDOG_COUNT	FFh	Watchdog count register	0000 0000b
	RESET_KEEP	FEh	Reset keep register (power on reset)	0000 0000b
	POWER_CFG	BAh	Power management configuration register	0000 0011b
	CLOCK_CFG	B9h	System clock configuration register	1000 0011b
	WAKE_CTRL	A9h	Wake-up control register	0000 0000b
	PCON	87h	Power control register (power on reset)	0001 0000b
Interrupt control registers	IP_EX	E9h	Extend interrupt priority register	0000 0000b
	IE_EX	E8h	Extend interrupt enable register	0000 0000b
	GPIO_IE	C7h	GPIO interrupt enable register	0000 0000b
	IP	B8h	Interrupt priority register	0000 0000b
	INTX	B3h	Extend external interrupt control register	0000 0000b
	IE	A8h	Interrupt enable register	0000 0000b
Flash-ROM registers	ROM_DATA_HH	8Fh	High byte of flash-ROM data register high word (read only)	xxxx xxxxb

	ROM_DATA_HL	8Eh	Low byte of flash-ROM data register high word (read only)	xxxx xxxxb
	ROM_DATA_HI	8Eh	16-bit SFR consists of ROM_DATA_HL and ROM_DATA_HH	xxxxh
	ROM_BUF_MOD	8Fh	Buffer mode register for flash-ROM erase/program operation	xxxx xxxxb
	ROM_DAT_BUF	8Eh	Data butter register for flash-ROM erase/program operation	xxxx xxxxb
	ROM_STATUS	86h	flash-ROM status register (read only)	0000 0000b
	ROM_CTRL	86h	flash-ROM control register (write only)	0000 0000b
	ROM_ADDR_H	85h	flash-ROM address register high	xxxx xxxxb
	ROM_ADDR_L	84h	flash-ROM address register low	xxxx xxxxb
	ROM_ADDR	84h	16-bit SFR consists of ROM_ADDR_L and ROM_ADDR_H	xxxxh
	ROM_DATA_LH	85h	High byte of flash-ROM data register low word (read only)	xxxx xxxxb
	ROM_DATA_LL	84h	Low byte of flash-ROM data register low word (read only)	xxxx xxxxb
	ROM_DATA_LO	84h	16-bit SFR consists of ROM_DATA_LL and ROM_DATA_LH	xxxxh
Port setting registers	XBUS_AUX	A2h	XBUS auxiliary configuration register	0000 0000b
	PIN_FUNC	AAh	Pin function selection register	0000 0000b
	P0_DIR_PU	C5h	Port0 direction control and pull-up enable register	1111 1111b
	P0_MOD_OC	C4h	Port0 output mode register	1111 1111b
	P4_DIR_PU	C3h	Port4 direction control and pull-up enable register	1111 1111b
	P4_MOD_OC	C2h	Port4 output mode register	1111 1111b
	P3_DIR_PU	97h	Port3 direction control and pull-up enable register	1111 1111b
	P3_MOD_OC	96h	Port3 output mode register	1111 1111b
	P2_DIR_PU	95h	Port2 direction control and pull-up enable register	1111 1111b
	P2_MOD_OC	94h	Port2 output mode register	1111 1111b
	P1_DIR_PU	93h	Port1 direction control and pull-up enable register	1111 1111b
	P1_MOD_OC	92h	Port1 output mode register	1111 1111b
	P5	ABh	Port5 input & output register	0010 0000b
	P4	C0h	Port4 input & output register	1111 1111b
	P3	B0h	Port3 input & output register	1111 1111b
	P2	A0h	Port2 input & output register	1111 1111b
	P1	90h	Port1 input & output register	1111 1111b
	P0	80h	Port0 input & output register	1111 1111b
Timer/counter 0 and 1 registers	TH1	8Dh	Timer1 count register high	xxxx xxxxb
	TH0	8Ch	Timer0 count register high	xxxx xxxxb
	TL1	8Bh	Timer1 count register low	xxxx xxxxb
	TL0	8Ah	Timer0 count register low	xxxx xxxxb
	TMOD	89h	Timer0/1 mode register	0000 0000b

	TCON	88h	Timer0/1 control register	0000 0000b
UART0 registers	SBUF	99h	UART0 data register	xxxx xxxxb
	SCON	98h	UART0 control register	0000 0000b
Timer/counter 2 registers	TH2	CDh	Timer2 count register high	0000 0000b
	TL2	CCh	Timer2 count register low	0000 0000b
	T2COUNT	CCh	16-bit SFR consists of TL2 and TH2	0000h
	RCAP2H	CBh	Count reload/capature 2 data register high	0000 0000b
	RCAP2L	CAh	Count reload/capature 2 data register low	0000 0000b
	RCAP2	CAh	16-bit SFR consists of RCAP2L and RCAP2H	0000h
	T2MOD	C9h	Timer2 mode register	0000 0000b
	T2CON	C8h	Timer2 control register	0000 0000b
PWMX registers	PWM_DATA3	A3h	PWM3 data register	xxxx xxxxb
	PWM_CTRL2	9Fh	PWM extend control register	0000 0000b
	PWM_CK_SE	9Eh	PWM clock divisor setting register	0000 0000b
	PWM_CTRL	9Dh	PWM control register	0000 0010b
	PWM_DATA0	9Ch	PWM0 data register	xxxx xxxxb
	PWM_DATA1	9Bh	PWM1 data register	xxxx xxxxb
	PWM_DATA2	9Ah	PWM2 data register	xxxx xxxxb
SPI0 registers	SPI0_SETUP	FCh	SPI0 setup register	0000 0000b
	SPI0_S_PRE	FBh	SPI0 slave preset value register	0010 0000b
	SPI0_CK_SE	FBh	SPI0 clock divisor setting register	0010 0000b
	SPI0_CTRL	FAh	SPI0 control register	0000 0010b
	SPI0_DATA	F9h	SPI0 data register	xxxx xxxxb
	SPI0_STAT	F8h	SPI0 status register	0000 1000b
UART1 registers	SIF1	BFh	UART1 interrupt status register	0000 0000b
	SBAUD1	BEh	UART1 baud rate setting register	xxxx xxxxb
	SBUF1	BDh	UART1 data register	xxxx xxxxb
	SCON1	BCh	UART1 control register	0100 0000b
UART2 registers	SIF2	B7h	UART2 interrupt status register	0000 0000b
	SBAUD2	B6h	UART2 baud rate setting register	xxxx xxxxb
	SBUF2	B5h	UART2 data register	xxxx xxxxb
	SCON2	B4h	UART2 control register	0000 0000b
UART3 registers	SIF3	AFh	UART3 interrupt status register	0000 0000b
	SBAUD3	AEh	UART3 baud rate setting register	xxxx xxxxb
	SBUF3	ADh	UART3 data register	xxxx xxxxb
	SCON3	ACh	UART3 control register	0000 0000b
ADC/TKEY registers	ADC_PIN	F7h	ADC pin digital input control register	0000 0000b
	ADC_CHAN	F6h	ADC analog signal channel selection register	0000 0000b
	ADC_DAT_H	F5h	ADC result data high byte (read only)	0000 xxxxb
	ADC_DAT_L	F4h	ADC result data low byte (read only)	xxxx xxxxb
	ADC_DAT	F4h	16-bit SFR consists of ADC_DAT_L and ADC_DAT_H	0xxxh
	ADC_CFG	F3h	ADC configuration register	0000 0000b

	ADC_CTRL	F2h	ADC control and status register	x000 000xb
	TKEY_CTRL	F1h	Touch key charging pulse width control register (write only)	0000 0000b
USB registers	UEP1_DMA_H	EFh	Endpoint1 buffer start address high byte	0000 0xxxb
	UEP1_DMA_L	EEh	Endpoint 1 buffer start address low byte	xxxx xxxxb
	UEP1_DMA	EEh	16-bit SFR consists of UEP1_DMA_L and UEP1_DMA_H	0xxxh
	UEP0_DMA_H	EDh	Endpoint0&4 buffer start address high byte	0000 0xxxb
	UEP0_DMA_L	ECh	Endpoint0&4 buffer start address low byte	xxxx xxxxb
	UEP0_DMA	ECh	16-bit SFR consists of UEP0_DMA_L and UEP0_DMA_H	0xxxh
	UEP2_3_MOD	EBh	Endpoint2&3 mode control register	0000 0000b
	UEP4_1_MOD	EAh	Endpoint1& 4 mode control register	0000 0000b
	UEP3_DMA_H	E7h	Endpoint3 buffer start address high byte	0000 0xxxb
	UEP3_DMA_L	E6h	Endpoint3 buffer start address low byte	xxxx xxxxb
	UEP3_DMA	E6h	16-bit SFR consists of UEP3_DMA_L and UEP3_DMA_H	0xxxh
	UEP2_DMA_H	E5h	Endpoint2 buffer start address high byte	0000 0xxxb
	UEP2_DMA_L	E4h	Endpoint2 buffer start address low byte	xxxx xxxxb
	UEP2_DMA	E4h	16-bit SFR consists of UEP2_DMA_L and UEP2_DMA_H	0xxxh
	USB_DEV_AD	E3h	USB device address register	0000 0000b
	USB_CTRL	E2h	USB control register	0000 0110b
	USB_INT_EN	E1h	USB interrupt enable register	0000 0000b
	UEP4_T_LEN	DFh	Endpoint4 transmittal length register	0xxx xxxxb
	UEP4_CTRL	DEh	Endpoint4 control register	0000 0000b
	UEP0_T_LEN	DDh	Endpoint0 transmittal length register	0xxx xxxxb
	UEP0_CTRL	DCh	Endpoint0 control register	0000 0000b
	USB_RX_LEN	DBh	USB receiving length register (read only)	0xxx xxxxb
	USB_MIS_ST	DAh	USB miscellaneous status register (read only)	xx10 1000b
	USB_INT_ST	D9h	USB interrupt status register (read only)	00xx xxxxb
	USB_INT_FG	D8h	USB interrupt flag register	0010 0000b
	UEP3_T_LEN	D7h	Endpoint3 transmittal length register	0xxx xxxxb
	UEP3_CTRL	D6h	Endpoint3 control register	0000 0000b
	UEP2_T_LEN	D5h	Endpoint2 transmittal length register	0000 0000b
	UEP2_CTRL	D4h	Endpoint2 control register	0000 0000b
	UEP1_T_LEN	D3h	Endpoint1 transmittal length register	0xxx xxxxb
	UEP1_CTRL	D2h	Endpoint1 control register	0000 0000b
	UDEV_CTRL	D1h	USB device port control register	00xx 0000b

5.3 General 8051 Register

Table 5.3.1 List of general 8051 registers

Name	Address	Description	Reset value

B	F0h	B register	00h
A, ACC	E0h	Accumulator	00h
PSW	D0h	Program status register	00h
GLOBAL_CFG	B1h	Global configuration register (CH547 Bootloader)	60h
		Global configuration register (CH547 application)	40h
		Global configuration register (CH546 Bootloader)	20h
		Global configuration register (CH546 application)	00h
CHIP_ID	A1h	CH547 chip ID (read only)	47h
		CH546 chip ID (read only)	46h
SAFE_MOD	A1h	Safe mode control register (write only)	00h
PCON	87h	Power control register (power on reset)	10h
DPH	83h	Data address pointer high 8 bits	00h
DPL	82h	Data address pointer low 8 bits	00h
DPTR	82h	16-bit SFR consists of DPL and DPH	0000h
SP	81h	Stack pointer	07h

B Register (B):

Bit	Name	Access	Description	Reset value
[7:0]	B	RW	Arithmetic register, mainly used for multiplication and division operations; it supports bit addressing	00h

A accumulator (A, ACC):

Bit	Name	Access	Description	Reset value
[7:0]	A/ACC	RW	Arithmetic accumulator, supports bit addressing	00h

Program Status Register (PSW):

Bit	Name	Access	Description	Reset value
7	CY	RW	Carry flag bit: when executing arithmetic operation and logic operation instruction, it is used to record the highest bit with input or debit; when performing 8-bit addition operation, if the highest bit is input, the position bit, otherwise it is cleared; when performing 8-bit subtraction operation, if the bit is debited, the position bit, otherwise it is cleared; logic instruction can make the position bit or clear it.	0
6	AC	RW	Auxiliary carry flag bit: when recording addition and subtraction operations, the lower 4 bits have an input or a borrow to the higher 4 bits, the AC is set, otherwise it is cleared.	0
5	F0	RW	Bit 0 of the bit-addressable general-purpose flag: user-definable, can be software cleared or set.	0
4	RS1	RW	Register group select bit high.	0
3	RS0	RW	Register group select bit low.	0
2	OV	RW	Overflow flag bit: When the result of an addition or subtraction operation exceeds 8 binary digits, the OV is set to 1 and the flag overflows, otherwise it is cleared to 0.	0

1	F1	RW	Bit 1 of the bit-addressable general flag: user-definable, can be software cleared or set.	0
0	P	RO	Parity flag bit: records the parity of 1 in accumulator A after the instruction is executed, P is set for an odd number of 1s, and P is cleared for an even number of 1s.	0

The status of the processor is stored in the status register PSW, which supports bit-by-bit addressing. The status word contains the feed flag bits, the auxiliary feed flag bits for BCD code processing, the parity flag bits, the overflow flag bits, and RS0 and RS1 for working register group selection. the areas where the working register groups are located can be accessed either directly or indirectly.

Table 5.3.2 RS1 and RS0 working register set selection table

RS1	RS0	Working register set
0	0	0 set (00h-07h)
0	1	1 set (08h-0Fh)
1	0	2 set (10h-17h)
1	1	3 set (18h-1Fh)

Table 5.3.3 Operations affecting flag bits (X means that flag bit is related to the operation result)

Operation	CY	OV	AC	Operation	CY	OV	AC
ADD	X	X	X	SETB C	1		
ADDC	X	X	X	CLR C	0		
SUBB	X	X	X	CPL C	X		
MUL	0	X		MOV C, bit	X		
DIV	0	X		ANL C, bit	X		
DA A	X			ANL C,/bit	X		
RRC A	X			ORL C, bit	X		
RLC A	X			ORL C,/bit	X		
CJNE	X						

Data pointer register (DPTR)：

Bit	Name	Access	Description	Reset value
[7:0]	DPL	RW	Data pointer low byte	00h
[7:0]	DPH	RW	Data pointer high byte	00h

The16-bit data pointer (DPTR) consists of DPL and DPH, which is used to access xSFR, xBUS, xRAM data memory and program memory. Actually, DPTR has 2 groups physical 16-bit data pointers DPTR0 and DPTR1, which are dynamically switched by DPS in XBUS_AUX.

Stack pointer (SP):

Bit	Name	Access	Description	Reset value
[7:0]	SP	RW	Stack pointer, mainly used for program and interrupt call, also for data push and pull	07h

Stack specific functions: preserving breakpoints and saving the context, managed based on the last-in-first-out

principle. When pushing data onto the stack, the SP pointer automatically increments by 1 to save the data or breakpoint information. When popping data from the stack, the data unit pointed to by the SP pointer is retrieved, and the SP pointer automatically decrements by 1. The initial value of SP after a reset is 07h, and the default stack storage starts from 08h.

5.4 Unique Register

Global Configuration Register (GLOBAL_CFG), only can be written in safe mode:

Bit	Name	Access	Description	Reset value
[7:6]	Reserved	RO	For CH547, fixed to 01	01b
[7:6]	Reserved	RO	For CH546, fixed to 00	00b
5	bBOOT_LOAD	RO	Boot loader status bit, for discriminating Bootloader or Application. Set to 1 by power on reset. Cleared to 0 by software reset. For all chips with ISP boot loader: 1: It has never been reset by software, usually in ISP boot loader state. 0: It has been reset by software, usually in application state.	1
4	bSW_RESET	RW	Software reset. If it is set to 1, software reset occurs. Automatically reset by hardware.	0
3	bCODE_WE	RW	Flash-ROM write enable: 0: Write protection. 1: Flash-ROM can be written and erased.	0
2	bDATA_WE	RW	Flash-ROM DataFlash write enable: 0: Write protection. 1: DataFlash can be written and erased.	0
1	Reserved	RO		0
0	bWDOG_EN	RW	Watchdog reset enable: 0: As timer only. 1: Enable reset if timer overflow.	0

Chip ID (CHIP_ID):

Bit	Name	Access	Description	Reset value
[7:0]	CHIP_ID	RO	For CH547, fixed to 47h to identify the chip	47h
[7:0]	CHIP_ID	RO	For CH546, fixed to 46h to identify the chip	46h

Safe Mode Control Register (SAFE_MOD):

Bit	Name	Access	Description	Reset value
[7:0]	SAFE_MOD	WO	To enter or get out of safe mode	00h

Some SFRs can only be written in safe mode, while they are always read-only in non-safe mode. Steps to enter safe mode:

(1). Write 55h to register.

(2). Write AAh to register.

(3). 13-23 system frequency periods are in safe mode, one or more safe SFRs or general SFRs can be changed during this time.

(4). After the period expires, safe mode ends automatically.

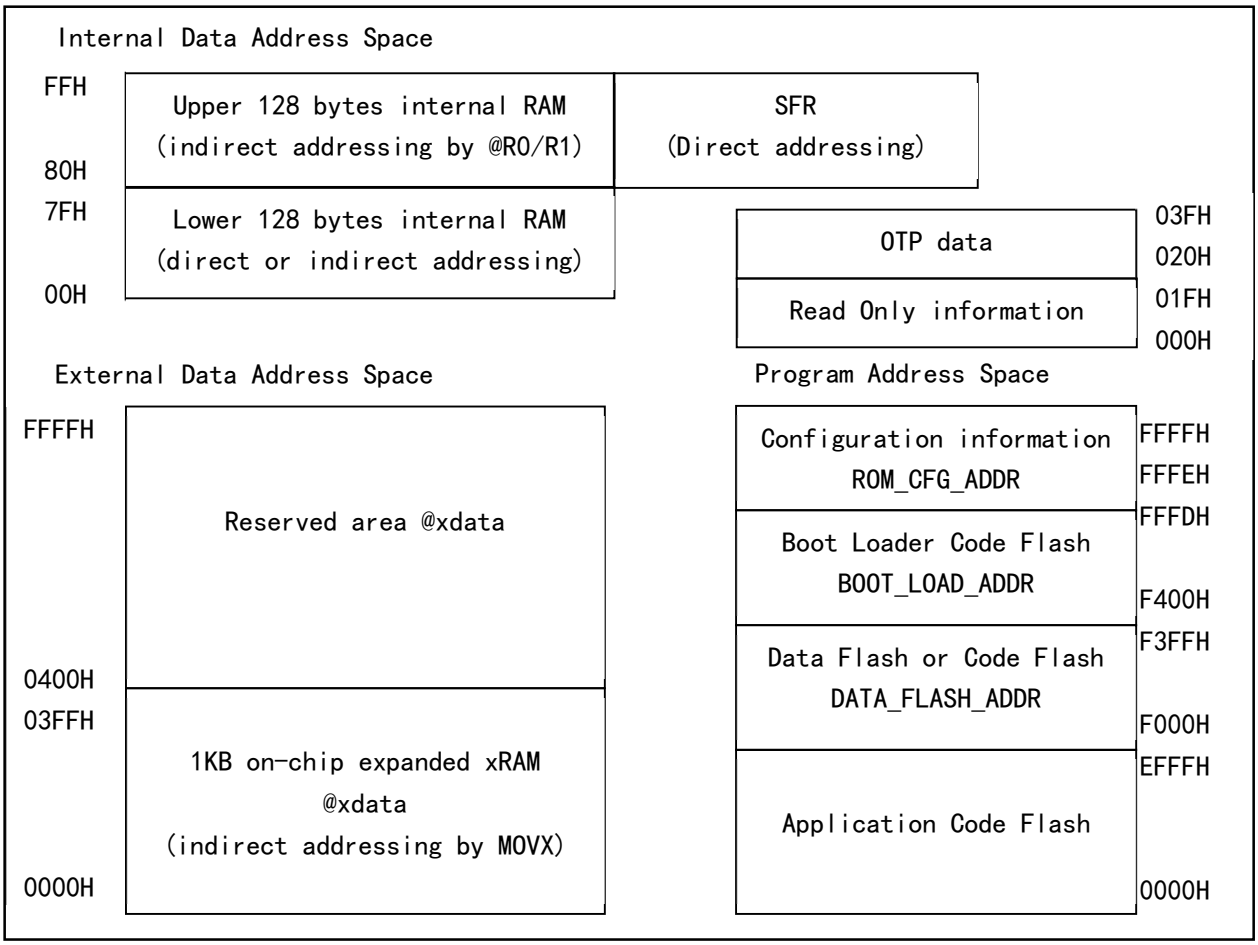
(5). Write anything to this register can get out of safe mode in advance.

6. Memory Structure

6.1 Memory Space

CH547 addressing memory is divided into program memory, internal code memory, external data memory, read only and OTP space.

Figure 6.1 Memory structure diagram



6.2 Program Memory

Program memory is total 64KB, as shown in Figure 6.1, and all is used for flash-ROM, including CodeFlash to save the command code, DataFlash to save the nonvolatile data, and Configuration Information space to configure the information.

Data Flash (EEPROM) addressing from F000h to F3FFH supports byte (8 bits) read, byte (8 bits) write, block (1 to 64 bytes) write, and block (64 bytes) erase. keeping the data after chip power-down, and also may be used for CodeFlash.

CodeFlash includes application code of low address and the Bootloader code of high address, they can also be combined with DataFlash for storing single application code.

For CH546, application code area of Code Flash is only 32KB.

Configuration information is total 16 bits, and may be configured by programmer, refer to Table 6.1.

Table 6.2 Description of flash-ROM Configuration Information

Address	Name	Description	Recommended value

15	Code_Protect	Code and data protection modes in flash-ROM: 0 - readout permitted; 1 - programmer readout prohibited, program confidential	0/1
14	No_Boot_Load	BootLoader start mode enable: 0: Start from address 0000h. 1: Start from address F400h.	1
13	En_Long_Reset	Additional delay during power-up reset enable: 0: Standard short reset. 1: Long reset, add 44mS.	0
12	En_P5.7_RESET	Enable P5.7 as a manual reset input pin: 0: Disable. 1: Enable RST.	1
11		Reserved	0
10		Reserved	0
9	Must_1	(Auto set to 1 by the programmer)	1
8	Must_0	(Auto set to 0 by the programmer)	0
[7:3]	All_0	(Auto set to 00000b by the programmer)	00000b
[2:0]	LV_RST_VOL (Vpot)	LVR threshold voltage selection (error 4%): 000, 001: 2.4V. 010: 2.7V. 011: 3.0V. 100: 3.6V. 101: 4.0V. 110: 4.3V. 111: 4.6V.	000b

6.3 Data Memory Space

Internal data memory is total 256 bytes, as shown in Figure 6.1, are all used for SFR and iRAM, iRAM is used for stack and fast data cache, including R0-R7, bit data, byte data and idata.

External data memory is total 64KB, as shown in Figure 6.1. Part of it is used for 1KB on-chip expanded xRAM, others (0400h to FFFFh) are reserved area.

Read-only information space and OTP data space each has 32 bytes, as shown in Figure 6.1, and they need to be accessed through a special operation.

6.4 flash-ROM Register

Table 6.4 List of flash-ROM registers

Name	Address	Description	Reset value
ROM_DATA_HH	8Fh	High byte of flash-ROM data register high word (read only)	xxh
ROM_DATA_HL	8Eh	Low byte of flash-ROM data register high word (read only)	xxh
ROM_DATA_HI	8Eh	16-bit SFR consists of ROM_DATA_HL and ROM_DATA_HH	xxxxh
ROM_BUF_MOD	8Fh	Buffer mode register for flash-ROM erase operation	xxh
ROM_DAT_BUF	8Eh	Data buffer register for flash-ROM erase operation	xxh
ROM_STATUS	86h	flash-ROM status register (read only)	00h
ROM_CTRL	86h	flash-ROM control register (write only)	00h

ROM_ADDR_H	85h	flash-ROM address register high	xxh
ROM_ADDR_L	84h	flash-ROM address register low	xxh
ROM_ADDR	84h	16-bit SFR consists of ROM_ADDR_L and ROM_ADDR_H	xxxxh
ROM_DATA_LH	85h	High byte of flash-ROM data register low word (read only)	xxh
ROM_DATA_LL	84h	Low byte of flash-ROM data register low word (read only)	xxh
ROM_DATA_LO	84h	16-bit SFR consists of ROM_DATA_LL and ROM_DATA_LH	xxxxh

flash-ROM Address Register (ROM_ADDR):

Bit	Name	Access	Description	Reset value
[7:0]	ROM_ADDR_H	RW	Flash-ROM address register high byte	xxh
[7:0]	ROM_ADDR_L	RW	Flash-ROM address register low byte	xxh

flash-ROM Data Register (ROM_DATA_HI, ROM_DATA_LO):

Bit	Name	Access	Description	Reset value
[7:0]	ROM_DATA_HH	RO	High byte of flash-ROM data register high word (16-bit)	xxh
[7:0]	ROM_DATA_HL	RO	Low byte of flash-ROM data register high word (16-bit)	xxh
[7:0]	ROM_DATA_LH	RO	High byte of flash-ROM data register low word (16-bit)	xxh
[7:0]	ROM_DATA_LL	RO	Low byte of flash-ROM data register low word (16-bit)	xxh

Buffer Mode Register for flash-ROM Erase Operation (ROM_BUF_MOD):

Bit	Name	Access	Description	Reset value
7	bROM_BUF_BYTE	RW	Buffer mode for flash-ROM erase operation (erase or program): 0: Select the data block programming mode, the data to be written is stored in xRAM pointed by DPTR, during programming CH547 automatically removes the data from xRAM in sequence and stores it temporarily in ROM_DAT_BUF before writing to flash-ROM, supports 1 byte to 64 bytes data length, actual length = MASK_ROM_ADR_END - ROM_ADDR_L [5:0] + 1; 1: Select single byte programming or 64-byte block erase mode, data to be written is stored directly in ROM_DAT_BUF.	x
6	Reserved	RW	Reserved	x
[5:0]	MASK_ROM_ADDR	RW	In flash-ROM block program mode, these bits are the lower 6 bits of the end address of the flash-ROM block program operation (including such address). In flash-ROM byte program or 64-byte block erase mode, these bits are reserved and recommended to be 00h.	xxh

Data Buffer Register for flash-ROM Erase Operation (ROM_DAT_BUF):

Bit	Name	Access	Description	Reset value
[7:0]	ROM_DAT_BUF	RW	Data buffer register for flash-ROM erase operation	xxh

Flash-ROM Control Register (ROM_CTRL):

Bit	Name	Access	Description	Reset value
[7:0]	ROM_CTRL	WO	Flash-ROM control register	00h

Flash-ROM Status Register (ROM_STATUS):

Bit	Name	Access	Description	Reset value
7	Reserved	RO	Reserved	1
6	bROM_ADDR_OK	RO	Flash-ROM operation address OK: 0: The parameter is invalid. 1: The address is valid.	0
[5:2]	Reserved	RO	Reserved	0000b
1	bROM_CMD_ERR	RO	Flash-ROM operation command error: 0: The command is valid. 1: Unknown command or timeout.	0
0	Reserved	RO	Reserved	0

6.5 Flash-ROM Operation Steps

1. Flash-ROM erase, changing all data bits in the target block to 0:
   (1). Get into safe mode, SAFE_MOD = 55h; SAFE_MOD = 0AAh;
   (2). Enable writing by setting GLOBAL_CFG, bCODE_WE corresponds to code, and bDATA_WE to data;
   (3). Set ROM_ADDR, write in 16-bit destination address, high 10 bits valid only;
   (4). Set ROM_BUF_MOD to 80h, to select 64-byte block erase mode;
   (5). Optional step. Set ROM_DAT_BUF to 00h;
   (6). Set ROM_CTRL to 0A6h, to execute block erase operation, and the program will automatically suspend during the operation;
   (7). After the operation, the program goes on. Read ROM_STATUS to check the operation result. If multiple blocks need to be erased, repeat steps (3) to (7). The sequence of step (3), (4), and (5) can be exchanged;
   (8). Get into safe mode again, SAFE_MOD = 55h; SAFE_MOD = 0AAh;
   (9). Enable write protection by setting GLOBAL_CFG (bCODE_WE=0, bDATA_WE=0).

2. Flash-ROM byte write, changing some data bits in the target byte from 0 to 1 (the bit data cannot be changed from 1 to 0):
   (1). Get into safe mode, SAFE_MOD = 55h; SAFE_MOD = 0AAh;
   (2). Enable writing by setting GLOBAL_CFG (bCODE_WE corresponds to code, and bDATA_WE to data);
   (3). Set ROM_ADDR, write in 16-bit destination address;
   (4). Set ROM_BUF_MOD to 80h, to select byte program mode;
   (5). Set ROM_DAT_BUF as the byte data to be written;
   (6). Set ROM_CTRL to9Ah, to execute write operation, and the program will automatically suspend during operation;

(7). After the operation, the program goes on. Read ROM_STATUS to check the operation result. If multiple blocks need to be written, repeat steps (3) to (7). The sequence of step (3), (4), and (5) can be exchanged;
(8). Get into safe mode again, SAFE_MOD = 55h; SAFE_MOD = 0AAh;
(9). Enable write protection by setting GLOBAL_CFG (bCODE_WE=0, bDATA_WE=0).

3. Flash-ROM block write, changing some data bits in multiple target bytes from 0 to 1 (the bit data cannot be changed from 1 to 0):
(1). Get into safe mode, SAFE_MOD = 55h; SAFE_MOD = 0AAh;
(2). Enable writing by setting GLOBAL_CFG (bCODE_WE corresponds to code, and bDATA_WE to data);
(3). Set ROM_ADDR, write in 16-bit start destination address, such as 1357h;
(4). Set ROM_BUF_MOD as the lower 6 bits of the end destination address (included), and such end address should be greater than or equal to the ROM_ADDR_L[5:0] start destination address, select block program mode. For example: if the end address is 1364h, ROM_BUF_MOD should be set to 24h (64H &3Fh), and the calculated number of bytes of the data block =0Dh;
(5). In xRAM, allocate a buffer based on the alignment in 64 bytes, such as 0580h to 05BFh, specify the offset address in such buffer with the lower 6 bits of the start destination address, obtain the xRAM buffer start address of this data block program operation, store the data block to be written from the xRAM buffer start address, and set the xRAM buffer start address into DPTR, e.g. DPTR=0580h+(57h&3Fh)=0597h, actually only the xRAM of 0597h-05A4h address is used in this programming operation;
(6). Set ROM_CTRL to 09Ah, to execute write operation, and the program will automatically suspend during operation;
(7). After the operation, the program goes on. Read ROM_STATUS to check the operation result. If multiple blocks need to be written, repeat steps (3) to (7). The sequence of step (3), (4), and (5) can be exchanged;
(8). Get into safe mode again, SAFE_MOD = 55h; SAFE_MOD = 0AAh;
(9). Enable write protection by setting GLOBAL_CFG (bCODE_WE=0, bDATA_WE=0).

4. Flash-ROM read:
Read data or code from the destination address through instruction MOVC or pointer of program area.

5. OTP byte write, changing some data bits in the target byte from 0 to 1 (the bit data cannot be changed from 1 to 0):
(1). Get into safe mode, SAFE_MOD = 55h; SAFE_MOD = 0AAh;
(2). Enable writing by setting GLOBAL_CFG (bDATA_WE);
(3). Set ROM_ADDR, write destination address (20h-3Fh), actually only the higher 4 bits of the lower 6 bits are valid;
(4). Set ROM_BUF_MOD to 80h, to select byte program mode;
(5). Set ROM_DAT_BUF as the byte data to be written;
(6). Set ROM_CTRL to 099h, to execute write operation, and the program will automatically suspend during operation;
(7). After the operation, the program goes on. Read ROM_STATUS to check the operation result. If multiple blocks need to be written, repeat steps (3) to (7). The sequence of step (3), (4), and (5) can be exchanged;
(8). Get into safe mode again, SAFE_MOD = 55h; SAFE_MOD = 0AAh;
(9). Enable write protection by setting GLOBAL_CFG (bCODE_WE=0, bDATA_WE=0).

6. ReadOnly information space or OTP data space read in 4 bytes:

(1). Set ROM_ADDR, write the destination address based on the alignment in 4 bytes (00h-3Fh), actually only the lower 6 bits are valid;
(2). Set ROM_CTRL to 08Dh, to execute read operation, and the program will automatically suspend during operation;
(3). After the operation, the program goes on. Read ROM_STATUS to check the operation result;
(4). Obtain 4-byte data from ROM_DATA_HI and ROM_DATA_LO in flash-ROM data register.

7. Note: When erasing flash-ROM/EEPROM, it is recommended to do so only at an ambient temperature of -20°C to 85°C. If erasure operations are carried out outside the above temperature range, it is generally normal, but the possibility of reducing the data retention capacity TDR and the number of erasures NEPCE or even affecting data accuracy cannot be ruled out. If programming erasure operations are carried out outside the above temperature range, although this is normally normal, the possibility of reducing the data retention capacity TDR and the number of erasures NEPCE and even the accuracy of the data cannot be ruled out.

6.6 On-board Program and ISP Download

When Code_Protect=0, the code and data in CH547 flash-ROM may be read and written through synchronous serial interface by an external programmer. When Code_Protect=1, the code and data in flash-ROM are protected, it can be erased but not read, Code_Protect will be removed after erase when power-up.
When CH547 presets BootLoader, it supports downloading application code through USB or UART. Without Bootloader, application code and Bootloader may only download through specialized programmer. Reserve 4 wires between CH547 and programmer for on-board programming in the circuit. The necessary pins are: P1.4, P1.6 and P1.7.

Table 6.6.1 Wires between CH547 and programmer

Pin	GPIO	Description
RST	P5.7	Programmed reset control pin (optional), high to allow entry into programmed state
SCS	P1.4	Programmed chip select input pin (necessary), default high, active low
SCK	P1.7	Programmed clock input pin (necessary)
MISO	P1.6	Data output pin in programming state (necessary)

6.7 Global Unique ID

CH547 MCUs all have a global unique identification number (ID) when out of factory. ID and verification total 8 bytes, located in the special read-only register form address 10h. For details, please refer to program routines.

Table 6.7.1 Chip ID address table

Offset address	ID data description
10h、11h	ID first word data, in order, the lowest byte of the ID number, the next lowest byte
12h、13h	ID second word data, in order, the next highest byte and the highest byte of the ID number
14h、15h	ID last word data, in order, is the second highest byte and highest byte of the 48-bit ID number
16h、17h	The 16-bit sum of the first, second and last word of the ID data, used for ID checksum

The ID number can be used with the downloading tools to encrypt the target program. For the general application, only the first 32 bits of the ID number are used.

6.8 Calibration Information for Temperature Sensor (TS)

The calibration information for the temperature sensor is located in the area with offset address 0Ch in the read-only information area. Please refer to the C example program for details of the operation.

7. Power Management, Sleep and Reset

7.1 External Power in

CH547 has a built-in 5V to 3.3V low dropout voltage regulator (LDO), and the generated 3.3V power is used in USB and other modules. CH547 supports external 5V or 3.3V or even 2.8V supply voltage input. Refer to the following table for the two supply voltage input modes.

External power voltage	VDD voltage: external voltage 2.8V~5V	V33 voltage: internal USB voltage 3.3V (Notes: V33 will be automatically shorted to VDD during sleep)
3.3V or 2.8V Including <3.6V	3.3V voltage input to I/O and LDO. A decoupling capacitor not less than 0.1uF to the ground necessarily.	Short VDD input as internal USB power. A decoupling capacitor not less than 0.1uF to the ground necessarily.
5V Including >3.6V	5V voltage input to I/O and LDO. A decoupling capacitor not less than 0.1uF to the ground necessarily.	Internal voltage regulator 3.3V output and 3.3V internal USB power input. A decoupling capacitor not less than 0.1uF to the ground necessarily.

After power on or system reset, CH547 is in running state by default. On the premise that the performance meets the requirements, the power consumption can be reduced during operation by appropriately reducing the system clock. When CH547 does not need to run at all, set PD in PCON to enter sleep mode, and may be waked up by USB, UART0, UART1, SPI0 and part of GPIOs.

7.2 Power and Sleep Control Register

Table 7.2.1 Power and sleep control registers

Name	Address	Description	Reset value
WDOG_COUNT	FFh	Watchdog count register	00h
RESET_KEEP	FEh	Reset keep register	00h
POWER_CFG	BAh	Power management configuration register	0xh
WAKE_CTRL	A9h	Wake-up control register	00h
PCON	87h	Power control register	10h

Watchdog Count Register (WDOG_COUNT):

Bit	Name	Access	Description	Reset value
[7:0]	WDOG_COUNT	RW	Watchdog current count, count full 0FFh turn 00h when overflow, overflow automatically set interrupt flag bWDOG_IF_TO to 1	00h

Reset Keep Register (RESET_KEEP):

Bit	Name	Access	Description	Reset value

[7:0]	RESET_KEEP	RW	Reset keep register, it may be modified by setting, except power-on reset may set it 0, no other resets may change it.	00h

Power Management Configuration Register (POWER_CFG), only can be written in safe mode:

Bit	Name	Access	Description	Reset value
7	bPWR_DN_MODE	RW	Sleep power off mode selection: 0: Power off/deep sleep mode, saving more power, but wake up slowly. 1: Standby/normal sleep mode, wake up quickly.	0
6	bUSB_PU_RES	RW	USB pull-up resistance selection: 0: 1.5KΩ, for the case when V33 is 3.3V. 1: 7KΩ, for the case when V33 is 5V.	0
5	bLV_RST_OFF	RW	Low voltage reset detection module OFF: 0: Enable supply voltage detection and generate reset signal at low voltage. 1: Low voltage detection module off.	0
4	bLDO_3V3_OFF	RW	USB voltage regulator LDO OFF control (auto OFF during sleep): 0: 3.3V voltage is generated by VDD power supply for USB and other modules. 1: Disable LDO and internally short V33 to VDD.	0
3	bLDO_CORE_VOL	RW	Core voltage mode: 0: Normal voltage mode. 1: Boost voltage mode, with better performance, and support higher system clock.	0
[2:0]	MASK_ULLDO_VOL	RW	Data keep supply voltage selection in power off/deep sleep mode: 000: 2.0V. 001: 1.9V. 010: 1.8V. 011: 1.7V. 100: 1.6V. 101: 1.5V. 110: 1.4V. 111: 1.3V. The above are relative reference values which do not need to be adjusted under a 5V supply; If 3.3V supply is used, it is recommended to read first, subtract 2 from the lower 3 bits (if the original value is less than 2 the result is cleared to 0) and write back in safe mode in order to select the relative higher two data holding voltages.	xxxb

Wake-up Control Register (WAKE_CTRL), only can be written in safe mode:

Bit	Name	Access	Description	Reset value
7	bWAK_BY_USB	RW	USB event wake-up enable: 1: Enable. 0: Disable.	0

6	bWAK_RXD1_LO	RW	UART1 pin RXD1 low-level input event wake-up enable: 0: Disable. 1: Enable. Select RXD1 or RXD1_ according to bUART1_PIN_X=0/1.	0
5	bWAK_P1_5_LO	RW	P1.5 low-level wake-up enable 0: Disable. 1: Enable.	0
4	bWAK_P1_4_LO	RW	P1.4 low-level wake-up enable 0: Disable. 1: Enable.	0
3	bWAK_P0_3_LO	RW	P0.3 low-level wake-up enable 0: Disable. 1: Enable.	0
2	bWAK_P57H_INT3L	RW	P5.7 high-level and INT3 low level wake-up enable 0: Disable. 1: Enable.	0
1	bWAK_INT0E_P33L	RW	INT0 edge change and P3.3 low-level wake-up enable. 0: Disable. 1: Enable. INT0 selects INT0 or INT0_ according to bINT0_PIN_X=0/1.	0
0	bWAK_RXD0_LO	RW	UART0 pin RXD0 low-level input wake-up enable. 0: Disable. 1: Enable. Select RXD0 or RXD0_ according to bUART0_PIN_X=0/1.	0

Voltage comparator wake-up enable is controlled by bCMP_EN. When bCMP_EN is 1, it will automatically wake up if the comparator result changes.

Power Control Register (PCON):

Bit	Name	Access	Description	Reset value
7	SMOD	RW	Baud rate selection for UART0 mode 1/2/3 when timer1 is used to generate UART0 baud rate: 0: Slow mode. 1: Fast mode.	0
6	Reserved	RO	Reserved	0
5	bRST_FLAG1	R0	Recent reset flag high bit	0
4	bRST_FLAG0	R0	Recent reset flag low bit	1
3	GF1	RW	General purpose flag bit 1 User-defined. Can be reset and set by software	0
2	GF0	RW	General purpose flag bit 0 User-defined. Can be reset and set by software	0
1	PD	RW	Sleep mode enable, set to 1 and sleep, hardware automatically clears when waking up. It is strongly recommended to turn off global interrupts	0

			(EA=0) before sleep.	
0	Reserved	RO	Reserved	0

Table 7.2.2 Description of recent reset flag

bRST_FLAG1	bRST_FLAG0	Reset flag description
0	0	Software reset, source: bSW_RESET=1 and (bBOOT_LOAD=0 or bWDOG_EN=1)
0	1	Power on reset or low voltage detection reset, source: voltage on VDD is lower than checking voltage
1	0	Watchdog reset, source: bWDOG_EN=1 and watchdog timeout overflows
1	1	External input manual reset by RST pin, source: En_P5.7_RESET=1 and P5.7 high-level input

7.3 Reset Control

CH547 has 5 reset sources: power on reset, low voltage detection reset, external reset, software reset, and watchdog reset. The latter three are hot reset.

7.3.1 Power on Reset and Low Voltage Detection Reset

Power on reset (POR) generates from internal detection circuit, and auto delay Tpor to keep reset status. CH547 runs at the end of delay.

Low voltage detection reset (LVR) generates from internal voltage detection circuit. The LVR circuit continuously monitors the voltage on VDD pin. When it is lower than the detection level (Vpot), LVR generates, and auto delay Tpor to keep reset status. CH547 runs at the end of delay.

Only power-on reset and low voltage detection reset can enable CH547 to reload the configuration information and clear RESET_KEEP, other hot resets do not affect.

7.3.2 External Reset

External reset is generated by the high-level on RST. The reset occurs when En_P5.7_RESET=1, and high level on RST keeping time is longer than Trst. After high-level ends, auto delay Trdl to keep reset status. CH547 runs from address 0 at the end of delay.

7.3.3 Software Reset

CH547 supports internal software reset to reset the CPU and restart without external intervention. Set bSW_RESET in GLOBAL_CFG to 1 to execute software reset, and auto delay Trdl to keep reset status. CH547 runs from address 0 after delay, and the bSW_RESET bit is reset automatically by hardware.

When bSW_RESET is set to 1, if bBOOT_LOAD=0 or bWDOG_EN=1, then bRST_FLAG1/0 will indicate the software reset after reset. When bSW_RESET is set to 1, if bBOOT_LOAD=1 and bWDOG_EN=0, then bRST_FLAG1/0 will keep the reset flag of last time and no new flag.

Bootloader runs first after power-on reset if ISP Bootloader is downloaded, it switches to the application code through software reset based on requirement. This software reset will clear bBOOT_LOAD, but not affect bRST_FLAG1/0 (as bBOOT_LOAD=1 before reset), so bRST_FLAG1/0 still indicates power on reset status after switching to application state.

7.3.4 Watchdog Reset

Watchdog reset occurs when the watchdog timer overflows. Watchdog timer is an 8-bit counter, whose clock frequency is Fsys/131072, and the overflow signal is generated when count to 0FFh and turn to 00h.

Watchdog timer overflow signal will trigger bWDOG_IF_TO to 1, which is automatically reset when WDOG_COUNT is reloaded or when it goes into corresponding interrupt service.

Write different initial values to WDOG_COUNT to realize different timing period Twdc. When the system clock is 12MHz, Twdc is about 2.8 s when 00h is written, and about 1.4 s when 80h is written.

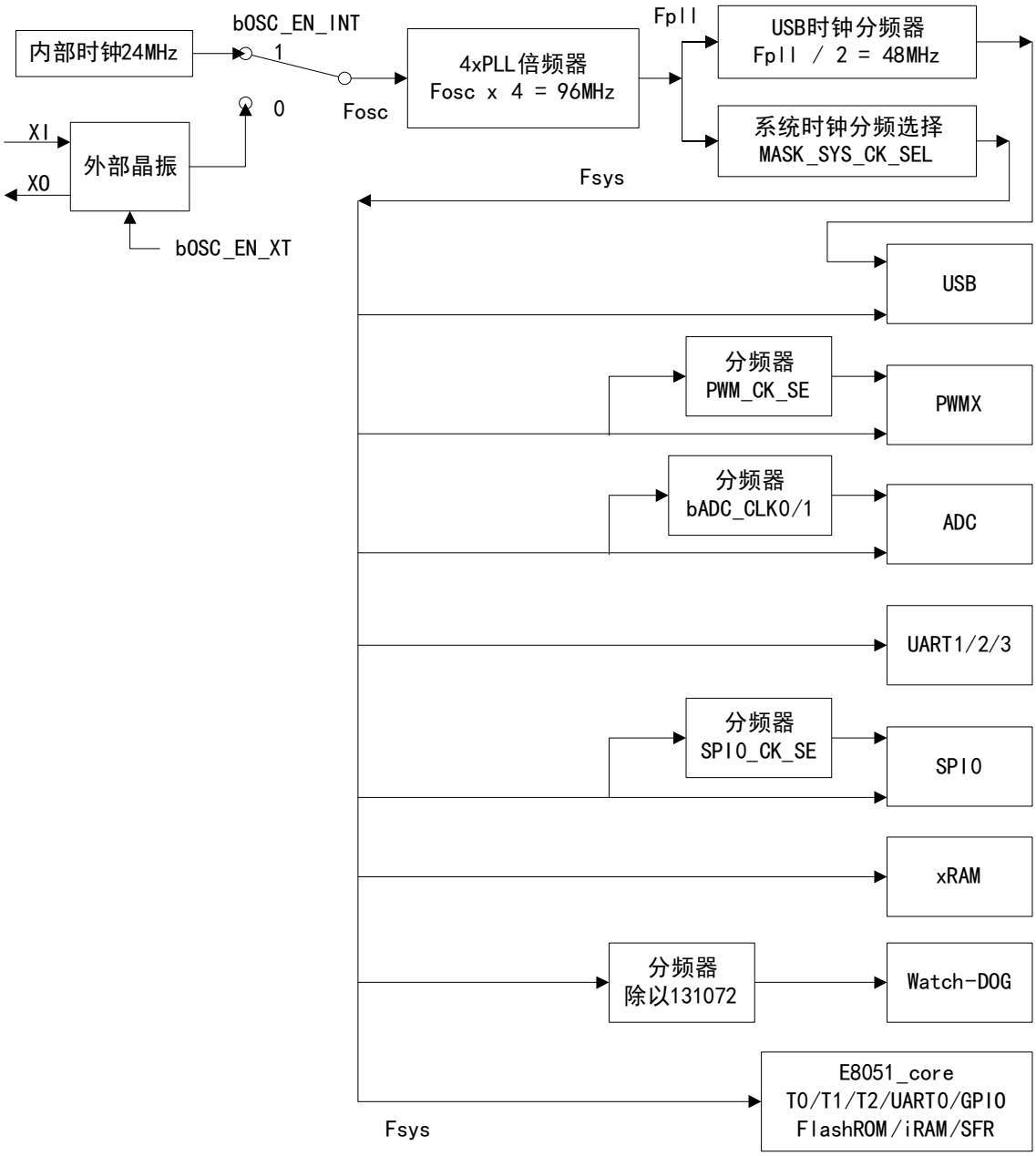
When watchdog timer overflows and bWDOG_EN=1, watchdog reset occurs. Auto delay Trdl to keep reset status. CH547 runs from address 0 after delay.

Clear WDOG_COUNT timely to avoid watchdog reset when bWDOG_EN = 1.

8. System Clock

8.1 Clock Block Diagram

Figure 8.1.1 Clock system and structure diagram



The internal clock or the external clock is used as the original clock Fosc after a binary selection, then after PLL multiplication to generate the Fpll high frequency clock, and finally after two sets of dividers to obtain the system clock Fsys and the USB module clock Fusb4x respectively. the system clock Fsys is provided directly to each module of the CH547.

8.2 Register Description

Table 8.2.1 Clock Control Register

Name	Address	Description	Reset value
CLOCK_CFG	B9h	System clock configuration register	83h

System clock configuration register (CLOCK_CFG), only can be written in safe mode:

Bit	Name	Access	Description	Reset value

7	bOSC_EN_INT	RW	Internal clock oscillator enable, a 1 enables the internal clock oscillator and selects the internal clock; a 0 disables the internal clock oscillator and selects the external crystal oscillator to provide the clock.	1
6	bOSC_EN_XT	RW	External crystal oscillator enable, this bit is 1 to enable the P4.6/XO pin as XI/XO and enable the oscillator, an external quartz crystal or ceramic oscillator is required between XI and XO; this bit is 0 to disable the external oscillator.	0
5	bWDOG_IF_TO	RO	The watchdog timer interrupt flag bit, a 1 in this bit indicates an interrupt, triggered by the timer overflow signal; a 0 in this bit indicates no interrupt. This bit is automatically cleared when the watchdog count register WDOG_COUNT is reloaded or when the corresponding interrupt service program is entered.	0
[4:3]	Reserved	RO	Reserved	00b
[2:0]	MASK_SYS_CK_SEL	RW	System clock frequency selection, refer to Table 8.2.2.	011b

Table 8.2.2 System clock frequency selection

MASK_SYS_CK_SEL	System main frequency Fsys	Relation with Fxt	Fsys when Fosc=24MHz
000b	Fpll / 512	Fxt / 128	187.5KHz
001b	Fpll / 128	Fxt / 32	750KHz
010b	Fpll / 32	Fxt / 8	3MHz
011b	Fpll / 8	Fxt / 2	12MHz
100b	Fpll / 6	Fxt / 1.5	16MHz
101b	Fpll / 4	Fxt / 1	24MHz
110b	Fpll / 3	Fxt / 0.75	32MHz
111b	Fpll / 2	Fxt / 0.5	Reserved, for custom chips only, to be used with bLDO_CORE_VOL=1

8.3 Clock Configuration

CH547 uses on-chip 24MHz clock by default after power-on. And select on-chip clock or external clock by CLOCK_CFG. XI pin may be used as P4.6 general-purpose I/O port when external crystal oscillator is disabled. Connect an oscillator between pins XI and XO when external crystal oscillator is enabled. In addition, connect a oscillating capacitor between XI and GND, XO and GND. When external clock is input directly, connect it to XI and keep XO suspended.

Source clock frequency: Fosc = bOSC_EN_INT ? 24MHz: Fxt

PLL frequency: Fpll = Fosc * 4

USB clock: Fusb4x = Fpll / 2

System clock frequency (Fsys) is obtained by divided Fpll, please refer to Table 8.2.2.

Default status after reset, Fosc=24MHz, Fpll=96MHz, Fusb4x=48MHz, and Fsys=12MHz.

Steps to switch to external crystal oscillator:

(1). Get into safe mode, SAFE_MOD = 55h; SAFE_MOD = AAh;

(2). Set bOSC_EN_XT in CLOCK_CFG to 1 with "OR" operation, other bits remain unchanged, to enable crystal oscillator;

(3). Delay several milliseconds, usually 5-10mS, to wait oscillator to work steadily;

(4). Get into safe mode again, SAFE_MOD = 55h; SAFE_MOD = AAh;

(5). Clear bOSC_EN_INT in CLOCK_CFG to 0 with "AND" operation, other bits remain unchanged, to switch to crystal oscillator;

(6). Get out of safe mode. Write any value into SAFE_MOD to get out of safe mode.

Steps to modify system frequency:

(1). Get into safe mode, SAFE_MOD = 55h; SAFE_MOD = AAh;

(2). Write new value to CLOCK_CFG;

(3). Get out of safe mode. Write any value into SAFE_MOD to get out of safe mode.

Notes:

(1). If the USB module is used, Fusb4x must be 48MHz. In addition, when the full speed USB is used, Fsys is not less than 6MHz. When the low-speed USB is used, Fsys is not less than 1.5MHz.

(2). Priority-use-of lower Fsys to reduce dynamic power dissipation and get wider Working temperature.

9. Interrupt

CH547 supports 16 interrupt sources, including 6 interrupts compatible with standard MCS51: INT0, T0, INT1, T1, UART0, T2, and 10 extended interrupts: SPI0, INT3, USB, ADC/UART2, UART1, PWMX/UART3, GPIO, WDOG, where the GPIO interrupt can be selected from 7 I/O pins.

Interrupt service programs are recommended to be as compact as possible, to avoid calling functions and subroutines as well as reading and writing xdata variables and code constants.

9.1 Register description

Table 9.1.1 List of interrupt vector

Interrupt	Entry address	Interrupt No.	Description	Default priority
INT_NO_INT0	0x0003	0	External interrupt 0	High priority ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ Low priority
INT_NO_TMR0	0x000B	1	Timer0 interrupt	
INT_NO_INT1	0x0013	2	External interrupt 1	
INT_NO_TMR1	0x001B	3	Timer1 interrupt	
INT_NO_UART0	0x0023	4	UART0 interrupt	
INT_NO_TMR2	0x002B	5	Timer2 interrupt	
INT_NO_SPI0	0x0033	6	SPI0 interrupt	
INT_NO_INT3	0x003B	7	External interrupt 3	
INT_NO_USB	0x0043	8	USB interrupt	
INT_NO_ADC INT_NO_UART2	0x004B	9	ADC interrupt (when bU2IE=0); UART2 interrupt (when bU2IE=1)	
INT_NO_UART1	0x0053	10	UART1 interrupt	
INT_NO_PWMX INT_NO_UART3	0x005B	11	PWMX interrupt (when bU3IE=0); UART3 interrupt (when bU3IE=1)	
INT_NO_GPIO	0x0063	12	GPIO Interrupt	
INT_NO_WDOG	0x006B	13	Watchdog timer interrupt	

Table 9.1.2 List of interrupt registers

Name	Address	Description	Reset value
IP_EX	E9h	Extended Interrupt Priority Control Register	00h
IE_EX	E8h	Extended Interrupt Enable Register	00h
GPIO_IE	CFh	GPIO Interrupt Enable Register	00h
IP	B8h	Interrupt Priority Control Register	00h
INTX	B3h	Extended External Interrupt Control Register	00h
IE	A8h	Interrupt Enable Register	00h

Interrupt Enable Register (IE):

Bit	Name	Access	Description	Reset value
7	EA	RW	Global interrupt enable 1:Interrupt is enabled when E_DIS is 0. 0:All interrupt requests are disabled.	0

6	E_DIS	RW	Global interrupt disable 1:All interrupt requests are disabled. 0:Interrupt is enabled when EA is 1. This bit is usually used to disable interrupt temporarily during flash-ROM operation.	0
5	ET2	RW	Timer2 interrupt enable 1:T2 interrupt is enabled. 0:T2 interrupt is disabled.	0
4	ES	RW	UART0 interrupt enable 1:UART0 interrupt is enabled. 0:UART0 interrupt is disabled.	0
3	ET1	RW	Timer1 interrupt enable 1:T1 interrupt is enabled. 0:T1 interrupt is disabled.	0
2	EX1	RW	External interrupt1 enable 1:INT1 interrupt is enabled. 0:INT1 interrupt is disabled.	0
1	ET0	RW	Timer0 interrupt enable 1:T0 interrupt is enabled. 0:T0 interrupt is disabled.	0
0	EX0	RW	External interrupt0 enable 1:INT0 interrupt is enabled. 0: INT0 interrupt is disabled.	0

Extended Interrupt Enable Register (IE_EX):

Bit	Name	Access	Description	Reset value
7	IE_WDOG	RW	Watchdog timer interrupt enable 1: WDOG interrupt is enabled. 0: WDOG interrupt is disabled.	0
6	IE_GPIO	RW	GPIO interrupt enable 1: GPIO interrupt is enabled. 0: GPIO interrupt is disabled.	0
5	IE_PWMX IE_UART3	RW	PWMX interrupt enable when bU3IE=0: 1: PWMX interrupt is enabled. 0: PWMX interrupt is disabled. UART3 interrupt enable when bU3IE=1: 1: UART3 interrupt is enabled. 0: UART3 interrupt is disabled.	0
4	IE_UART1	RW	UART1 interrupt enable 1: UART1 interrupt is enabled. 0: UART1 interrupt is disabled.	0
3	IE_ADC IE_UART2	RW	ADC interrupt enable when bU2IE=0: 1: ADC interrupt is enabled. 0: ADC interrupt is disabled.	0

			UART2 interrupt enable when bU2IE=1: 1: UART2 interrupt is enabled. 0: UART2 interrupt is disabled.	
2	IE_USB	RW	USB interrupt enable 1: USB interrupt is enabled. 0: USB interrupt is disabled.	0
1	IE_INT3	RW	External interrupt 3 enable 1: INT3 interrupt is enabled. 0: INT3 interrupt is disabled.	0
0	IE_SPI0	RW	SPI0 interrupt enable 1: SPI0 interrupt is enabled. 0: SPI0 interrupt is disabled.	0

GPIO Interrupt Enable Register (GPIO_IE):

Bit	Name	Access	Description	Reset value
7	bIE_IO_EDGE	RW	GPIO edge interrupt mode enable: 0: Level interrupt mode. bIO_INT_ACT=1 and interrupt will be requested constantly if there is a valid GPIO input level. Otherwise bIO_INT_ACT=0 and no interrupt request occurs with invalid GPIO input level. 1: Edge interrupt mode. There are interrupt flag bIO_INT_ACT and interrupt request with valid GPIO input edge, bIO_INT_ACT cannot be cleared by software, but it is automatically cleared when reset or interrupt program is running in level interrupt mode.	0
6	bIE_RXD1_LO	RW	1: UART1 RX pin interrupt is enabled (valid with low level in level mode or falling edge in edge mode). 0: UART1 RX pin interrupt is disabled. Select RXD1 or RXD1_ according to bUART1_PIN_X=0/1.	0
5	bIE_P1_5_LO	RW	1: P1.5 interrupt is enabled (valid with low level in level mode or falling edge in edge mode). 0: P1.5 interrupt is disabled.	0
4	bIE_P1_4_LO	RW	1: P1.4 interrupt is enabled (valid with low level in level mode or falling edge in edge mode). 0: P1.4 interrupt is disabled.	0
3	bIE_P0_3_LO	RW	1: P0.3 interrupt is enabled (valid with low level in level mode or falling edge in edge mode). 0: P0.3 interrupt is disabled.	0
2	bIE_P5_7_HI	RW	1: P5.7 interrupt is enabled (valid with high level in level mode or rising edge in edge mode). 0: P1.5 interrupt is disabled.	0
1	bIE_P4_6_LO	RW	1: P4.6 interrupt is enabled (valid with low level in level mode or falling edge in edge mode). 0: P4.6 interrupt is disabled.	0

0	bIE_RXD0_LO	RW	1: UART0 RX pin interrupt is enabled (valid with low level in level mode or falling edge in edge mode). 0: UART0 RX pin interrupt is disabled. Select RXD0 or RXD0_ based on bUART0_PIN_X=0/1.	0

Extended External Interrupt Register (INTX):

Bit	Name	Access	Description	Reset value
7	Reserved	RO	Reserved	0
6	Reserved	RO	Reserved	0
5	bIX3	RW	INT3 Input signal polarity 0: Default polarity (triggered by low level or falling edge). 1: Reverse polarity (triggered by high level or rising edge).	0
4	Reserved	RO	Reserved	0
3	bIE3	RW	INT3 interrupt request flag Auto reset after it enters interrupt.	0
2	bIT3	RW	INT3 trigger mode control 0: Triggered by low or high level. 1: Triggered by falling or rising edge.	0
1	Reserved	RO	Reserved	0
0	Reserved	RO	Reserved	0

Interrupt Priority Control Register (IP):

Bit	Name	Access	Description	Reset value
7	PH_FLAG	RO	High priority interrupt running flag	0
6	PL_FLAG	RO	Low priority interrupt running flag	0
5	PT2	RW	Timer2 interrupt priority control bit	0
4	PS	RW	UART0 interrupt priority control bit	0
3	PT1	RW	Timer1 interrupt priority control bit	0
2	PX1	RW	External interrupt 1 priority control bit	0
1	PT0	RW	Timer0 interrupt priority control bit	0
0	PX0	RW	External interrupt 0 priority control bit	0

Extended Interrupt Priority Control Register (IP_EX):

Bit	Name	Access	Description	Reset value
7	bIP_LEVEL	RO	Current interrupt nesting level flag bit 0: No interrupt or dual interrupt nesting. 1: Single interrupt nesting.	0
6	bIP_GPIO	RW	GPIO interrupt priority control bit	0
5	bIP_PWMX bIP_UART3	RW	PWMX interrupt priority control bit when bU3IE=0. UART3 interrupt priority control bit when bU3IE=1.	0
4	bIP_UART1	RW	UART1 interrupt priority control bit	0
3	bIP_ADC bIP_UART2	RW	ADC interrupt priority control bit when bU2IE=0. UART2 interrupt priority control bit when bU2IE=1.	0

2	bIP_USB	RW	USB interrupt priority control bit	0
1	bIP_INT3	RW	External interrupt 3 interrupt priority control bit	0
0	bIP_SPI0	RW	SPI0 interrupt priority control bit	0

The IP and IP_EX registers are used to set the interrupt priority. If a bit is set to 1, the corresponding interrupt source is set to a high priority; if a bit is cleared to 0, the corresponding interrupt source is set to a low priority. For interrupt sources of the same level, the system has a default priority order, and the default priority pole order is shown in Table 9.1.1. Where the combination of PH_FLAG and PL_FLAG indicates the priority of the current interrupt.

Table 9.1.3 Current interrupt priority status indication

PH_FLAG	PL_FLAG	Current interrupt priority status
0	0	No current interrupts
0	1	Currently executing a low priority interrupt
1	0	Currently executing a high priority interrupt
1	1	Unexpected status, unknown error

10. I/O Port

10.1 GPIO Introduction

The CH547 provides up to 44 I/O pins, some of which are multiplexed. Of these, the inputs and outputs of ports P0 to P4 are addressable by bit.

If the pins are not configured for multiplexing, they default to the general purpose I/O pin state. When used as general-purpose digital I/O, all I/O ports have true "read-modify-write" functionality and support bit manipulation commands such as SETB or CLR to independently change the direction of certain pins or port levels.

10.2 GPIO Register

All registers and bits in this section are generally expressed: "n" (n=0, 1, 2, 3, 4) to express the serial number of ports, and "x" (x=0, 1, 2, 3, 4, 5, 6, 7) to express the serial number of bits.

Table 10.2.1 List of GPIO Registers

Name	Address	Description	Reset value
P0	80h	P0 input/output register	FFh
P0_DIR_PU	C5h	P0 direction control and pull-up enable register	FFh
P0_MOD_OC	C4h	P0 output mode register	FFh
P1	90h	P1 input/output register	FFh
P1_DIR_PU	93h	P1 direction control and pull-up enable register	FFh
P1_MOD_OC	92h	P1 output mode register	FFh
P2	A0h	P2 input/output register	FFh
P2_DIR_PU	95h	P2 direction control and pull-up enable register	FFh
P2_MOD_OC	94h	P2 output mode register	FFh
P3	B0h	P3 input/output register	FFh
P3_DIR_PU	97h	P3 direction control and pull-up enable register	FFh
P3_MOD_OC	96h	P3 output mode register	FFh
P4	C0h	P4 input/output register	FFh
P4_DIR_PU	C3h	P4 direction control and pull-up enable register	FFh
P4_MOD_OC	C2h	P4 output mode register	FFh
P5	ABh	P5 input/output register	20h
PIN_FUNC	AAh	Pin function selection register	00h
XBUS_AUX	A2h	Bus auxiliary setting register	00h

Pn Input/Output Register (Pn):

Bit	Name	Access	Description	Reset value
[7:0]	Pn.0～Pn.7	RW	Pn.x pin state input and data output bits, support addressing by bit. *Notes: P4.7 is the internal bit, the write operation must be set to 1, and the read operation is meaningless.*	FFh

Pn Output Mode Register (Pn_MOD_OC):

Bit	Name	Access	Description	Reset value
[7:0]	Pn_MOD_OC	RW	Pn.x pin output mode setting: 0: Push-pull output;	FFh

			1: Open-drain output.	

Pn Direction Control and Pull-up Enable Register (Pn_DIR_PU):

Bit	Name	Access	Description	Reset value
[7:0]	Pn_DIR_PU	RW	Pn.x direction control in push-pull output mode: 0: Input. 1: Output. Pn.x pull-up resistor enable control in open-drain output mode: 0: Disable the pull-up resistor. 1: Enable the pull-up resistor;	FFh

Port Pn configuration is realized by Pn_MOD_OC[x] and Pn_DIR_PU[x], details as follows.

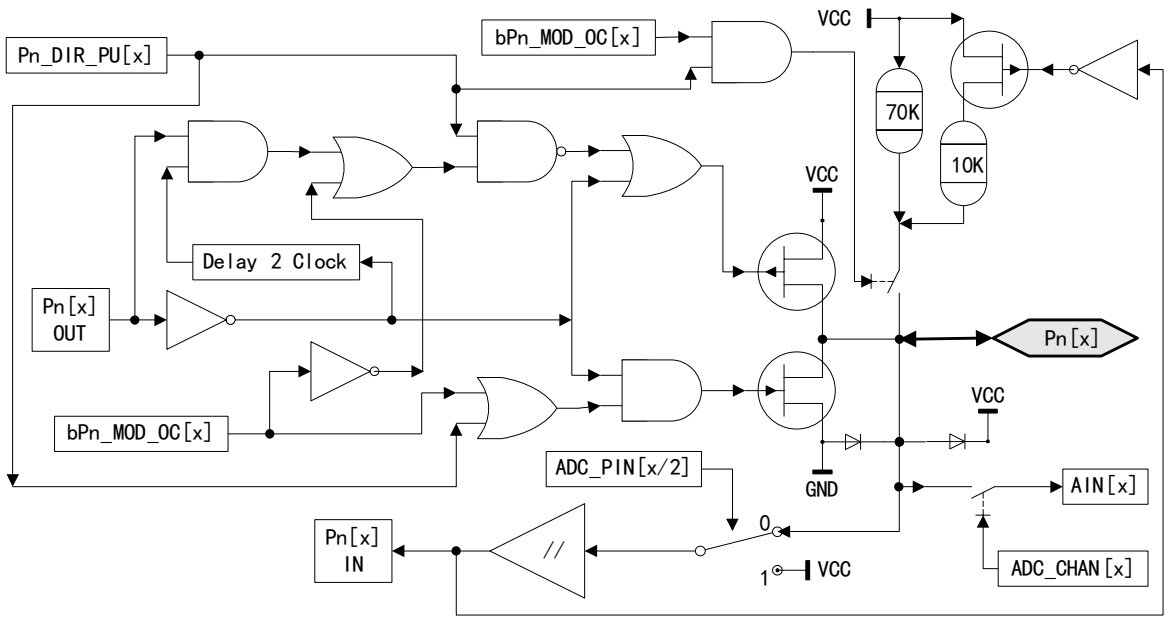
Table 10.2.2 Port configuration register combination

Pn_MOD_OC	Pn_DIR_PU	Working mode description
0	0	High impedance input mode, pins without pull-up resistor
0	1	Push-pull output mode with symmetry driving ability, a port can output or absorb large current in this mode
1	0	Open-drain output, support high impedance input, pins without pull-up resistor
1	1	Standard bi-direction mode (standard 8051), open-drain output, support input, pins with pull-up resistor. It will automatically generate 2 clock period of high level to accelerate conversion when output transfer from low level to high level

Ports P1-P4 support pure input, push-pull output and standard bi-direction modes. Each pin has a controllable internal pull-up resistor, and a protection diode attached to VDD and GND.

Figure 10.2.1 shows pins P0.x of port P0 and pins P1.x of port P1, also suitable for ports P2, P3 and P4 without AIN, ADC_PIN or ADC_CHAN.

Figure 10.2.1 Equivalent schematic diagram of I/O pins



P5 Input/Output Register (P5):

Bit	Name	Access	Description	Reset value
7	P5.7	R0	P5.7 pin state input bit	0
6	Reserved	RO	Reserved	0
5	P5.5	RW	P5.5 pin data output bit (open-drain output, support high voltage): 0: Output low level. 1: No output (high impedance, supports external pull-up resistor).	1
4	P5.4	RW	P5.4 pin data output bit: 0: Output low level. 1: Output high level.	0
3	Reserved	RO	Reserved	0
2	Reserved	RO	Reserved	0
1	P5.1	R0	P5.1 pin state input bit, built-in controllable pull-down resistor	0
0	P5.0	R0	P5.0 pin state input bit, built-in controllable pull-down resistor	0

10.3 GPIO Alternate Functions and Mapping

Some of the CH547 I/O pins are multiplexed and are all general purpose I/O pins by default after power-up. After enabling different function modules, the corresponding pins are configured as the corresponding function pins of the respective function modules.

Pin Function Selection Register (PIN_FUNC):

Bit	Name	Access	Description	Reset value
7	bPWM0_PIN_X	RW	PWM0 pin mapping enable 0: PWM0 enables P2.5. 1: PWM0 enables P1.5.	0

6	bIO_INT_ACT	R0	GPIO interrupt request activation state: When bIE_IO_EDGE=0, 1: GPIO with valid level and interrupt request. 0: GPIO with invalid level. When bIE_IO_EDGE=1, this bit is used as edge interrupt flag, 1: Valid edge is detected and this bit cannot be reset by software, but can only be reset automatically when reset or in level interrupt mode or when it enters corresponding interrupt service program.	0
5	bUART1_PIN_X	RW	UART1 pin mapping enable 0: RXD1/TXD1 enable P2.6/P2.7. 1: RXD1/TXD1 enable P1.6/P1.7.	0
4	bUART0_PIN_X	RW	UART0 pin mapping enable 0: RXD0/TXD0 enable P3.0/P3.1. 1: RXD0/TXD0 enable P0.2/P0.3.	0
3	Reserved	RO	Reserved	0
2	bINT0_PIN_X	RW	INT0 pin mapping enable 0: INT0 enables P3.2. 1: INT0 enables P2.2.	0
1	bT2EX_PIN_X	RW	T2EX/CAP2 pin mapping enable 0: T2EX/CAP2 enables P1.1. 1: T2EX/CAP2 enables P2.5.	0
0	bT2_PIN_X	RW	T2 pin mapping enable 0: T2 enables P1.0. 1: T2 enables P2.4.	0

Table 10.3.1 List of GPIO pins alternate functions

GPIO	Other functions: left-to-right priority
P0[0]	AIN8, P0.0
P0[1]	AIN9, P0.1
P0[2]	RXD_/bRXD_, AIN10, P0.2
P0[3]	TXD_/bTXD_, AIN11, P0.3
P0[4]	RXD2/bRXD2, P0.4
P0[5]	TXD2/bTXD2, P0.5
P0[6]	RXD3/bRXD3, P0.6
P0[7]	TXD3/bTXD3, P0.7
P1[0]	T2/bT2, AIN0, P1.0
P1[1]	T2EX/bT2EX, CAP2/bCAP2, AIN1, P1.1
P1[2]	AIN2, P1.2
P1[3]	AIN3, P1.3
P1[4]	SCS/bSCS, AIN4, P1.4
P1[5]	MOSI/bMOSI, PWM0_/bPWM0_, AIN5、P1.5
P1[6]	MISO/bMISO, RXD1_/bRXD1_, AIN6、P1.6

P1[7]	SCK/bSCK, TXD1_/bTXD1_, AIN7、P1.7
P2[0]	P2.0
P2[1]	P2.1
P2[2]	PWM3/bPWM3, INT0_/bINT0, P2.2
P2[3]	PWM2/bPWM2, P2.3
P2[4]	PWM1/bPWM1, T2_/bT2_, P2.4
P2[5]	PWM0/bPWM0, T2EX_/bT2EX_, CAP2_/bCAP2_, P2.5
P2[6]	RXD1/bRXD1, P2.6
P2[7]	TXD1/bTXD1, P2.7
P3[0]	RXD/bRXD, P3.0
P3[1]	TXD/bTXD, P3.1
P3[2]	INT0/bINT0, P3.2
P3[3]	INT1/bINT1, P3.3
P3[4]	T0/bT0, P3.4
P3[5]	T1/bT1, P3.5
P3[6]	P3.6
P3[7]	INT3/bINT3, P3.7
P4[0]	P4.0
P4[1]	P4.1
P4[2]	P4.2
P4[3]	P4.3
P4[4]	P4.4
P4[5]	P4.5
P4[6]	XI, P4.6
P5[0]	UDM/bUDM, P5.0
P5[1]	UDP/bUDP, P5.1
P5[4]	bALE/bCKO, P5.4
P5[5]	bHVOD, P5.5
P5[7]	RST/bRST, P5.7

The left-to-right priority shown in table above is the priority of some modules competing for using GPIO. For example, P1.6/P1.7 is set for UART1_, then P1.7 can still be used for SCK in higher priority if only RXD1_ is needed.

11. External Bus (xBUS)

CH547 does not provide bus signals for the external, does not support external bus, but the on-chip xRAM can be normally accessed.

External Bus Auxiliary Configuration Register (XBUS_AUX):

Bit	Name	Access	Description	Reset value
7	bUART0_TX	R0	UART0 Tx status 1: It is transmitting.	0
6	bUART0_RX	R0	UART0 Rx status 1: It is receiving.	0
5	bSAFE_MOD_ACT	R0	Safe mode status 1: It is in safe mode.	0
4	bALE_CLK_EN	RW	ALE pin clock output enable 1: Enable P5.4 output divided system frequency. 0: Clock signal is disabled.	0
3	bALE_CLK_SEL	RW	When bALE_CLK_EN=1, ALE pin clock frequency is selected; If the bit is 0, select 12 frequency division. If the bit is 1, select 4 frequency division	0
3	GF2	RW	General flag bit 2 when bALE_CLK_EN=0: User-defined. Can be reset and set by software.	0
2	bDPTR_AUTO_INC	RW	Enable DPTR add by 1 automatically after MOVX_@DPTR command.	0
1	Reserved	RO	Reserved	0
0	DPS	RW	Dual DPTR data pointer selection: 0: DPTR0. 1: DPTR1.	0

Table 11.1 P5.4 alternate ALE/CKO output status

P5[4]	bALE_CLK_EN	bALE_CLK_SEL	P5.4 pin function description
0	0	0	Output low level (default)
0	1	0	Fsys/12
0	1	1	Fsys/4
1	X	X	Output high level

12. Timer

12.1 Timer0/1

Timer0 and Timer1 are 16-bit timers/counters, which are configured by TCON and TMOD. TCON is used for T0 and T1 startup control and overflow interrupt as well as external interrupt control. Each timer is a 16-bit timing unit composed of 2 8-bit registers. High byte counter of Timer0 is TH0, and low byte is TL0. High byte counter of Timer1 is TH1, and low byte is TL1. Timer1 may also be used for UART0 baud rate generator.

Table 12.1.1 List of Timer0/1registers

Name	Address	Description	Reset value
TH1	8Dh	Timer1 count high byte	xxh
TH0	8Ch	Timer0 count high byte	xxh
TL1	8Bh	Timer1 count low byte	xxh
TL0	8Ah	Timer0 count low byte	xxh
TMOD	89h	Timer0/1 method register	00h
TCON	88h	Timer0/1 control register	00h

Timer/Counter 0/1 Control Register (TCON):

Bit	Name	Access	Description	Reset value
7	TF1	RW	Timer1 overflow interrupt flag Auto reset after it enters Timer1 interrupt service.	0
6	TR1	RW	Timer1 startup/stop bit Set 1 to start. Set and reset by software.	0
5	TF0	RW	Timer0 overflow interrupt flag Auto reset after it enters Timer0 interrupt.	0
4	TR0	RW	Timer0 startup/stop bit Set 1 to start. Set and reset by software.	0
3	IE1	RW	INT1 interrupt request flag Auto reset after it enters interrupt.	0
2	IT1	RW	INT1 trigger mode control 0: Low level action. 1: Falling edge action.	0
1	IE0	RW	INT0 interrupt request flag Auto reset after it enters interrupt.	0
0	IT0	RW	INT0 trigger mode control 0: Low level action. 1: Falling edge action.	0

Timer/Counter 0/1 Mode Register (TMOD):

Bit	Name	Access	Description	Reset value
7	bT1_GATE	RW	Gate enable bit control, whether Timer1 start is affected by the external interrupt signal INT1. 0: Timer1 will start or not independent of INT1; 1: It will only start if the INT1 pin is high and TR1 is 1.	0

6	bT1_CT	RW	Counter or timer mode selection for Timer1: 0: Timer, use internal clock. 1: Counter, use T1 pin falling edge as clock	0
5	bT1_M1	RW	Timer/Counter1 mode high bit	0
4	bT1_M0	RW	Timer/Counter1 mode low bit	0
3	bT0_GATE	RW	Gate enable bit control, whether Timer0 start is affected by the external interrupt signal INT0. 0: Timer0 will start or not independent of INT0; 1: It will only start if the INT0 pin is high and TR0 is 1.	0
2	bT0_CT	RW	Counter or timer mode selection for Timer0: 0: Timer, use internal clock. 1: Counter, use T0 pin falling edge as clock	0
1	bT0_M1	RW	Timer/Counter0 mode high bit	0
0	bT0_M0	RW	Timer/Counter0 mode low bit	0

Table 12.1.2 Timern operating mode selection for bTn_M1 and bTn_M0 (n=0, 1)

bTn_M1	bTn_M0	Timern operating mode (n=0、1)
0	0	Mode0: 13-bit timer or counter n by cascaded THn and lower 5 bits of TLn, the upper 3 bits of TLn are ignored. When the counts of all 13 bits change from 1 to 0, set the overflow flag TFn and reset the initial value.
0	1	Mode1: 16-bit timer or counter n by cascaded THn and TLn. When the counts of all 16 bits change from 1 to 0, set the overflow flag TFn and reset the initial value.
1	0	Mode2: 8-bit overload timer/counter n, TLn is used for count unit, and THn is used as the overload count unit. When the counts of all 8 bits change from 1 to 0, set the overflow flag TFn and automatically load the initial value from THn.
1	1	Mode3: For timer/counter 0, it is divided into TL0 and TH0. TL0 is used as an 8-bit timer/counter, occupying all control bits of Timer0. TH0 is also used as an 8-bit timer, occupying TR1, TF1 and interrupt resources of Timer1. In this case, Timer1 is still available, but the startup control bit TR1 and overflow flag bit TF1 cannot be used. For timer/counter 1, it stops after it enters mode3.

Timern count low byte (TLn) (n=0, 1):

Bit	Name	Access	Description	Reset value
[7:0]	TLn	RW	Timern count low byte	xxh

Timern count high byte (THn) (n=0, 1):

Bit	Name	Access	Description	Reset value
[7:0]	THn	RW	Timern count high byte	xxh

12.2 Timer2

Timer2 is a 16-bit auto-reload timer/counter, configured by T2CON and T2MOD. High byte if Timer2 is TH2, and low byte is TL2. Timer2 may be used as UART0 baud rate generator, and provide 3-channel level capture. The capture value is stored in the RCAP2 register.

Table 12.2.1 List of Timer2 registers

Name	Address	Description	Reset value
TH2	CDh	Timer2 counter high byte	00h
TL2	CCh	Timer2 counter low byte	00h
T2COUNT	CCh	16-bit SFR consists of TL2 and TH2	0000h
RCAP2H	CBh	Count reload/capture 2 data register high byte	00h
RCAP2L	CAh	Count reload/capture 2 data register low byte	00h
RCAP2	CAh	16-bit SFR consists of RCAP2L and RCAP2H	0000h
T2MOD	C9h	Timer2 method register	00h
T2CON	C8h	Timer2 control register	00h

Timer/Counter2 Control Register (T2CON):

Bit	Name	Access	Description	Reset value
7	TF2	RW	Timer2 overflow interrupt flag Set to 1 when the counts of all 16 bits of Timer2 change from 1 to 0. Reset by software. This bit will not be set when either RCLK=1 or TCLK=1.	0
6	EXF2	RW	Timer2 external trigger flag Set by T2EX edge trigger when EXEN2=1. Reset by software.	0
5	RCLK	RW	UART0 Rx clock selection 0: Timer1 overflow pulse. 1: Timer2 overflow pulse.	0
4	TCLK	RW	UART0 Tx clock selection 0: Timer1 overflow pulse. 1: Timer2 overflow pulse.	0
3	EXEN2	RW	T2EX trigger enable 0: Ignore T2EX. 1: Enable trigger reload or capture by T2EX edge.	0
2	TR2	RW	Timer2 startup/stop bit Set 1 to start. Set and reset by software.	0
1	C_T2	RW	Timer2 clock source selection 0: Internal clock. 1: Edge counter based on T2 falling edge.	0
0	CP_RL2	RW	Timer2 function select bit, if RCLK or TCLK is 1, this bit should be forced to 0. 0: Timer2 acts as a timer/counter and can automatically reload the count initial value when the counter overflows or the T2EX level changes; 1: Timer2's capture 2 function is enabled to capture the valid edge of T2EX.	0

Timer/Counter2 Method Register (T2MOD):

Bit	Name	Access	Description	Reset value

7	bTMR_CLK	RW	Fastest internal clock mode for T0/T1/T2 under faster clock mode: 0: Use divided clock. 1: Use original Fsys as clock without dividing. This bit has no effect on selecting standard clock timer		0
6	bT2_CLK	RW	Timer2 internal clock frequency selection bit, this bit is 0 to select standard clock, timing/counting mode is Fsys/12, UART0 clock mode is Fsys/4; this bit is 1 to select fast clock, timing/counting mode is Fsys/4 (bTMR_CLK=0) or Fsys (bTMR_CLK=1), UART0 clock mode is Fsys/2 (bTMR_CLK=0) or Fsys (bTMR_CLK=1)		0
5	bT1_CLK	RW	Timer1 internal clock frequency selection: 0 = Standard clock, Fsys/12. 1 = Faster clock, Fsys/4 if bTMR_CLK = 0, or Fsys if bTMR_CLK = 1.		0
4	bT0_CLK	RW	Timer0 internal clock frequency selection: 0 = Standard clock, Fsys/12. 1 = Faster clock, Fsys/4 if bTMR_CLK = 0, or Fsys if bTMR_CLK = 1.		0
3	bT2_CAP_M1	RW	Timer2 capture mode high bit	Capture mode selection: X0: from falling ege to falling edge. 01: from any edge to any edge (level change). 11: from rising edge to rising edge.	0
2	bT2_CAP_M0	RW	Timer2 capture mode low bit		0
1	T2OE	RW	Timer2 clock output enable 0: Disable output. 1: Enable clock output at T2 pin, frequency = TF2/2.		0
0	Reserved	RO	Reserved		0

Count Reload/Capture 2 Data Register (RCAP2):

Bit	Name	Access	Description	Reset value
[7:0]	RCAP2H	RW	High byte of reload value in timer/counter mode. High byte of timer captured by CAP2 in capture mode.	00h
[7:0]	RCAP2L	RW	Low byte of reload value in timer/counter mode. Low byte of timer captured by CAP2 in capture mode	00h

Timer2 Counter (T2COUNT):

Bit	Name	Access	Description	Reset value
[7:0]	TH2	RW	Counter high byte	00h
[7:0]	TL2	RW	Counter low byte	00h

12.3 PWM Register

The PWM_DATA register in this section is represented in a generic format: "n" (n=0-3) to represent the serial number of ports.

Table 12.3.1 List of PWMX registers

Name	Address	Description	Reset value
PWM_CK_SE	9Eh	PWM clock divisor setting register	00h
PWM_CTRL	9Dh	PWM control register	02h
PWM_CTRL2	9Fh	PWM extended control register	00h
PWM_DATA0	9Ch	PWM0 data register	xxh
PWM_DATA1	9Bh	PWM1 data register	xxh
PWM_DATA2	9Ah	PWM2 data register	xxh
PWM_DATA3	A3h	PWM3 data register	xxh

PWMn Data Register (PWM_DATAn):

Bit	Name	Access	Description	Reset value
[7:0]	PWM_DATAn	RW	Store the current data of PWMn. Duty cycle of PWMn output active level = PWM_DATAn/PWM_CYCLE	xxh

PWM Control Register (PWM_CTRL):

Bit	Name	Access	Description	Reset value
7	Reserved	RO	Reserved	0
6	bPWM1_POLAR	RW	PWM1 output polarity control 0: Default low and active high. 1: Default high and active low.	0
5	bPWM0_POLAR	RW	PWM0 output polarity control 0: Default low and active high. 1: Default high and active low.	0
4	bPWM_IF_END	RW	PWM cycle end interrupt flag 1: There is a PWM cycle end interrupt. Write 1 to reset, or reload PWM_DATA0 data to reset.	0
3	bPWM1_OUT_EN	RW	PWM1 output enable 1: Enable PWM1 output.	0
2	bPWM0_OUT_EN	RW	PWM0 output enable 1: Enable PWM0 output.	0
1	bPWM_CLR_ALL	RW	1: Clear PWM count and FIFO. Reset by software.	1
0	bPWM_MOD_6BIT	RW	PWM data width mode: 0: 8-bit data, and PWM cycle is 256. 1: 6-bit data, and PWM cycle is 64.	0

PWM Extended Control Register (PWM_CTRL2):

Bit	Name	Access	Description	Reset value
7	Reserved	RO	Reserved	0
6	Reserved	RO	Reserved	0
5	Reserved	RO	Reserved	0
4	Reserved	RO	Reserved	0

3	Reserved	RO	Reserved	0
2	Reserved	RO	Reserved	0
1	bPWM3_OUT_EN	RW	PWM3 output enable 1: Enable PWM3 output.	0
0	bPWM2_OUT_EN	RW	PWM2 output enable 1: Enable PWM2 output.	0

PWM Clock Divisor Setting Register (PWM_CK_SE):

Bit	Name	Access	Description	Reset value
[7:0]	PWM_CK_SE	RW	Set PWM clock frequency division factor	00h

12.4 PWM Function

The CH547 provides 4 PWMs, the CH546 only provides the first 2 PWMs (PWM0 and PWM1). The PWM output duty cycle can be dynamically modified to obtain various output voltages by integrating low-pass filtering with simple RC resistors and capacitors, equivalent to a low-speed digital-to-analogue converter DAC.

PWM_CYCLE = bPWM_MOD_6BIT ? 64 : 256

PWMn output duty cycle = PWM_DATAn / PWM_CYCLE

The range of 0% to 99.6% duty cycle is supported in 8-bit data mode and 0% to 100% duty cycle in 6-bit data mode (if PWM_DATAn is greater than PWM_CYCLE then it is treated as 100%).

12.5 Timer

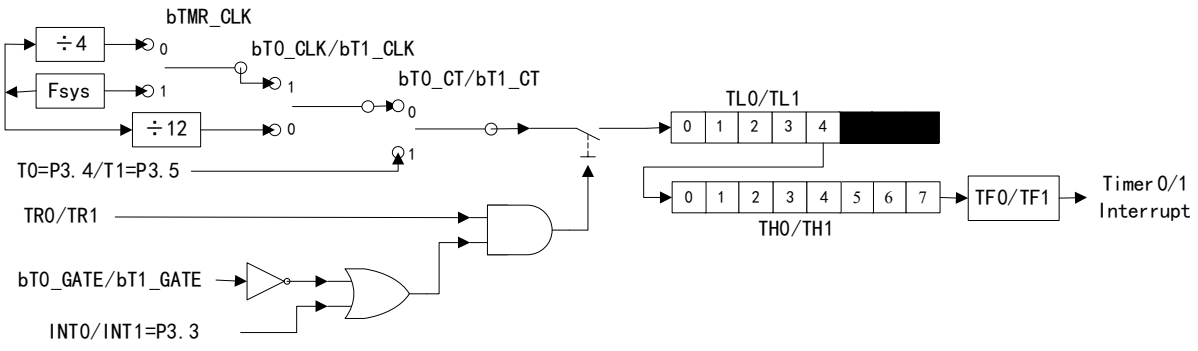
12.5.1 Timer0/1

(1). Set T2MOD to select Timer internal clock frequency. Timer0/1 frequency is Fsys/12 when bTn_CLK(n=0/1) is 0; If bTn_CLK is 1, then Fsys/4 or Fsys is selected as the clock by bTMR_CLK=0 or 1.

(2). Set TMOD to configure Timer working mode.

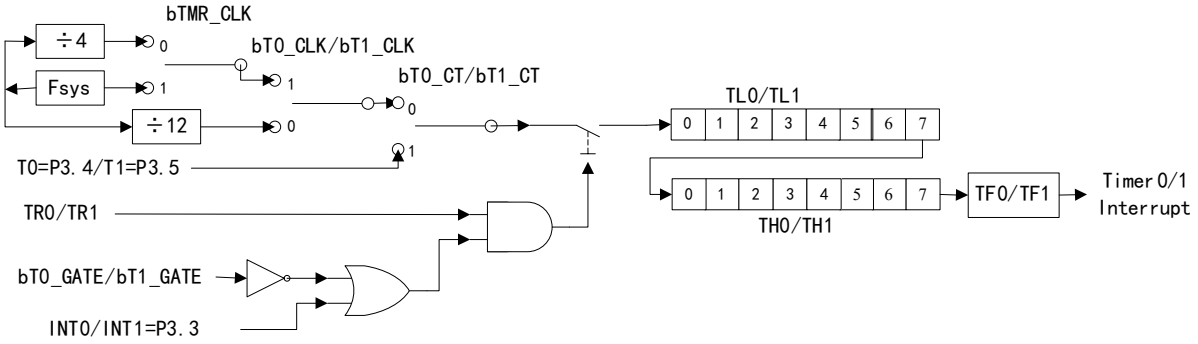
Mode0: 13-bit timer/counter

Figure 12.5.1.1 Timer0/1 mode0



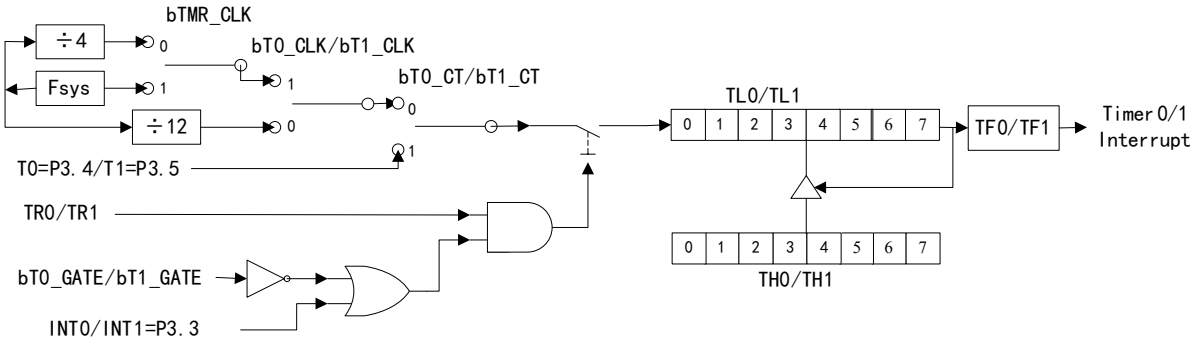
Mode1: 16-bit timer/counter

Figure 12.5.1.2 Timer0/1 mode1



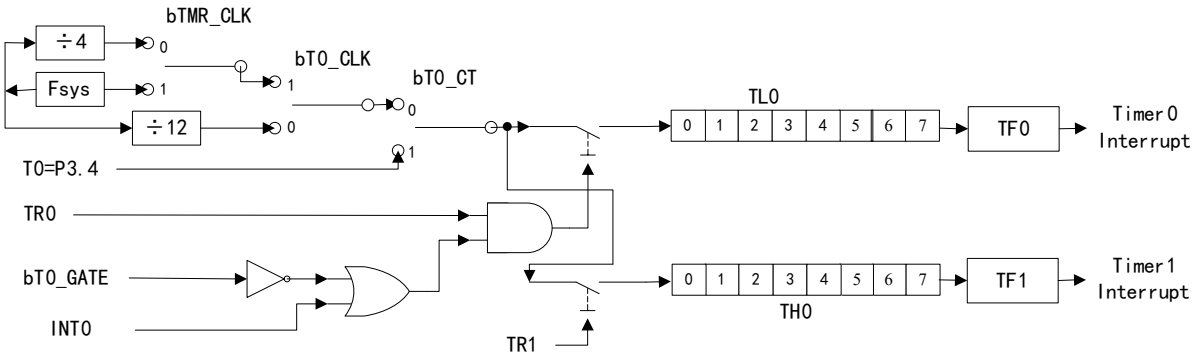
Mode2: Auto-reload 8-bit timer/counter

Figure 12.5.1.3 Timer0/1 mode2



Mode3: Timer0 is divided into 2 separate 8-bit timer/counter, and borrowed TR1 of Timer1. Timer1 substitutes the borrowed TR1 control bit by whether starting mode3. Timer1 stops when it gets into mode3.

Figure 12.5.1.4 Timer0 mode3



(3). Set timer/counter initial value TLn and THn (n=0/1).

(4). Set TRn (n=0/1) in TCON to enable or disable timer/counter, and check through TFn(n=0/1) or interrupt mode.

12.5.2 Timer2

Timer2 16-bit reload timer/counter mode:

(1). Clear RCLK and TCLK in T2CON to 0, to select non-baud rate generator mode.

(2). Clear C_T2 in T2CON to 0, to use internal clock, and jump to step (3). Or set it to 1 to select T2 falling edge as the count clock and skip step (3).

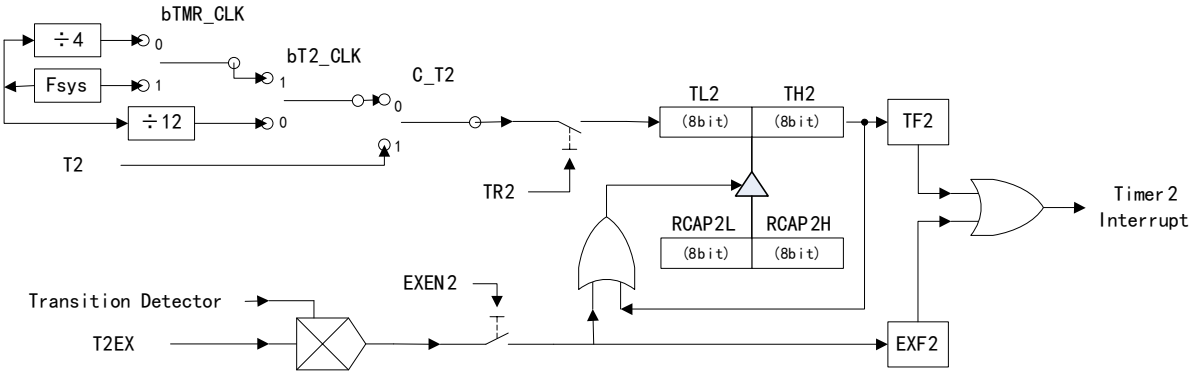
(3). Set T2MOD to select Timer internal clock. Timer2 frequency is Fsys/12 when bT2_CLK=0, Fsys/4 when bTMR_CLK=0 and Fsys when bTMR_CLK=1 if bT2_CLK=1.

(4). Clear CP_RL2 in T2CON to 0, to select Timer216-bit reload timer/counter function.

(5). Set RCAP2L and RCAP2H as reload value when timer overflows, set TL2 and TH2 as initial value (generally the same as RCAP2L and RCAP2H), set TR2 to 1 and enable Timer2.

(6). Read TF2 or Timer2 interrupt to get current timer/counter status.

Fig.12.5.2.1 Timer2 16-bit reload timer/counter



Timer2 clock output mode:

Refer to 16-bit reload timer/counter mode, set T2OE in T2MOD to 1 to enable pin T2 output clock of half TF2 frequency.

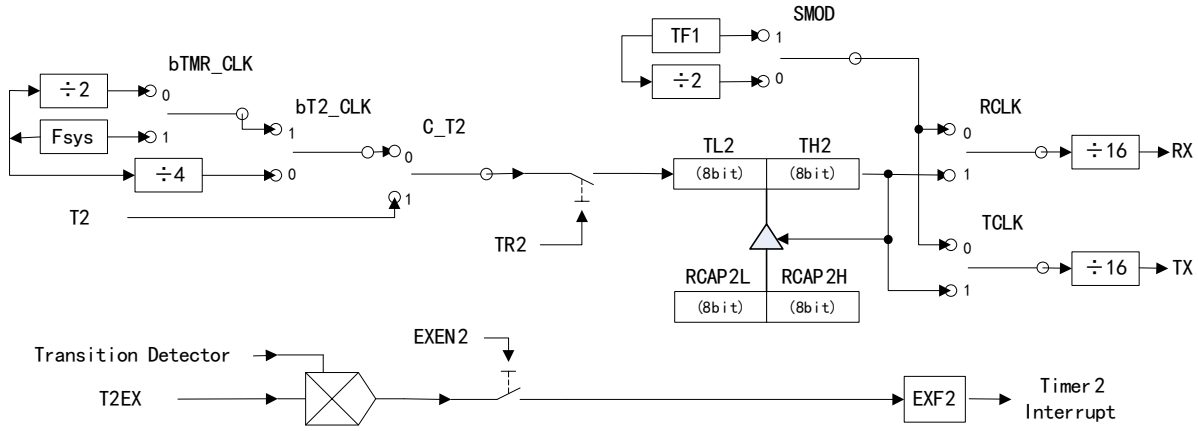
Timer2 UART0 baud rate generator mode:

(1). Clear C_T2 in T2CON to 0, to select internal clock. Or set it to 1 to select T2 falling edge as clock, set RCLK and TCLK in T2CON to 1 or set one of them to 1 as required, to select UART baud rate generator mode.

(2). Set T2MOD to select Timer internal clock frequency. Timer2 frequency is Fsys/4 if bT2_CLK is 0, Fsys/2 when bTMR_CLK=0 or Fsys when bTMR_CLK=1 if bT2_CLK=1.

(3). Set RCAP2L and RCAP2H as reload value after timer overflows, set TR2 to 1 and enable Timer2.

Figure 12.5.2.2 Timer2 UART0 baud rate generator



Timer2 signal channel capture mode:

(1). Clear RCLK and TCLK in T2CON to 0, to select non-baud rate generator mode.

(2). Clear C_T2 in T2CON to 0 to select internal clock, and jump to step (3). Or set it to 1 to select T2 falling edge as the count clock and skip step (3).

(3). Set T2MOD to select Timer internal clock frequency. Timer2 clock is Fsys/12 if bT2_CLK=0, Fsys/4 when bTMR_CLK=0 or Fsys when bTMR_CLK=1 if bT2_CLK=1.

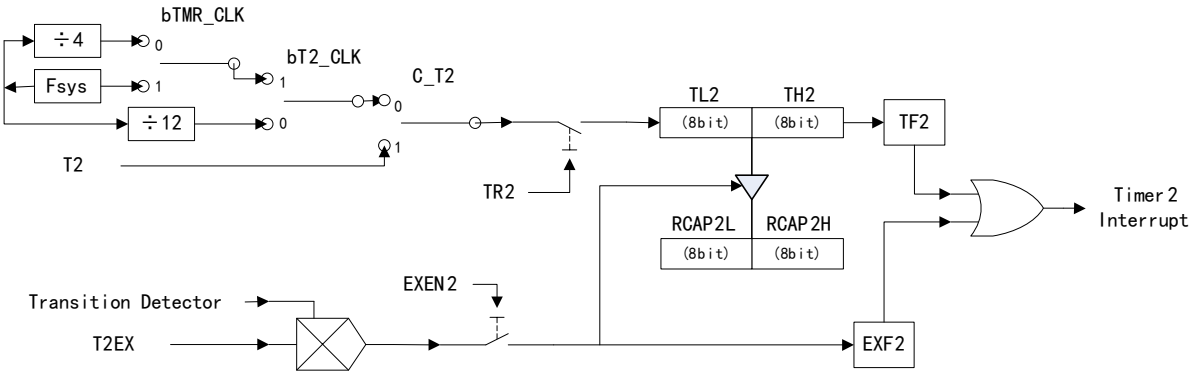
(4). Set bT2_CAP_M1 and bT2_CAP_M0 in T2MOD, to select corresponding edge capture mode.

(5). Set CP_RL2 in T2CON to 1, to select T2EX pin capture function of Timer2.

(6). Set TL2 and TH2 as initial value of the timer, and set TR2 to 1 to enable Timer2.

(7). At the end of CAP2 capture, RCAP2L and RCAP2H keep TL2 and TH2 value, set EXF2 to trigger interrupt. The signal width of 2 valid edges is the difference between last time capturing of RCAP2L / RCAP2H and next.

Figure 12.5.2.3 Timer2 capture mode



13. Universal Asynchronous Receiver Transmitter (UART)

13.1 UART Introduction

The CH547 chip provides four full duplex asynchronous serial ports: UART0 to UART3. The CH546 provides only UART0.

UART0 is a standard MCS51 serial port whose data reception and transmission is achieved by accessing physically separate receive/transmit registers via SBUF. Data written to SBUF is loaded into the transmit register, and read operations to SBUF correspond to the receive buffer register.

UART1 is a simplified MCS51 serial port whose data reception and transmission is achieved by SBUF1 accessing physically separate receive/transmit registers. The data written to SBUF1 is loaded into the transmit register, while the read operation to SBUF1 corresponds to the receive buffer register. uart1 has a separate baud rate generator compared to UART0, which removes the multi-computer communication mode and fixed baud rate.

UART2 is based on UART1 with an interrupt enable bit added to replace the ADC interrupt.

UART3 is the same as UART2, also based on UART1, with an additional interrupt enable bit to replace the PWMX interrupt.

13.2 UART Register

Table 13.2.1 List of UART registers

Name	Address	Description	Reset value
SBUF	99h	UART0 data register	xxh
SCON	98h	UART0 control register	00h
SCON1	BCh	UART1 control register	40h
SBUF1	BDh	UART1 data register	xxh
SBAUD1	BEh	UART1 baud rate setting register	xxh
SIF1	BFh	UART1 interrupt status register	00h
SCON2	B4h	UART2 control register	00h
SBUF2	B5h	UART2 data register	xxh
SBAUD2	B6h	UART2 baud rate setting register	xxh
SIF2	B7h	UART2 interrupt status register	00h
SCON3	ACh	UART3 control register	00h
SBUF3	ADh	UART3 data register	xxh
SBAUD3	AEh	UART3 baud rate setting register	xxh
SIF3	AFh	UART3 interrupt status register	00h

13.2.1 UART0 Register Description

UART0 control register (SCON):

Bit	Name	Access	Description	Reset value
7	SM0	RW	UART0 mode bit0, data bit selection: 0: 8-bit data. 1: 9-bit data.	0
6	SM1	RW	UART0 mode bit1, baud rate selection: 0: Fixed. 1: Variable, generated by T1 or T2.	0
5	SM2	RW	UART0 Multi-machine communication control bit:	0

			When receiving data in modes 2 and 3, when SM2=1, if RB8 is 0, then RI is not set to 1 and reception is invalid; if RB8 is 1, then RI is set to 1 and reception is valid; when SM2=0, RI is set when receiving data and reception is valid, regardless of whether RB8 is 0 or 1; In mode 1, if SM2=1, then reception is only valid if a valid stop bit is received; In mode 0, the SM2 bit must be set to 0.	
4	REN	RW	UART0 receive enable 0: Disable. 1: Enable.	0
3	TB8	RW	Bit 9 of the sent data, in modes 2 and 3, TB8 is used to write bit 9 of the sent data, which can be a parity bit; in multi-machine communication, it is used to indicate whether the host is sending an address byte or a data byte, TB8=0 for data, TB8=1 for address.	0
2	RB8	RW	Bit 9 of the received data, in modes 2 and 3, RB8 is used to store bit 9 of the received data; in mode 1, if SM2=0, then RB8 is used to store the received stop bit; in mode 0, RB8 is not used.	0
1	TI	RW	Transmit interrupt flag bit, set by hardware after a data byte has been transmitted and needs to be cleared by software.	0
0	RI	RW	Receive interrupt flag bit, set by hardware after a data byte is received, needs to be cleared by software.	0

Table 13.2.1.1 UART0 working mode

SM0	SM1	Description
0	0	Mode 0, shift register method, baud rate fixed at Fsys/12
0	1	Mode 1, 8-bit asynchronous communication method, variable baud rate, generated by timer T1 or T2
1	0	Mode 2, 9-bit asynchronous communication method, baud rate is Fsys/128 (SMOD=0) or Fsys/32 (SMOD=1)
1	1	Mode 3, 9-bit asynchronous communication method, variable baud rate, generated by timer T1 or T2

In mode1 and mode3, UART0 baud rate is generated by T1 when RCLK=0 and TCLK=0. Set T1 in mode2 auto reload 8-bit timer, clear bT1_CT and bT1_GATE, as follow:

Table 13.2.1.2 Calculation formula of UART0 baud rate

bTMR_CLK	bT1_CLK	SMOD	Description
1	1	0	TH1 = 256 - Fsys / 32 / baud rate
1	1	1	TH1 = 256 - Fsys / 16 / baud rate
0	1	0	TH1 = 256 - Fsys / 4 / 32 / baud rate
0	1	1	TH1 = 256 - Fsys / 4 / 16 / baud rate
X	0	0	TH1 = 256 - Fsys / 12 / 32 / baud rate
X	0	1	TH1 = 256 - Fsys / 12 / 16 / baud rate

In mode1 and3, UART0 baud rate is generated by T2 when RCLK=1 and TCLK=1. Set T2 in mode2 auto-reload 16-bit timer, clear C_T2 and CP_RL2, as follow:

Table 13.2.1.3 Calculation formula of UART0 baud rate

bTMR_CLK	bT2_CLK	Description
1	1	RCAP2 = 65536 - Fsys / 16 / baud rate
0	1	RCAP2 = 65536 - Fsys / 2 / 16 / baud rate
X	0	RCAP2 = 65536 - Fsys / 4 / 16 / baud rate

UART0 Data Register (SBUF):

Bit	Name	Access	Description	Reset value
[7:0]	SBUF	RW	UART0 data register, including physically separated transmit register and receive register. The transmit register is used to write data to SBUF. The receive register is used to read data from SBUF.	xxh

13.2.2 UART1 Register Description

UART1 Control Register (SCON1):

Bit	Name	Access	Description	Reset value
7	bU1SM0	RW	UART1 working method selection 0: 8-bit data. 1: 9-bit data.	0
6	Reserved	RO	Reserved	1
5	bU1SMOD	RW	UART1 baud rate selection: 0: Slow mode. 1: Fast mode.	0
4	bU1REN	RW	UART1 receive enable 0: Disable. 1: Enable.	0
3	bU1TB8	RW	The 9th transmitted data bit, can be a parity bit in 9-bit data mode. In 8-bit data mode, TB8 is ignored.	0
2	bU1RB8	RW	The 9th received data bit. In 9-bit data mode, RB8 is used to store the 9th bit of the received data. In 8-bit data mode, RB8 is used to store the received stop bit.	0
1	bU1TIS	WO	Write 1, and the transmit interrupt flag bit will be preset to 1, and the read value is always 0.	0
0	bU1RIS	WO	Write 1, and the receive interrupt flag bit will be preset to 1, and the read value is always 0.	0

UART1 baud rate is generated by SBAUD1, and can be divided into two cases according to bU1SMOD:
When bU1SMOD=0, SBAUD1 = 256 - Fsys / 32 / baud rate.
When bU1SMOD=1, SBAUD1 = 256 - Fsys / 16 / baud rate.

UART1 Interrupt Status Register (SIF1):

Bit	Name	Access	Description	Reset value
[7:2]	Reserved	RO	Reserved	000000b
1	bU1TI	RW	Transmit interrupt flag bit, set by hardware after a byte is transmitted. Write 1 to reset by software (writing 0 to this bit will be ignored)	0
0	bU1RI	RW	Receive interrupt flag bit, set by hardware after a byte is received effectively. Write 1 to reset by software (writing 0 to this bit will be ignored)	0

Note: Writing a 1 to the interrupt flag bit to clear it ensures that only the specified flag bit is cleared and does not affect other interrupt flags under the same register (other interrupt flags may already be 1 before this write operation, or may become 1 during this write operation). Same as below.

UART1 Data Register (SBUF1):

Bit	Name	Access	Description	Reset value
[7:0]	SBUF1	RW	UART1 data register, including physically separated transmit register and receive register. The transmit register is used to write data to SBUF1. The receive register is used to read data from SBUF1.	xxh

13.2.3 UART2 Register Description

UART2 Control Register (SCON2):

Bit	Name	Access	Description	Reset value
7	bU2SM0	RW	UART2 working mode selection 0: 8-bit data. 1: 9-bit data.	0
6	bU2IE	RW	UART2 interrupt enable 0: UART2 request interrupt disabled, and the interrupt flag can be inquired. 1: UART2 interrupt enabled, and the original ADC interrupt is disabled for replacement.	0
5	bU2SMOD	RW	UART2 baud rate selection: 0: Slow mode. 1: Fast mode.	0
4	bU2REN	RW	UART2 receive enable 0: Disable. 1: Enable.	0
3	bU2TB8	RW	The 9th transmitted data bit. In 9-bit data mode, TB8 is used to write the 9th transmitted data bit, which can be a parity bit. In 8-bit data mode, TB8 is ignored.	0
2	bU2RB8	RW	The 9th received data bit. In 9-bit data mode, RB8 is used to store the 9th received data bit. In 8-bit data mode, RB8 is used to store the received stop bit.	0
1	bU2TIS	WO	Write 1, and the transmit interrupt flag bit will be preset to 1, and the	0

			read value is always 0.	
0	bU2RIS	WO	Write 1, and the receive interrupt flag bit will be preset to 1, and the read value is always 0.	0

UART2 baud rate is generated by SBAUD2, and it can be divided into 2 cases according to bU2SMOD:
When bU2SMOD=0, SBAUD2 = 256 - Fsys / 32 / baud rate.
When bU2SMOD=1, SBAUD2 = 256 - Fsys / 16 / baud rate.

UART2 Interrupt Status Register (SIF2):

Bit	Name	Access	Description	Reset value
[7:2]	Reserved	RO	Reserved	000000b
1	bU2TI	RW	Transmit interrupt flag bit, set by hardware after a byte is transmitted. Write 1 to reset by software (writing 0 to this bit will be ignored).	0
0	bU2RI	RW	Receive interrupt flag bit, set by hardware after a byte is received effectively. Write 1 to reset by software (writing 0 to this bit will be ignored).	0

UART2 Data Register (SBUF2):

Bit	Name	Access	Description	Reset value
[7:0]	SBUF2	RW	UART2 data register, including physically separated transmit register and receive register. The transmit register is used to write data to SBUF2. The receive register is used to read data from SBUF2.	xxh

13.2.4 UART3 Register Description

UART3 Control Register (SCON3):

Bit	Name	Access	Description	Reset value
7	bU3SM0	RW	UART3 working mode selection 0: 8-bit data. 1: 9-bit data.	0
6	bU3IE	RW	UART3 interrupt enable 0: UART3 request interrupt disabled, and the interrupt flag can be inquired. 1: UART3 interrupt enabled, and the original PWMX interrupt is disabled for replacement.	0
5	bU3SMOD	RW	UART3baud rate selection 0: Slow mode. 1: Fast mode.	0
4	bU3REN	RW	UART3 receive enable 0: Disable. 1: Enable.	0
3	bU3TB8	RW	The 9th transmitted data bit. In 9-bit data mode, TB8 is used to write	0

			the 9th transmitted data bit, which can be a parity bit. In 8-bit data mode, TB8 is ignored.	
2	bU3RB8	RW	The 9th received data bit. In 9-bit data mode, RB8 is used to store the 9th received data bit. In 8-bit data mode, RB8 is used to store the received stop bit.	0
1	bU3TIS	WO	Write 1, the transmit interrupt flag bit will be preset to 1, and the read value is always 0.	0
0	bU3RIS	WO	Write 1, the receive interrupt flag bit will be preset to 1, and the read value is always 0.	0

UART3 baud rate is generated by SBAUD3, and it can be divided into 2 cases according to bU3SMOD:
When bU3SMOD=0, SBAUD3 = 256 - Fsys / 32 / baud rate;
When bU3SMOD=1, SBAUD3 = 256 - Fsys / 16 / baud rate.

UART3 Interrupt Status Register (SIF3):

Bit	Name	Access	Description	Reset value
[7:2]	Reserved	RO	Reserved	000000b
1	bU3TI	RW	Transmit interrupt flag bit, set by hardware after a byte is transmitted. Write 1 to reset by software (writing 0 to this bit will be ignored).	0
0	bU3RI	RW	Receive interrupt flag bit, set by hardware after a byte is received effectively. Write 1 to reset by software (writing 0 to this bit will be ignored).	0

UART3 Data Register (SBUF3):

Bit	Name	Access	Description	Reset value
[7:0]	SBUF3	RW	UART3 data register, including physically separated transmit register and receive register. The transmit register is used to write data to SBUF3. The receive register is used to read data from SBUF3.	xxh

13.3 UART Application

UART0 application:
(1). Select UART0 baud rate generator from T1 or T2, and set counter.
(2). Enable T1 or T2.
(3). Set SM0, SM1, SM2 in SCON to select UART0 working mode. Set REN to 1 and enable UART0 receiver.
(4). Set UART interrupt or query R1 and T1 interrupt status.
(5). Read/write SBUF to receive/transmit data, and the allowed receive baud rate error should be not more than 2%.

UART1 application:
(1). Select bU1SMOD and set SBAUD1 based on the baud rate.
(2). Set bU1SM0 in SCON1 to select UART1 working mode. Set bU1REN to 1 and enable UART1 receiver.
(3). Set UART1 interrupt or query bU1RI and bU1TI interrupt status (only write 1 to the specified bit to reset).

(4). Read/write to SBUF1 to receive/transmit data, and the allowed baud rate error should be not more than 2%.

UART2 application (UART3 application):

(1). Select bU2SMOD and set SBAUD2 based on the baud rate.

(2). Set bU2SM0 in SCON2 to select UART2 working mode. Set bU2REN to 1 and enable UART2 receiver.

(3). Query bU2RI and bU2TI interrupt status (write 1 to the specified bit to reset), or enable UART2 interrupt and set bU2IE to 1 to replace ADC (PWMX for UART3) interrupt.

(4). Read/write to SBUF2 to receive/transmit data, and the allowed baud rate error should be not more than 2%.

14. Synchronous Serial Interface (SPI)

14.1 SPI Introduction

CH547 provides one SPI interface for high-speed synchronous data transfer between peripheral devices.

(1). Support master mode and slave mode;

(2). Support mode0 and mode3 clock mode;

(3). Optional 3-wire full-duplex mode or 2-wire half-duplex mode;

(4). Optional MSB first or LSB first;

(5). Clock frequency is variable, up to half of the system clock frequency;

(6). Built-in 1-byte receiver FIFO and 1-byte transmitter FIFO;

(7). Support the first byte pre-load data in slave mode to facilitate the host to obtain the returned data immediately in the first byte.

14.2 SPI Register

Table 14.2.1 List of SPI registers

Name	Address	Description	Reset value
SPI0_SETUP	FCh	SPI0 setup register	00h
SPI0_S_PRE	FBh	SPI0 slave mode preset data register	20h
SPI0_CK_SE	FBh	SPI0 clock divisor setting register	20h
SPI0_CTRL	FAh	SPI0 control register	02h
SPI0_DATA	F9h	SPI0 data register	xxh
SPI0_STAT	F8h	SPI0 status register	08h

SPI0 setup register (SPI0_SETUP):

Bit	Name	Access	Description	Reset value
7	bS0_MODE_SLV	RW	SPI0 master/slave mode selection 0: Master mode. 1: Slave mode/device mode.	0
6	bS0_IE_FIFO_OV	RW	FIFO overflow interrupt enable in slave mode 1: FIFO overflow interrupt is enabled. 0: FIFO overflow will not result in interrupt.	0
5	bS0_IE_FIRST	RW	The first receive byte interrupt in slave mode enable: 1: The first receive byte will trigger interrupt in slave mode. 0: The first receive byte will not trigger interrupt.	0
4	bS0_IE_BYTE	RW	Data byte transfer completion interrupt enable: 1: Byte transfer completion interrupt is enabled. 0: Byte transfer completion interrupt will not result in interrupt.	0
3	bS0_BIT_ORDER	RW	Data byte bit order control: 0: MSB in first. 1: LSB in first.	0
2	Reserved	RO	Reserved	0

1	bS0_SLV_SELT	R0	CS activation status in slave mode: 0: Not selected at present. 1: Selected at present.	0
0	bS0_SLV_PRELOAD	R0	Preload data state in slave mode 1: It is in preload state before data transmission while CS is valid	0

SPI0 clock divisor setting register (SPI0_CK_SE):

Bit	Name	Access	Description	Reset value
[7:0]	SPI0_CK_SE	RW	SPI0 clock divisor setting in master mode	20h

SPI0 slave mode preset data register (SPI0_S_PRE)

Bit	Name	Access	Description	Reset value
[7:0]	SPI0_S_PRE	RW	Pre-load first transfer data in slave mode	20h

SPI0 control register (SPI0_CTRL):

Bit	Name	Access	Description	Reset value
7	bS0_MISO_OE	RW	SPI0 MISO output enable: 1: Enable output. 0: Disable output.	0
6	bS0_MOSI_OE	RW	SPI0 MOSI output enable: 1: Enable output. 0: Disable output.	0
5	bS0_SCK_OE	RW	SPI0 SCK output enable: 1: Enable output. 0: Disable output.	0
4	bS0_DATA_DIR	RW	SPI0 data direction: 0: Output data, only regard FIFO writing as valid operation, start a SPI transmission. 1: Input data, reading or writing FIFO are all valid, start a SPI transmission.	0
3	bS0_MST_CLK	RW	SPI0 master clock mode: 0: Mode0, default low level when SCK is free. 1: Mode3, SCK default high level.	0
2	bS0_2_WIRE	RW	SPI0 2-wire half duplex mode enable: 0: 3-wire full-duplex mode, including SCK, MOSI, and MISO. 1: 2-wire half-duplex mode, including SCK, MISO.	0
1	bS0_CLR_ALL	RW	1: Clear SPI0 interrupt flag and FIFO. Reset by software.	1
0	bS0_AUTO_IF	RW	Clear byte receiving completion interrupt flag automatically by FIFO valid operation enable bit:	0

			1: It will clear byte receiving completion interrupt flag S0_IF_BYTE automatically when there is valid FIFO read/write operation.	

SPI0 data register (SPI0_DATA):

Bit	Name	Access	Description	Reset value
[7:0]	SPI0_DATA	RW	Including physically separated receive FIFO and transmit FIFO. The receive FIFO is used for read operation. The transmit FIFO is used for write operation. SPI transmission can be started by valid read/write operation	xxh

SPI0 status register (SPI0_STAT):

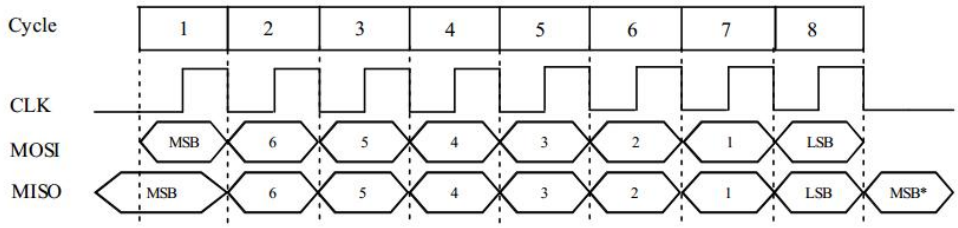
Bit	Name	Access	Description	Reset value
7	S0_FST_ACT	R0	1: First byte has been received in slave mode	0
6	S0_IF_OV	RW	FIFO overflow flag in slave mode: 1: FIFO overflow interrupt. 0: No interrupt Directly write 0 to reset, or write 1 to the corresponding bit in the register to reset. Transmit FIFO empty triggers interrupt when bS0_DATA_DIR=0. Receive FIFO full triggers interrupt when bS0_DATA_DIR=1.	0
5	S0_IF_FIRST	RW	The first byte received completion interrupt flag in slave mode: 1: The first byte has been received. Directly write 0 to reset, or write 1 to the corresponding bit in the register to reset.	0
4	S0_IF_BYTE	RW	Data byte transfer completion interrupt flag 1: One byte has been transferred. Directly write 0 to reset, or write 1 to the corresponding bit in the register to reset. Valid FIFO operation while bS0_AUTO_IF=1 can also reset it.	0
3	S0_FREE	R0	SPI0 free flag 1: No SPI shifting at present, usually in free period between data bytes.	1
2	S0_T_FIFO	R0	SPI0 transmit FIFO count, the valid value is 0 or 1	0
1	Reserved	R0	Reserved	0
0	S0_R_FIFO	R0	SPI0 receive FIFO count, the valid value is 0 or 1	0

14.3 SPI Transfer Format

SPI host mode supports two transfer formats, including mode0 and mode3, which can be selected by setting bSn_MST_CLK in SPIn_CTRL. CH547 always samples MISO data during CLK rising edge. The data transfer formats are shown below.

Mode0: bSn_MST_CLK = 0

Figure 14.3.1 SPI mode0 timing diagram



Mode3: bSn_MST_CLK = 1

Figure 14.3.2 SPI mode3 timing diagram

14.4 SPI Configuration

14.4.1 SPI Master Mode Configuration

In SPI master mode, SCK pin outputs serial clock, and CS output pin can be assigned as any I/O pin.

SPI0 configuration steps:

(1). Configure SPI clock frequency by setting SPI0_CK_SE.

(2). Configure SPI master mode by setting bS0_MODE_SLV in SPI0_SETUP to 0.

(3). Set bS0_MST_CLK in SPI0_CTRL to select mode0/3 as required.

(4). Set bS0_SCK_OE and bS0_MOSI_OE in SPI0_CTRL to 1, set bS0_MISO_OE to 0, set bSCK and bMOSI as output, bMISO as input, and CS pin as output.

Data transmission:

(1). Write SPI0_DATA register, write data ready for sending to FIFO and start SPI transmission once automatically.

(2). Wait for S0_FREE until it is 1, indicating that data transmission is over, and can continue to send next byte.

Data reception:

(1). Write SPI0_DATA register, start SPI transmission once by writing any data such as 0FFh to FIFO.

(2). Wait for S0_FREE until it is 1, indicating that data reception is over, and can get data by reading SPI0_DATA.

(3). The operation above can also start SPI transmission once while bS0_DATA_DIR has been 1, otherwise no SPI transmission starts.

14.4.2 SPI Slave Mode Configuration

Only SPI0 supports slave mode. In slave mode, the serial clock is received on the SCK pin from the master device.

(1). Set bS0_MODE_SLV in SPI0_SETUP to 1, to select slave mode.

(2). Set bS0_SCK_OE and bS0_MOSI_OE in SPI0_CTRL to 0, set bS0_MISO_OE to 1, set bSCK, bMOSI and

bMISO as well as CS pin as input. When SCS is valid (low level), MISO will automatically enable output. In addition, it is recommended to set MISO pin high impedance input mode (P1_MOD_OC[6]=0, P1_DIR_PU[6]=0), so that MISO will not output during invalid CS, which is conductive to sharing the SPI bus.

(3). Optional step. Set SPI0_S_PRE for the first data output after the CS pin is effective. After the 8 serial clocks, that is the first data byte exchanged, the CH547 slave device gets the first byte (possibly command code) from SPI master, and the external SPI master gets the data byte (possibly status value) in SPI0_S_PRE. The bit7 in SPI0_S_PRE will be automatically loaded into the MISO pin during low level SCK after the SCS pin is effective. In SPI mode0, if the bit7 in SPI0_S_PRE is set, the external SPI master will get the preset value of bit7 in SPI0_S_PRE by inquiring the MISO pin when the SCS pin is effective but there is no data transfer, thereby the value of bit7 in SPI0_S_PRE can be obtained only by the effective SCS.

Data transmission:

Read S0_IF_BYTE or wait for interrupt, and write SPI0_DATA after each SPI data byte transfer, and write the data to be sent to FIFO. Or wait for S0_FREE to be changed from 0 to 1, and the next byte can be transmitted.

Data reception:

Read S0_IF_BYTE or wait for interrupt, and read the SPI0_DATA register after each SPI data byte transfer, and obtain the received data from FIFO. Read S0_R_FIFO to know whether there are any remaining bytes in FIFO.

15. Analog to Digital Converter (ADC) and Touch-key (TKEY)

15.1 Introduction to ADC and CMP

CH547 provides a 12-bit analog to digital converter, including ADC and CMP.

This ADC provides 12 external analog signal input channels and 4 internal input channels (reference voltage), which allows time-sharing acquisition, and supports analog input voltage from 0 to VDD. CH546 only provides 8 external analog signal input channels (AIN0-AIN7) and 4 internal input channels.

The positive input of the CMP multiplexes the above ADC inputs. The inverse input has 2 external analog signal input channels and 2 internal reference voltage input channels, which allows time-sharing comparison. There are more than 52 kinds of combinations, supporting analog input voltage from 0 to VDD.

15.2 ADC and CMP Register

Table 15.2.1 List of ADC registers

Name	Address	Description	Reset value
ADC_CTRL	F2h	ADC control and status register	xxh
ADC_CFG	F3H	ADC configuration register	00h
ADC_DAT_H	F5h	ADC result data high byte (read only)	0xh
ADC_DAT_L	F4h	ADC result data low byte (read only)	xxh
ADC_DAT	F4h	16-bit SFR consists of ADC_DAT_L and ADC_DAT_H	0xxxh
ADC_CHAN	F6h	ADC analog signal channel selection register	00h
ADC_PIN	F7h	ADC pin digital input control register	00h

ADC Control and Status Register (ADC_CTRL):

Bit	Name	Access	Description	Reset value
7	bCMPDO	RO	CMP result output bit after synchronous delay, the status of bCMPO after synchronous delay with bCMP_IF	x
6	bCMP_IF	RW	CMP result change interrupt flag 1: CMP result has changed. Write 1 to reset.	0
5	bADC_IF	RW	ADC conversion completion interrupt flag 1: An ADC conversion is completed. Write 1 to reset or write TKEY_CTRL to reset.	0
4	bADC_START	RW	ADC start control, set 1 to start an ADC conversion. Reset automatically at the end of ADC conversion.	0
3	bTKEY_ACT	RO	Touch-key detection activation state 1: Capacitor is being charged and the ADC is being measured.	0
[2:1]	Reserved	R0	Reserved	00b
0	bCMPO	RO	CMP result real-time output 0: Voltage on positive input is lower than voltage on inverted input. 1: Voltage on positive input is higher than voltage on inverted input.	x

ADC Configuration Register (ADC_CFG):

Bit	Name	Access	Description	Reset value
[7:6]	Reserved	R0	Reserved	00b
5	bADC_AIN_EN	RW	CMP positive input and ADC input channel external AIN enable 1: One of 16 AIN is selected by MASK_ADC_CHAN. 0: Disable external AIN.	0
4	bVDD_REF_EN	RW	Internal reference voltage enable 1: Internal reference voltage is generated by multiple series resistors to the supply voltage. 0: Disable divider resistance.	0
3	bADC_EN	RW	ADC power control 0: ADC power off, and enter sleep state. 1: ADC power on.	0
2	bCMP_EN	RW	CMP power control 0: CMP power off, and enter sleep state. 1: CMP power on. In addition, it will automatically enable CMP wake-up function, and it will automatically wake up if the comparator result changes during sleep.	0
1	bADC_CLK1	RW	ADC reference clock frequency selection high bit	0
0	bADC_CLK0	RW	ADC reference clock frequency selection low bit	0

Table 15.2.2 ADC reference clock frequency selection

bADC_CLK1	bADC_CLK0	ADC reference clock frequency	Time required to complete an ADC	Applicable scope
0	0	750KHz	512 Fosc	Rs<=16KΩ or Cs>=0.08uF
0	1	1.5MHz	256 Fosc	Rs<=8KΩ or Cs>=0.08uF
1	0	3MHz	128 Fosc	VDD>=3V and (Rs<=4KΩ or Cs>=0.08uF)
1	1	6MHz	64 Fosc	VDD>=4.5V and (Rs<=2KΩ or Cs>=0.08uF)

Note: VDD refers to supply voltage, Cs refers to capacitance parallel with signal source, and Rs refers to internal resistance in series with signal source (the sampling time is only 3 reference clocks).

ADC Analog Signal Channel Selection Register (ADC_CHAN):

Bit	Name	Access	Description	Reset value
[7:6]	MASK_CMP_CHAN	RW	CMP inverted input signal channel selection	00b
[5:4]	MASK_ADC_I_CH	RW	CMP positive input and ADC input internal signal channel selection	00b
[3:0]	MASK_ADC_CHAN	RW	CMP positive input and ADC input external signal channel selection when bADC_AIN_EN=1. External signal channel disable when bADC_AIN_EN=0. For CH546, only the lower 3 bits are valid	0000b

Table 15.2.1 CMP inverted input signal channel selection

bCMP_EN	bVDD_REF_EN	MASK_CMP_CHAN	CMP inverted input signal channel selection
0	x	xxb	Disconnect signal channel, suspended
1	0	00b	Disconnect signal channel, suspended
1	1	00b	Connect to internal reference voltage: 12.5% of VDD voltage
1	0	01b	Connect to internal reference voltage: 100% of VDD voltage
1	1	01b	Connect to internal reference voltage: 25% of VDD voltage
1	x	10b	Connect to external signal AIN1 (P1.1)
1	x	11b	Connect to external signal AIN2 (P1.2)

Table 15.2.2 CMP positive input and ADC input internal signal channel selection

bADC_EN	bADC_AIN_EN	bVDD_REF_EN	MASK_ADC_I_CH	CMP positive input and ADC input internal signal channel selection
x	x	0	00b	Disconnect internal signal channel, suspended
x	x	1	00b	Connect to internal reference voltage: 50% of VDD voltage
x	x	x	01b	Connect to internal reference voltage: V33 voltage
x	x	x	10b	Connect to internal voltage/with noise: 54.5% of V33 voltage
1	0	x	11b	Connect to internal signal: temperature sensor (TS), Please refer to the C example program for details
0	x	x	11b	Disconnect internal signal channel, suspended
x	1	x	11b	Disconnect internal signal channel, suspended

Table 15.2.3 CMP positive input and ADC input external signal channel selection

bADC_AIN_EN	MASK_ADC_CHAN	CMP positive input and ADC input external signal channel selection
0	xxxxb	Disconnect the external signal channel (AIN0-AIN11), suspended
1	0000b	Connect to external signal AIN0 (P1.0)
1	0001b	Connect to external signal AIN1 (P1.1)
1	0010b	Connect to external signal AIN2 (P1.2)
1	0011b	Connect to external signal AIN3 (P1.3)
1	0100b	Connect to external signal AIN4 (P1.4)
1	0101b	Connect to external signal AIN5 (P1.5)
1	0110b	Connect to external signal AIN6 (P1.6)
1	0111b	Connect to external signal AIN7 (P1.7)

1	1000b	Connect to external signal AIN8 (P0.0)
1	1001b	Connect to external signal AIN9 (P0.1)
1	1010b	Connect to external signal AIN10 (P0.2)
1	1011b	Connect to external signal AIN11 (P0.3)
1	11xxb	Disconnect the external signal channel (AIN0-IN11), suspended

For CH546, only the lower 3 bits of MASK_ADC_CHAN are valid, and MASK_ADC_CHAN[3] is always 0.

CMP positive input and ADC input can only be connected to the internal signal, or only connected to external signal, or connected to both the internal and external signals. When connected to internal and external signals simultaneously, intercommunication can be implemented between internal signals and external signals. The ON resistance is a series connection of 2 Rsw, and the internal reference voltage (there is also its internal resistance) will be connected to the external signal pins AIN0-AIN11 via the above two Rsw resistors, which is equivalent to the pull-up resistor providing a specific voltage for signal pins.
Ca is a 15pF sampling capacitor. The R2/R1 resistance ratio is 54.5:45.5. The 4R/2R/R resistance ratio is 4:2:1.

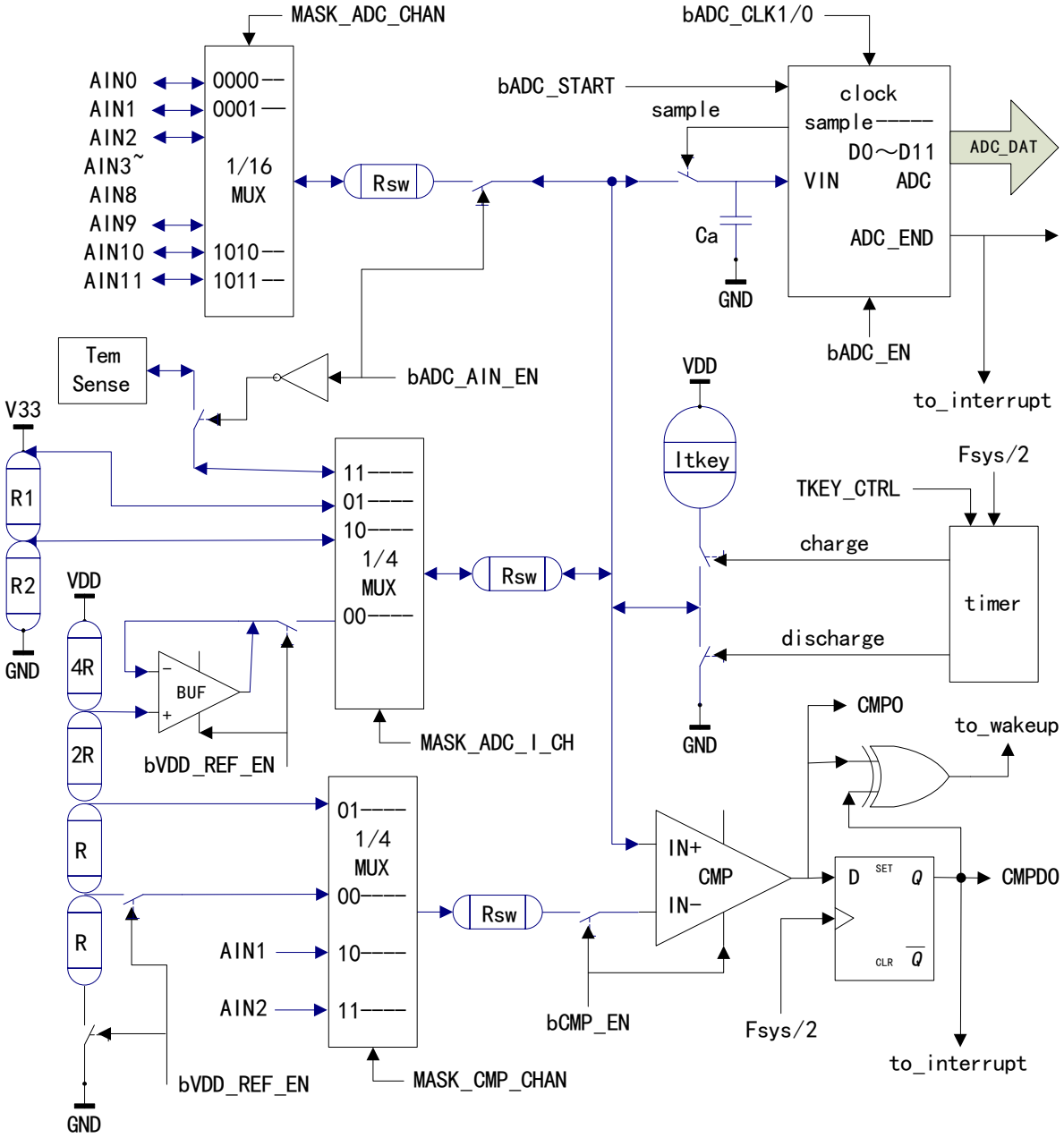
ADC Data Register (ADC_DAT):

Bit	Name	Access	Description	Reset value
[7:0]	ADC_DAT_H	RO	High byte of ADC sampling result data	0xh
[7:0]	ADC_DAT_L	RO	Low byte of ADC sampling result data	xxh

ADC Pin Digital Input Control Register (ADC_PIN):

Bit	Name	Access	Description	Reset value
7	Reserved	RO	Reserved	0
6	Reserved	RO	Reserved	0
5	bAIN10_11_DI_DIS	RW	AIN10 and AIN11 digital input disable 0: AIN10 and AIN11 digital input enabled.	0
4	bAIN8_9_DI_DIS	RW	AIN8 and AIN9 digital input disable 0: AIN8 and AIN9 digital input enabled.	0
3	bAIN6_7_DI_DIS	RW	AIN6 and AIN7 digital input disable 0: AIN6 and AIN7 digital input enabled.	0
2	bAIN4_5_DI_DIS	RW	AIN4 and AIN5 digital input disable 0: AIN4 and AIN5 digital input enabled.	0
1	bAIN2_3_DI_DIS	RW	AIN2 and AIN3 digital input disable 0: AIN2 and AIN3 digital input enabled.	0
0	bAIN0_1_DI_DIS	RW	AIN0 and AIN1 digital input disable 0: AIN0 and AIN1 digital input enabled.	0

Figure 15.2.1 ADC/CMP/TKEY structure diagram (blue lines to represent analog signals)



15.3 TKEY Register

Table 15.3.1 List of TKEY registers

Name	Address	Description	Reset value
TKEY_CTRL	F1h	Touch key charging pulse width control register	00h

Touchkey Charging Pulse Width Control Register (TKEY_CTRL):

Bit	Name	Access	Description	Reset value
[7:0]	TKEY_CTRL	WO	Touch key charging pulse width value, only the lower 7 bits are valid, counted in 2 times the system period (2/Fsys), the ADC is automatically activated to measure the voltage on the capacitor when timed.	00h

15.4 ADC and Touch-Key Function

ADC sampling mode configuration steps:

(1). Set bADC_EN in ADC_CFG to 1, to enable ADC module, and set bADC_CLK0/1 to select frequency.

(2). Set MASK_ADC_CHAN or MASK_ADC_I_CH in ADC_CHAN register, to select external or internal signal channel.

(3). Optional step. Reset bADC_IF. Optional. The interrupt needs to be enabled if the interrupt mode is enabled.

(4). Set bADC_START in ADC_CTRL, to start an ADC conversion.

(5). Wait for bADC_START until it is 0, or bADC_IF to be set to 1 (if cleared before), indicating that ADC conversion is completed and the result can be read through ADC_DAT. This data is the value of the input voltage relative to 4095 equal parts of the VDD supply voltage, for example, if the result value is 475, the input voltage is approximate to 475/4095 of the VDD voltage. If the VDD supply voltage is also uncertain, another reference voltage value can be measured, and the measured input voltage value and the VDD supply voltage value can be calculated proportionally.

(6). Set bADC_START again, to start the next ADC conversion.

(7). If the ADC reference clock frequency is high, resulting in a short sampling time, or high internal resistance in series with signal source, or large Rsw internal resistance due to low supply voltage, then Ca may not sample enough signal voltage, and it will affect ADC result. The solution is to discard the first ADC data, immediately start the second ADC and use its ADC result data (sample twice).

(8). In case of high accuracy requirement, it is recommended to calibrate before use and eliminate the inherent deviation with software.

CMP mode configuration steps:

(1). Set bCMP_EN in ADC_CFG to 1, to enable CMP module.

(2). Set MASK_ADC_CHAN, MASK_CMP_CHAN and MASK_ADC_I_CH in ADC_CHAN, to select positive/inverted input signals respectively. Multiple combinations can be selected, such as comparison between AIN0-AIN11 and AIN1/AIN2, comparison between AIN0-AIN11 and internal reference voltage, and comparison between AIN1/AIN2 and internal reference voltage, etc.

(3). Optional step. Reset bCMP_IF. Optional, the interrupt needs to be enabled if the interrupt mode is enabled.

(4). Read the bCMPO bit to get the CMP result.

(5). If the bCMP_IF is changed into 1, it indicates that the CMP result has changed.

Touch-Key detection steps:

(1). Set bADC_EN in ADC_CFG to 1, to enable ADC module, and set bADC_CLK0/1 to select frequency.

(2). Set MASK_ADC_CHAN in ADC_CHAN, to select touch-key signal channel.

(3). Select the appropriate charging pulse width according to the actual capacitance of the touch key, and write into the TKEY_CTRL register. The simple calculation formula is as follows (assume that the external capacitance of the touch key Ckey=25pF, VDD=5V, Fsys=12MHz, rough calculation):

count=(Ckey+Cint)*0.7VDD/ITKEY/(2/Fsys)=(25p+15p)*0.35*5*12M/50u=17

TKEY_CTRL=count > 127 ? 127 : count

(4). Optional step. The interrupt needs to be enabled if the interrupt mode is enabled.

(5). When the capacitor charge timing of the touch key is reached, CH547 will automatically set bADC_START to start ADC and measure the voltage on the capacitor

(6). Wait for bTKEY_ACT until it is 0, or bADC_IF to be set to 1, indicating the end of charging and ADC conversion, and the result can be read through ADC_DAT. Software then compares this value with that without pressing the key, and determines whether the touch key is pressed or not according to the change in capacitance.

(7). Shift to step (2) as required, to select another touch key signal channel for detection.
(8). If the actual capacitance of the touch key is greater than 40pF or the system clock frequency is 48MHz/6MHz, then the internal automatic discharge time may be insufficient, and it may be necessary to output GPIO low level at about 1uS for full discharge of the above capacitor.

For the above selected external analog signal channel, the corresponding GPIO pin must be set in high-impedance input mode or open-drain output mode and set in output 1 state (equivalent to high-impedance input), Pn_DIR_PU[x]=0, and disable the pull-up resistor and pull-down resistor.

16. USB Controller

16.1 USB Introduction

CH547 has built-in USB device controller and USB transceiver, with features as follows:
(1). Support USB 2.0 full-speed (12Mbps) and low-speed (1.5Mbps) modes;
(2). Support USB control transmission, bulk transmission, interrupt transmission, and synchronous/real-time transmission;
(3). Support up to 64-byte packet, with built-in FIFO, support interrupt and DMA.

CH547 USB registers are divided into:
(1). USB global registers;
(2). USB device controller registers.

16.2 Global register

Table 16.2.1 USB global registers (those marked in grey are controlled by bUC_RESET_SIE reset)

Name	Address	Description	Reset value
USB_INT_FG	D8h	USB interrupt flag register	0010 0000b
USB_INT_ST	D9h	USB interrupt status register (read only)	00xx xxxxb
USB_MIS_ST	DAh	USB miscellaneous status register (read only)	xx10 1000b
USB_RX_LEN	DBh	USB receiving length register (read only)	0xxx xxxxb
USB_INT_EN	E1h	USB interrupt enable register	0000 0000b
USB_CTRL	E2h	USB control register	0000 0110b
USB_DEV_AD	E3h	USB device address register	0000 0000b

USB Interrupt Flag Register (USB_INT_FG):

Bit	Name	Access	Description	Reset value
7	U_IS_NAK	RO	1: Receive NAK busy response during current USB transfer. 0: Receive non-NAK response.	0
6	U_TOG_OK	RO	The current USB transfer DATA0/1 synchronization flag matching status 1: Indicates synchronization and valid data; 0: Indicates lack of synchronization and potentially invalid data.	0
5	U_SIE_FREE	RO	The idle status bit of the USB protocol processor	1

			0: Busy, indicating an ongoing USB transfer; 1: USB idle.	
4	UIF_FIFO_OV	RW	USB FIFO overflow interrupt flag 1: FIFO overflow interrupt. 0: No interrupt. Directly write 0 to reset, or write 1 to the corresponding bit in the register to reset.	0
3	Reserved	RO	Reserved	0
2	UIF_SUSPEND	RW	USB bus suspend or wake-up event interrupt flag 1: There is an interrupt, triggered by USB suspend event or wake-up event. 0: No interrupt. Directly write 0 to reset, or write 1 to the corresponding bit in the register to reset.	0
1	UIF_TRANSFER	RW	USB transfer completion interrupt flag 1: There is an interrupt, triggered by USB transfer completion. 0: No interrupt. Directly write 0 to reset, or write 1 to the corresponding bit in the register to reset.	0
0	UIF_BUS_RST	RW	USB bus reset event interrupt flag 1: There is an interrupt, triggered by USB bus reset event. 0: No interrupt. Directly write 0 to reset, or write 1 to the corresponding bit in the register to reset.	0

USB Interrupt Status Register (USB_INT_ST):

Bit	Name	Access	Description	Reset value
7	bUIS_IS_NAK	RO	1: Receive NAK busy response during current USB transfer. The same as U_IS_NAK	0
6	bUIS_TOG_OK	RO	Current USB transfer DATA0/1 synchronization flag match state 1: Synchronization. 0: Out of synchronization. The same as U_TOG_OK	0
5	bUIS_TOKEN1	RO	Current USB transmission transaction token PID high bit	x
4	bUIS_TOKEN0	R0	Current USB transmission transaction token PID low bit	x
[3:0]	MASK_UIS_ENDP	RO	Endpoint serial number of the current USB transfer transaction 0000: Endpoint 0. ... 1111: Endpoint 15.	xxxxb

bUIS_TOKEN1 and bUIS_TOKEN0 make up MASK_UIS_TOKEN, the token PID used to identify the current USB transmission transaction in USB device mode: 00 for OUT packets; 01 for SOF packets; 10 for IN packets; 11 for SETUP packets.

USB Miscellaneous Status Register (USB_MIS_ST):

Bit	Name	Access	Description	Reset value
7	Reserved	RO	Reserved	x
6	Reserved	RO	Reserved	x
5	bUMS_SIE_FREE	RO	USB SIE free state 0: Busy, and USB transfer is in progress. 1: Free. The same as U_SIE_FREE	1
4	bUMS_R_FIFO_RDY	RO	USB receive FIFO data ready state 0: Receive FIFO is empty. 1: Receive FIFO is not empty.	0
3	bUMS_BUS_RESET	RO	USB bus reset status 0: No USB bus reset at present. 1: USB bus reset is in progress.	1
2	bUMS_SUSPEND	RO	USB suspend status 0: There is USB activity at present. 1: No USB activity for some time, and request to be suspended.	0
1	Reserved	RO	Reserved	0
0	Reserved	RO	Reserved	0

USB receiving length register (USB_RX_LEN):

Bit	Name	Access	Description	Reset value
[7:0]	bUSB_RX_LEN	RO	The number of bytes received by USB endpoint currently	xxh

USB interrupt enable register (USB_INT_EN):

Bit	Name	Access	Description	Reset value
7	bUIE_DEV_SOF	RW	1: Enable receiving SOF packet interrupt. 0: Disable.	0
6	bUIE_DEV_NAK	RW	1: Enable receiving NAK interrupt. 0: Disable.	0
5	Reserved	RO	Reserved	0
4	bUIE_FIFO_OV	RW	1: Enable FIFO overflow interrupt. 0: Disable.	0
3	Reserved	RO	Reserved	0
2	bUIE_SUSPEND	RW	1: Enable USB bus suspend or wake-up event interrupt. 0: Disable.	0
1	bUIE_TRANSFER	RW	1: Enable USB transfer completion interrupt. 0: Disable.	0
0	bUIE_BUS_RST	RW	1: Enable USB bus reset event interrupt. 0: Disable.	0

USB Control Register (USB_CTRL)

Bit	Name	Access	Description	Reset value
7	Reserved	RO	Reserved	0
6	bUC_LOW_SPEED	RW	USB bus speed selection 0: Full-speed (12Mbps). 1: Low-speed (1.5Mbps).	0
5	bUC_DEV_PU_EN	RW	USB device enable and internal pull-up resistor enable 1: Enable USB device transfer and enable internal pull-up resistor.	0
5	bUC_SYS_CTRL1	RW	USB system control high bit	0
4	bUC_SYS_CTRL0	RW	USB system control low bit	0
3	bUC_INT_BUSY	RW	Auto pause enable bit before USB transfer completion interrupt flag is not reset 1: Auto pause and respond busy NAK before UIF_TRANSFER is not reset. 0: Not pause.	0
2	bUC_RESET_SIE	RW	USB SIE software reset control 1: Force reset USB SIE and most of USB control registers. Reset by software.	1
1	bUC_CLR_ALL	RW	1: Clear USB interrupt flag and FIFO. Reset by software.	1
0	bUC_DMA_EN	RW	1: Enable USB DMA and DMA interrupt. 0: Disable.	0

USB system control consists of bUC_SYS_CTRL1 and bUC_SYS_CTRL0.

bUC_SYS_CTRL1	bUC_SYS_CTRL0	USB system control description
0	0	Disable USB device function, disable internal pull-up resistor
0	1	Enable USB device function, disable internal pull-up resistor, and an external pull-up resistor is required
1	X	Enables the USB device function and enables the internal 1.5KΩ pull-up resistor. This pull-up resistor takes precedence over the pull-down resistor and can also be used in GPIO mode

USB Device Address Register (USB_DEV_AD):

Bit	Name	Access	Description	Reset value
7	bUDA_GP_BIT	RW	USB general-purpose flag. User-defined. Can be reset and set by software.	0
[6:0]	MASK_USB_ADDR	RW	USB device address	00h

16.3 Device Register

In USB device mode, CH547 provides 5 bidirectional endpoints, including endpoint0-endpoint4. The maximum data packet size of all endpoints is 64 bytes.

Endpoint0 is the default endpoint and supports control transfer. Transmission and reception share a 64-byte data buffer.

Endpoint1, endpoint2, endpoint3 each has a transmission endpoint IN and a reception endpoint OUT. The transmitter and receiver each has a single 64-byte buffer or a double 64-byte buffer, support control transfer, bulk transfer, interrupt transfer, and real-time/isochronous transfer.

Endpoint4 has a transmission endpoint IN and a reception endpoint OUT. The transmitter and receiver each has a single 64-byte buffer, supports control transfer, bulk transfer, interrupt transfer, and real-time/isochronous transfer.

Each endpoint has a control register (UEPn_CTRL) and a transmittal length register (UEPn_T_LEN) (n=0/1/2/3/4), to configure the synchronization trigger bit of endpoint, the response to OUT transactions and IN transactions and the transmittal length.

As the necessary USB bus pull-up resistor for USB device, it can be set to be enabled/disabled by software at any time. When bUC_DEV_PU_EN in USB_CTRL is set to 1, CH547 will internally connect the pull-up resistor to USB DP pin or DM pin based on bUD_LOW_SPEED and enable the USB device function.

When USB bus reset or USB bus suspend/wake-up event is detected, or when the USB successfully processes data transmission and reception, USB SIE will set the corresponding interrupt flag and generate interrupt request. The application program can directly read, or read and analyze USB_INT_FG in the USB interrupt service program, and perform corresponding processing according to UIF_BUS_RST and UIF_SUSPEND. In addition, if UIF_TRANSFER is valid, it is required to continue to analyze USB_INT_ST, and perform the corresponding processing according to MASK_UIS_ENDP and MASK_UIS_TOKEN. If bUEP_R_TOG of OUT transaction of each endpoint is set in advance, you can judge whether the synchronization trigger bit of the packet received matches the synchronization trigger bit of the endpoint through U_TOG_OK or bUIS_TOG_OK. If the data is synchronized, the data is valid. If the data is not synchronized, the data should be discarded. Every time the USB receive/transmit interrupt is processed, the synchronization trigger bit of corresponding endpoint should be modified correctly to synchronize the packet sent next time and detect whether the packet received next time is synchronized. In addition, bUEP_AUTO_TOG can be set to automatically toggle the corresponding synchronization trigger bit after successful reception/transmission.

The data to be sent by each endpoint is in their own buffer, and the transmittal length is independently set in UEPn_T_LEN. The data received by each endpoint is in their own buffer, but the receiving length is in USB_RX_LEN, and it can be distinguished according to the current endpoint serial number when USB is receiving an interrupt.

Table 16.3.1 List of USB device registers (those marked in grey are controlled by RB_UC_RESET_SIE reset)

Name	Address	Description	Reset value
UDEV_CTRL	D1h	USB device physical port control register	00xx 0000b
UEP1_CTRL	D2h	Endpoint1 control register	0000 0000b
UEP1_T_LEN	D3h	Endpoint1 transmit length register	0xxx xxxxb
UEP2_CTRL	D4h	Endpoint2 control register	0000 0000b
UEP2_T_LEN	D5h	Endpoint2 transmit length register	0000 0000b
UEP3_CTRL	D6h	Endpoint3 control register	0000 0000b
UEP3_T_LEN	D7h	Endpoint3 transmit length register	0xxx xxxxb
UEP0_CTRL	DCh	Endpoint0 control register	0000 0000b
UEP0_T_LEN	DDh	Endpoint0 transmit length register	0xxx xxxxb
UEP4_CTRL	DEh	Endpoint4 control register	0000 0000b
UEP4_T_LEN	DFh	Endpoint4 transmit length register	0xxx xxxxb

UEP4_1_MOD	EAh	Endpoint1/4 mode control register	0000 0000b
UEP2_3_MOD	EBh	Endpoint2/3 mode control register	0000 0000b
UEP0_DMA_H	EDh	Endpoint0&4 buffer start address high byte	0000 0xxxb
UEP0_DMA_L	ECh	Endpoint0&4 buffer start address low byte	xxxx xxxxb
UEP0_DMA	ECh	16-bit SFR consists of UEP0_DMA_L and UEP0_DMA_H	0xxxh
UEP1_DMA_H	EFh	Endpoint1 buffer start address high byte	0000 0xxxb
UEP1_DMA_L	EEh	Endpoint1 buffer start address low byte	xxxx xxxxb
UEP1_DMA	EEh	16-bit SFR consists of UEP1_DMA_L and UEP1_DMA_H	0xxxh
UEP2_DMA_H	E5h	Endpoint2 buffer start address high byte	0000 0xxxb
UEP2_DMA_L	E4h	Endpoint2 buffer start address low byte	xxxx xxxxb
UEP2_DMA	E4h	16-bit SFR consists of UEP2_DMA_L and UEP2_DMA_H	0xxxh
UEP3_DMA_H	E7h	Endpoint3 buffer start address high byte	0000 0xxxb
UEP3_DMA_L	E6h	Endpoint3 buffer start address low byte	xxxx xxxxb
UEP3_DMA	E6h	16-bit SFR consists of UEP3_DMA_L and UEP3_DMA_H	0xxxh

USB Device Physical Port Control Register (UDEV_CTRL), controlled by bUC_RESET_SIE reset:

Bit	Name	Access	Description	Reset value
7	bUD_PD_DIS	RW	USB UDP/UDM pin internal pull-down resistor disable 1: Disable internal pull-down resistor. 0: Enable internal pull-down resistor. This bit also can be used in GPIO mode to provide pull-down resistor.	0
6	Reserved	RO	Reserved	0
5	bUD_DP_PIN	RO	Current UDP pin status 0: Low level. 1: High level.	x
4	bUD_DM_PIN	RO	Current UDM pin status 0: Low level. 1: High level.	x
3	Reserved	RO	Reserved	0
2	bUD_LOW_SPEED	RW	USB device physical port low-speed mode enable bit 1: Low-speed (1.5Mbps) mode. 0: Full-speed (12Mbps) mode.	0
1	bUD_GP_BIT	RW	USB device mode general-purpose flag User-defined. Can be reset and set by software.	0
0	bUD_PORT_EN	RW	USB device physical port enable 1: Enable physical port. 0: Disable physical port.	0

Endpoint n Control Register (UEPn_CTRL):

Bit	Name	Access	Description	Reset value
7	bUEP_R_TOG	RW	Expected data toggle flag of USB endpoint n receiver (SETUP/OUT):	0

			1: Expected DATA1. 0: Expected DATA0.	
6	bUEP_T_TOG	RW	Prepared data toggle flag of USB endpoint n transmitter (IN): 1: Transmit DATA1. 0: Transmit DATA0.	0
5	Reserved	RO	Reserved	0
4	bUEP_AUTO_TOG	RW	Auto toggle enable 1: Auto toggle. 0: Manual toggle. Only supports single-receive or single-transmit mode of endpoint1/2/3, not supported when RX_EN and TX_EN of an endpoint are 1.	0
3	bUEP_R_RES1	RW	High bit of handshake response type for USB endpoint n receiving (SETUP/OUT).	0
2	bUEP_R_RES0	RW	Low bit of handshake response type for USB endpoint n receiving (SETUP/OUT).	0
1	bUEP_T_RES1	RW	High bit of handshake response type for USB endpoint n transmittal (IN).	0
0	bUEP_T_RES0	RW	Low bit of handshake response type for USB endpoint n transmittal (IN).	0

MASK_UEP_R_RES consists of bUEP_R_RES1 and bUEP_R_RES0, used to indicate handshake response type for USB endpoint n receiver (SETUP/OUT):
00: ACK or ready.
01: Timeout/no response, for real-time/isochronous transfer of non-endpoint0.
10: NAK or busy.
11: STALL or error.

MASK_UEP_T_RES consists of bUEP_T_RES1 and bUEP_T_RES0, used to indicate handshake response type for USB endpoint n transmitter (IN):
00: DATA0/DATA1 or expected ACK.
01: DATA0/DATA1 and expected no response, for real-time/isochronous transfer of non-endpoint0.
10: NAK or busy.
11: STALL or error.

Endpoint n Transmit Length Register (UEPn_T_LEN):

Bit	Name	Access	Description	Reset value
[7:0]	bUEPn_T_LEN	RW	Set the number of data bytes that USB endpoint n is ready to transmit (n = 0/1/3/4).	xxh
	bUEP2_T_LEN		Set the number of data bytes that USB endpoint 2 is ready to transmit	00h

USB Endpoint1/4 Mode Control Register (UEP4_1_MOD):

Bit	Name	Access	Description	Reset value
7	bUEP1_RX_EN	RW	USB endpoint1 receive (OUT) enable:	0

			1: Enable. 0: Disable.	
6	bUEP1_TX_EN	RW	USB endpoint1 transmit (IN) enable: 1: Enable. 0: Disable.	0
5	Reserved	RO	Reserved	0
4	bUEP1_BUF_MOD	RW	Endpoint1 data buffer mode control	0
3	bUEP4_RX_EN	R0	USB endpoint4 receive (OUT) enable: 1: Enable. 0: Disable.	0
2	bUEP4_TX_EN	RW	USB endpoint4 transmit (IN) enable: 1: Enable. 0: Disable.	0
[1:0]	Reserved	RO	Reserved	00b

Configuration of buffer mode of endpoint0 and endpoint4 by bUEP4_RX_EN bit and bUEP4_TX_EN bit. Refer to the following table.

Table 16.3.2 Buffer mode of endpoint0 and endpoint4

bUEP4_RX_EN	bUEP4_TX_EN	Description: buffer start address is UEP0_DMA
0	0	Single 64-byte buffer for endpoint0 receive & transmit (OUT&IN).
1	0	Single 64-byte buffer for endpoint0 receive & transmit (OUT & IN) and single 64-byte buffer for endpoint4 receiving (OUT), total=128 bytes
0	1	Single 64-byte buffer for endpoint0 receive & transmit (OUT&IN) and single 64-byte buffer for endpoint4 transmittal (IN), total=128 bytes
1	1	Single 64-byte buffer for endpoint0 receive & transmit (OUT & IN) + 64-byte buffer for endpoint4 receiving (OUT) + 64-byte buffer for endpoint4 transmittal (IN), total=192bytes. Start address UEP0_DMA+0: endpoint0 receiving & transmittal. Start address UEP0_DMA+64: endpoint4 receiving. Start address UEP0_DMA+128: endpoint4 transmittal.

USB Endpoint2/3 Mode Control Register (UEP2_3_MOD):

Bit	Name	Access	Description	Reset value
7	bUEP3_RX_EN	RW	USB endpoint3 receive (OUT) enable: 1: Enable. 0: Disable.	0
6	bUEP3_TX_EN	RW	USB endpoint3 transmit (IN) enable: 1: Enable. 0: Disable.	0
5	Reserved	RO	Reserved	0
4	bUEP3_BUF_MOD	RW	Endpoint3 buffer mode control	0
3	bUEP2_RX_EN	R0	USB endpoint2 receive (OUT) enable: 1: Enable. 0: Disable.	0

2	bUEP2_TX_EN	RW	USB endpoint2 transmit (IN) enable: 1: Enable. 0: Disable.	0
1	Reserved	RO	Reserved	0
0	bUEP2_BUF_MOD	RW	Endpoint2 buffer mode control	0

Buffer mode of USB endpoint1/2/3 is controlled by bUEPn_RX_EN, bUEPn_TX_EN and bUEPn_BUF_MOD (n=1/2/3). Refer to the following table. In the double 64-byte buffer mode, the first 64-byte buffer is selected based on bUEP_*_TOG=0 and the last 64-byte buffer is selected based on bUEP_*_TOG=1 during USB transfer for automatic switch.

Table 16.3.3 Buffer mode of endpoint n (n=1/2/3)

bUEPn_RX_EN	bUEPn_TX_EN	bUEPn_BUF_MOD	Description: buffer start address is UEPn_DMA
0	0	x	Disable endpoint, and disable UEPn_DMA buffer
1	0	0	Single 64-byte receiving buffer (OUT)
1	0	1	Double 64-byte receiving buffer, selected by bUEP_R_TOG.
0	1	0	Single 64-byte transmitting buffer (IN)
0	1	1	Double 64-byte transmitting buffer, selected by bUEP_T_TOG.
1	1	0	Single 64-byte receiving buffer (OUT). Single 64-byte transmittal buffer (IN)
1	1	1	Double 64-byte receiving buffer, selected by bUEP_R_TOG. Double 64-byte transmitting buffer, selected by bUEP_T_TOG, total=256 bytes. Start address UEPn_DMA+0: endpoint receiving when bUEP_R_TOG=0. Start address UEPn_DMA+64: endpoint receiving when bUEP_R_TOG=1. Start address UEPn_DMA+128: endpoint transmitting when bUEP_T_TOG=0. Start address UEPn_DMA+192: endpoint transmitting when bUEP_T_TOG=1.

USB Endpoint n Buffer Start Address (UEPn_DMA) (n=0/1/2/3):

Bit	Name	Access	Description	Reset value
[7:0]	UEPn_DMA_H	RW	Endpoint n buffer start address high byte, only the low 3 bits are valid, and the high 5 bits are fixed to 0.	0xh
[7:0]	UEPn_DMA_L	RW	Endpoint n buffer start address low byte	xxh

Note: Length of the buffer for receiving data >= min (maximum packet length possible + 2 bytes, 64 bytes)

17. Parameters

17.1 Absolute Maximum Ratings

(Critical or exceeding the absolute maximum value may cause the chip to operate improperly or even be damaged)

Symbol	Parameter description		Min.	Max.	Unit
TA	Ambient temperature during operation	Fsys<40MHz	-40	85	℃
		For custom chips Fsys=48MHz	-20	70	℃
TAROM	Ambient temperature for Flash-ROM/EEPROM erase operations (recommended)		-20	85	℃
TS	Ambient temperature for storage		-55	125	℃
VDD	Supply voltage (VDD is connected to power, GND to ground)		-0.4	7.0	V
V33	Internal USB supply voltage		-0.4	VDD+0.4	V
VIO	Voltage on input/output pins		-0.4	VDD+0.4	V
VIOU	Voltage on UDP/UDM pin		-0.4	V33+0.4	V
VIOHV	Voltage on P5.5/HVOD pin		-0.4	13	V

17.2 Electrical Characteristics at 5V

(Test conditions: TA=25℃, VDD=5V, Fsys=12MHz)

Symbol	Parameter description		Min.	Typ.	Max.	Unit
VDD5	VDD supply voltage	V33 is only connected to an external capacitor	3.7	5	6.5	V
V33	Internal LDO output voltage (Automatically shorted to VDD during sleep)	TA=-15～65℃	3.23	3.3	3.38	V
		TA=-40～85℃	3.2	3.3	3.4	V
ICC24M5	Total supply current when Fsys=24MHz			4.4		mA
ICC12M5	Total supply current when Fsys=12MHz			3.0		mA
ICC750K5	Total supply current when Fsys=750KHz			1.6		mA
ISLP5	Total supply current after standby/normal sleep			1.1	1.5	mA
ISLP5L	Total supply current after power off/deep sleep bLDO_3V3_OFF=1, LDO disabled			4	20	uA
IADC5	ADC operating current			200	800	uA
ICMP5	CMP operating current			100	500	uA
ITKEY5	Touch-key capacitor charging current		35	50	70	uA
VIL5	Input low level voltage		0		1.2	V
VIH5	Input high level voltage		2.4		VDD	V
VOL5	Output low level voltage (I_{IL}=15mA)				0.4	V
VOH5	Output high level voltage (I_{OH}=6mA)		VDD-0.4			V
VOH5U	DP/UDM high level output voltage (I_{OH}=8mA)		V33-0.4			V
VHVOD	Voltage on P5.5/HVOD pin (not output / high impedance)		0	12	12.6	V
IIN	The input current without pull-up resistor		-5	0	5	uA

IDN5	The input current with pull-down resistor	-35	-70	-140	uA
IUP5	The input current with pull-up resistor	35	70	140	uA
IUP5X	The input current with pull-up resistor from low to high	250	400	600	uA
Rsw5	On-resistance of analogue switches for modules such as ADCs	500	700	1350	Ω
Vpot	Threshold voltage for power-on reset	2.3	4.0	4.6	V

17.3 Electrical Characteristics at 3.3V

(Test conditions: TA=25℃, VDD=V33=3.3V, Fsys=12MHz)

Symbol	Parameter description		Min.	Typ.	Max.	Unit
VDD3	VDD supply voltage	V33 is shorted to VDD, with USB enabled	3.0	3.3	3.6	V
		V33 is shorted to VDD, with USB disabled	2.7	3.3	3.6	V
ICC24M3	Total supply current when Fsys=24MHz			4.4		mA
ICC12M3	Total supply current when Fsys=12MHz			3.0		mA
ICC750K3	Total supply current when Fsys=750KHz			1.6		mA
ISLP3	Total supply current after standby/normal sleep			1.1	1.5	mA
ISLP3L	Total supply current after power off/deep sleep bLDO_3V3_OFF=1, LDO disabled			3	16	uA
IADC3	ADC operating current			180	700	uA
ICMP3	CMP operating current			70	300	uA
ITKEY3	Touch-key capacitor charging current		35	50	70	uA
VIL3	Input low level voltage		0		0.8	V
VIH3	Input high level voltage		1.9		VDD	V
VOL3	Output low level voltage (I_{IL}=10mA)				0.4	V
VOH3	Output high level voltage (I_{OH}=4mA)		VDD-0.4			V
VOH3U	DP/UDM high level output voltage (I_{OH}=8mA)		V33-0.4			V
VHVOD	Voltage on P5.5/HVOD pin (not output / high impedance)		0	12	12.6	V
IIN	The input current without pull-up resistor		-5	0	5	uA
IDN3	The input current with pull-down resistor		-15	-30	-60	uA
IUP3	The input current with pull-up resistor		15	30	60	uA
IUP3X	The input current with pull-up resistor from low to high		100	170	250	uA
Rsw3	On-resistance of analogue switches for modules such as ADCs		600	1000	2500	Ω
Vpot	Threshold voltage for power-on reset		2.3	2.7	3.0	V

17.4 Timing Parameters

(Test conditions: TA=25℃, VDD=5V or VDD=V33=3.3V, Fsys=12MHz)

Symbol	Parameter description	Min.	Typ.	Max.	Unit

Fxt	External crystal frequency or XI input clock frequency		6	24	24	MHz
Fosc	Internal clock frequency after calibration when VDD>=3V	TA=-15~65℃	23.52	24	24.48	MHz
		TA=-40~85℃	23.38	24	24.72	MHz
Fosc3	Internal clock frequency after calibration when VDD<3V		23.1	24	24.9	MHz
Fpll	PLL frequency after internal frequency doubling		24	96	96	MHz
Fusb4x	USB sampling clock frequency, with USB function enabled		47.04	48	48.96	MHz
Fsys	System clock frequency (VDD>=3V)		0.1	12	40	MHz
	System clock frequency (VDD<3V)		0.1	12	24	MHz
Tpor	Power on reset delay		8	11	15	mS
Trst	External input valid reset signal width		70			nS
Trdl	Thermal reset delay		20	30	50	uS
Twdc	Formula for calculating watchdog overflow period/timing period		131072 * (0x100 - WDOG_COUNT) / Fsys			
Tusp	Detecting USB auto-hang time		4	5	6	mS
Twaksb	Time to wake up from standby/normal sleep		0.5	0.8	5	uS
Twakdp	Time to wake up from power down/deep sleep		120	200	1000	uS

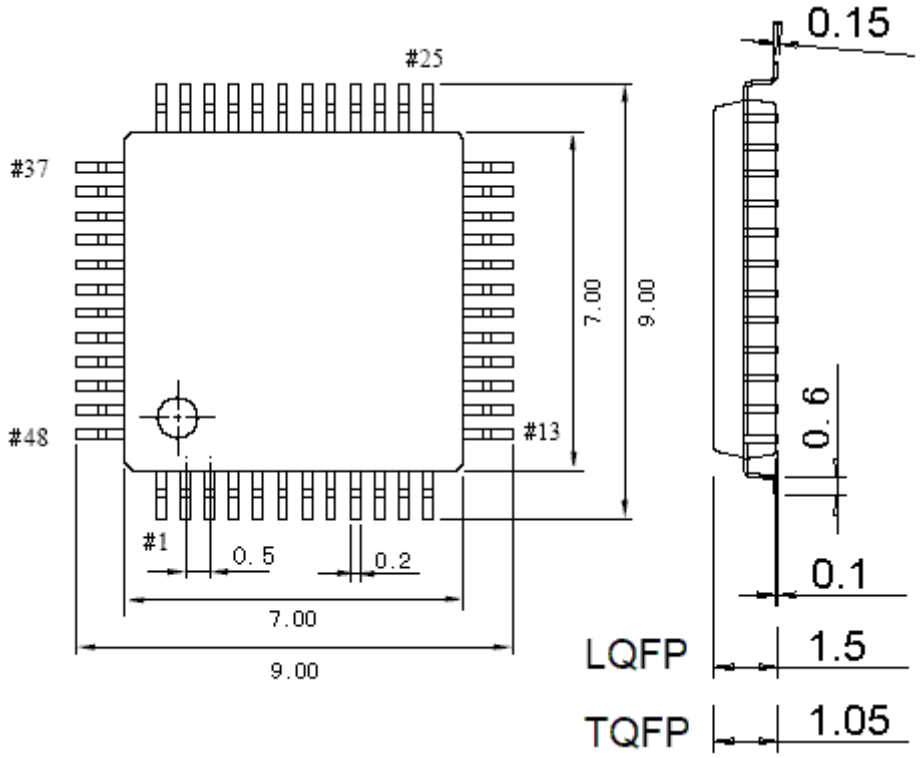
17.5 Other Parameters

(Test conditions: TA=25℃, VDD=4.5V~5.5V or VDD=V33=3.0V~3.6V)

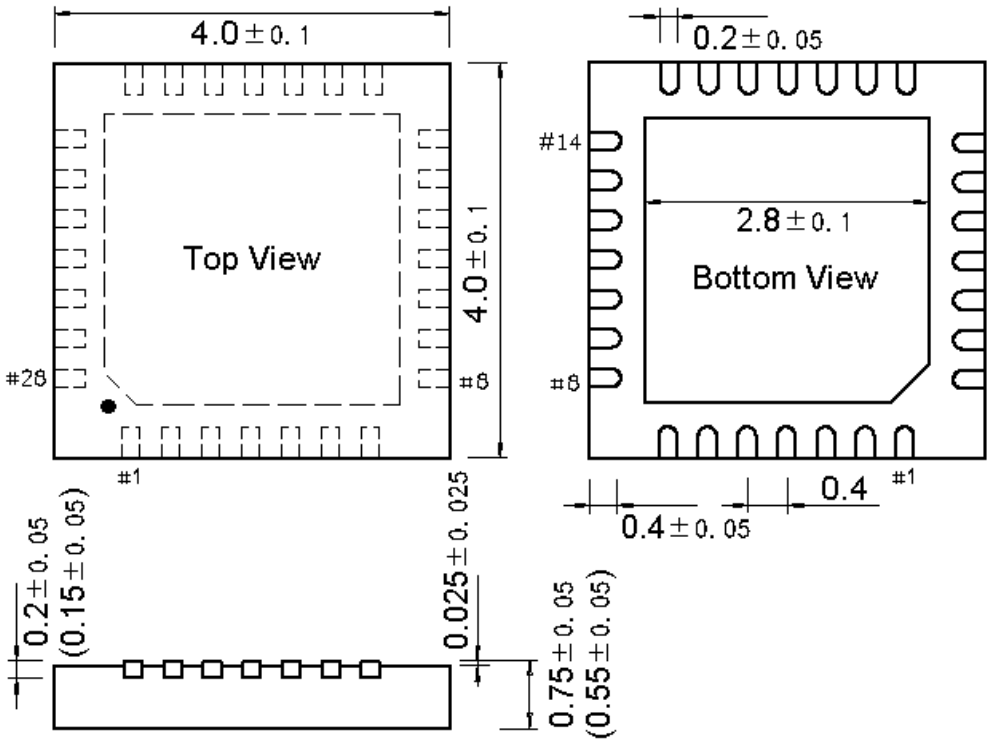
Symbol	Parameter description	Min.	Typ.	Max.	Unit
RTS	Measurement range of TS	-40		90	℃
ATSC	Measurement error of TS after software calibration		±9		℃
CTSV	Sensitivity of TS (voltage/temperature coefficient)	4	5	6	mV/℃
TERPG	Single erase/write operation time of Flash-ROM/EEPROM	2	5	8	mS
NEPCE	Erase/write cycle endurance of Flash-ROM/EEPROM	10K	Sampling value 100K		times
TDR	Data retention capability of Flash-ROM/EEPROM	10			years
VESD	ESD voltage tolerance on I/O input or output pins	4K	Sampling value 8K		V

18. Package Information

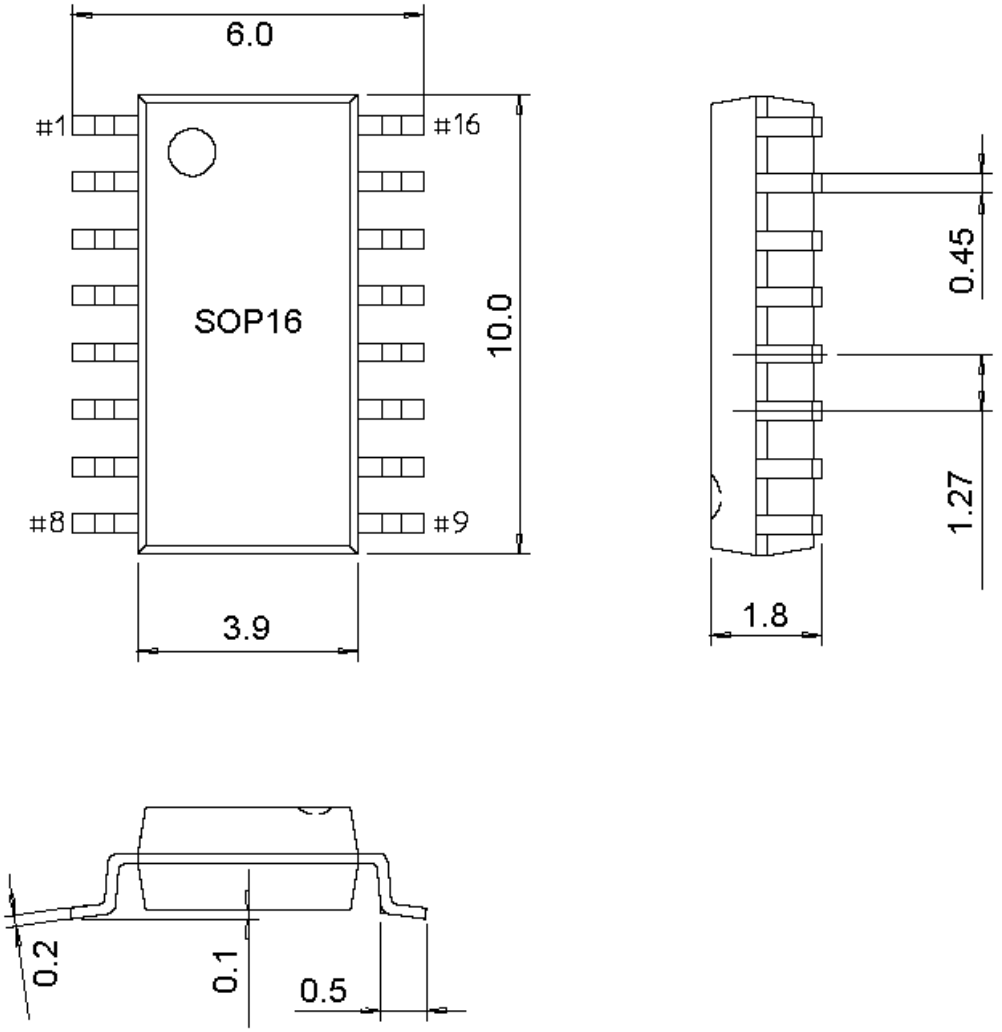
18.1 LQFP48-7*7



18.2 QFN28-4*4



18.3 SOP16-150mil



19. Revision History

Version	Date	Description
V1.0	June 21, 2018	Initial release
V1.1	November 8, 2018	Program routine file name deleted. VDD3 modified. INTX added.
V1.2	May 28, 2019	Register is renamed POWER_CFG. It is recommended to disable global interrupt during sleep. Note that V33 will be automatically shorted to VDD during sleep. Package information added.
V1.3	November 29, 2019	Typo in Section 12.3 corrected (PWM_CTRL). Typo in Section 15.4 corrected.
V1.4	October 21, 2021	bUEP_AUTO_TOG in Section 16.3 modified. System clock limited not more than 48MHz. Note that USB pins are not connected in series with external resistors.
V1.5	January 05, 2022	Expression optimized: Directly write 0 to reset, or write 1 to the corresponding bit in the register to reset.
V1.6	May 22, 2023	Fine-tune the current parameters for 17 sections, reserve a main frequency of 48MHz for new product design, and adjust MASK_ULLDO_VOL during deep sleep under 3.3V power supply.