8-bit Enhanced USB MCU CH549

Datasheet

Version: 1H

https://wch-ic.com

1. Overview

CH549 is an enhanced E8051 core microcontroller compatible with MCS51 instruction set. 79% of its instructions are single-byte single-cycle instructions, and the average instruction speed is 8 to 15 times faster than that of standard MCS51.

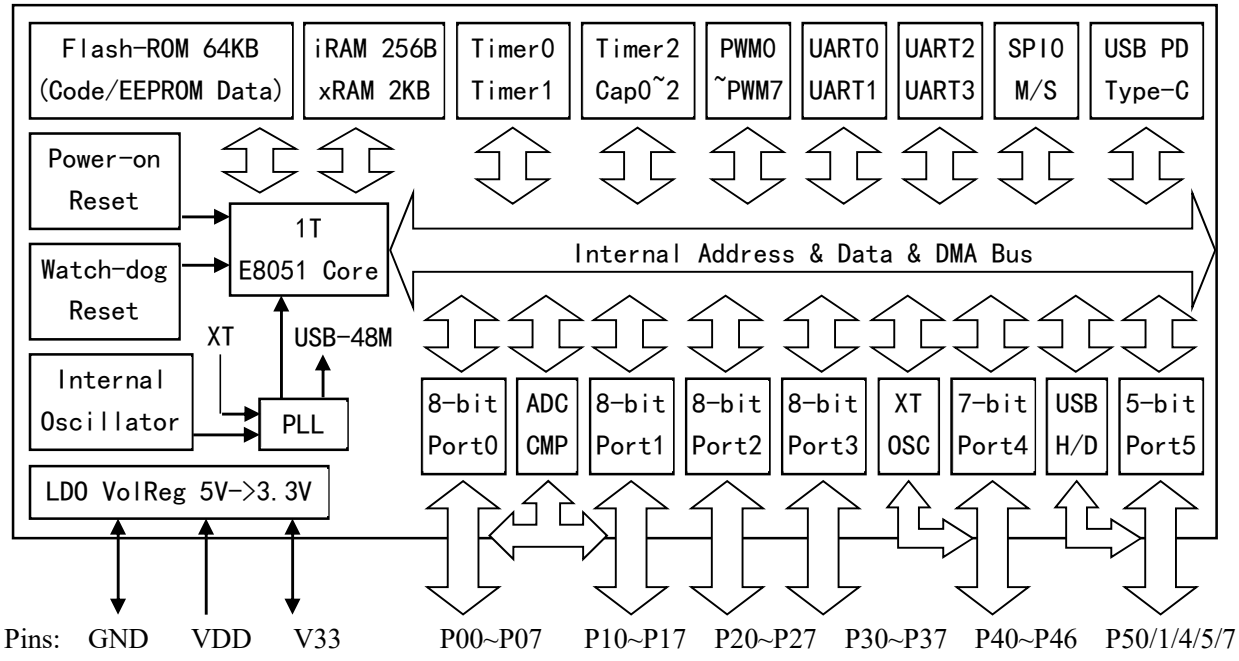
CH549 built-in 64K program memory Flash-ROM, 256byte internal iRAM and 2K byte on-chip xRAM. xRAM support DMA.

CH549 built-in 12-bit ADC, capacitive Touchkey detection, TS, built-in clock, 3 timers and 3-channel signal capture, 8-channel PWM, 4 UARTs, SPI and other functional modules. It supports full-speed and low-speed USB-Host mode and USB-Device mode as well as USB type-C. For complete PD functions, it is recommended to use CH543.

CH548 is the simplified version of CH549, program memory ROM is only 32KB. It only provides UART0 and UART1, others are the same as CH549. For details, directly refer to CH549 manuals and materials.

Model	Program ROM Boot ROM	xRAM iRAM	Nonvolatile EEPROM	USB host USB device	USB Type-C	Timer	Signal capture	8-bit PWM	UART	SPI Master /slave	12-bit ADC	Capacitive Touchkey
CH549	60KB+3KB	2048 +256	1KB	Full/ low-speed	Support	3	3	8	4	1	16	16
CH548	32KB+3KB								2			

The following is the internal block diagram of CH549, for reference only.

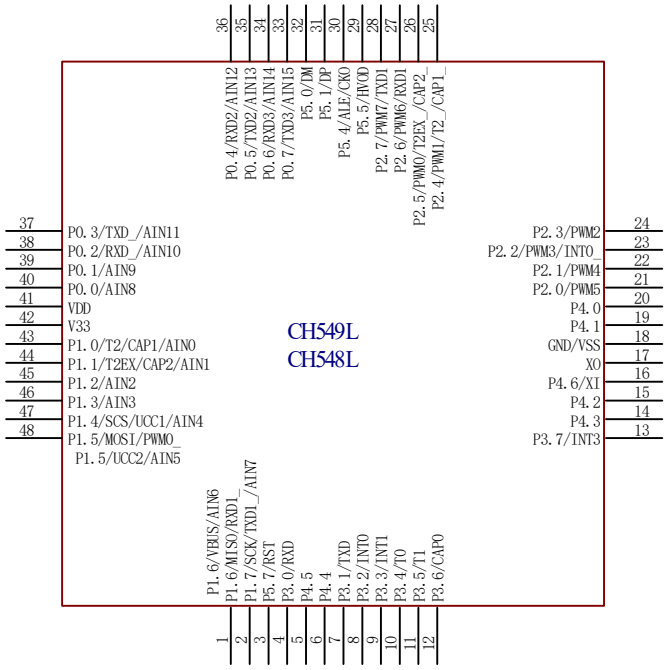


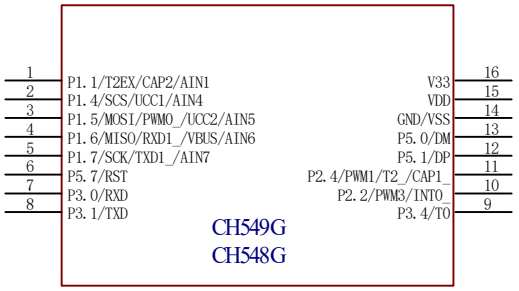
2. Features

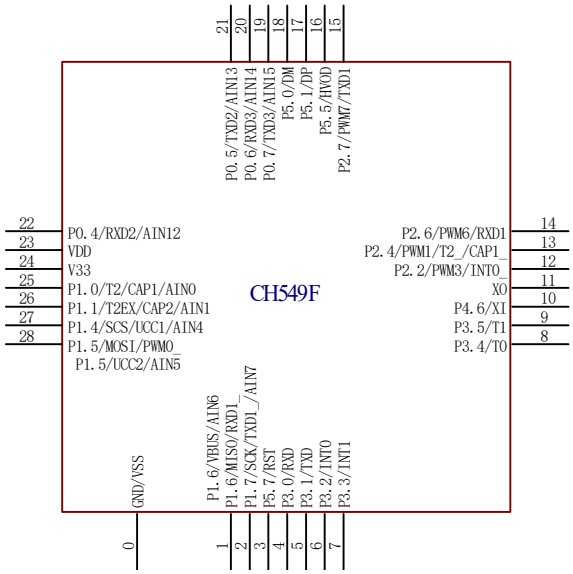
- Core: Enhanced E8051 core, compatible with MCS51 instruction set. 79% of its instructions are single-byte single-cycle instructions, the average instruction speed is 8 ~15 times faster than the standard MCS51, unique XRAM data fast copy instructions, double DPTR pointers.
- ROM: 64KB non-volatile memory Flash-ROM, supporting 10K erasures, can be used entirely for program storage space; or it can be divided into 60KB program storage area and 1KB data storage area EEPROM as well as 3KB boot code BootLoader/ISP program area.
- EEPROM: 1KB EEPROM, divided into 16 independent blocks. It supports single-byte read, single-byte write, block write (1~64 bytes) and block erase (64 bytes). In typical environments, 100K erases are generally supported (unguaranteed).
- OTP: One-time programmable data store OTP has a total of 32 bytes, supporting double-word reading (4 bytes) and single-byte writing.
- RAM: 256-byte internal iRAM, can be used for fast data temporary storage and stack; 2KB on-chip xRAM, can be used for a large number of data temporary storage and DMA direct memory access.
- USB: Built-in USB controller and USB transceiver, support USB-Host mode and USB-Device mode, support USB 2.0 full-speed 12Mbps or low-speed 1.5Mbps. Support up to 64-byte packets, built-in FIFO, DMA.
- USB type-C: Support USB type-C master-slave detection, USB PD power transmission control and 32-bit CRC calculation.
- Timer: 3 timers, the standard MCS51 timer T0/T1/T2.
- Capture: Timer T2 is extended to support 3-channel signal capture.
- PWM: 8-channel PWM output, supporting standard 8-bit data or fast 6-bit data.
- UART: 4 UARTs, UART0 is the standard MCS51 UART; UART1/2/3 has built-in communication baud rate setting register.
- SPI: SPI controller supports Master/Slave mode, built-in FIFO, clock frequency up to half of the system main frequency Fsys, and supports serial data input and output simplex.
- ADC: 16 channel 12-bit A/D converter, it supports multiple combinations of voltage comparisons.
- Touch-Key: 16-channel capacitive Touchkey detection. Each ADC channel supports Touchkey detection.
- TS: Built-in simple temperature sensor.
- GPIO: Support up to 44 GPIO pins (including XI, RST and USB pins), supporting MCS51 compatible quasi-bi-directional mode, and adds high-resistance input, push-pull output and open-drain output modes, one of which supports 12V high-voltage open-drain output.
- Interrupt: 16 interrupt sources, including 6 interrupts compatible with standard MCS51 (INT0, T0, INT1, T1, UART0, T2), and extended 10 interrupts (SPI0, INT3, USB, ADC/UART2, UART1, PWMX/UART3, GPIO, WDOG), of which GPIO interrupts can be selected from 7 pins.
- Watch-Dog: Based on 8-bit prescaler, supporting timing interrupt.
- Reset: 5 reset signal sources, built-in power-on reset and multi-stage adjustable power supply low-voltage detection reset module, software reset and watchdog overflow reset, optional pin external input reset.
- Clock: Built-in 24MHz clock source, external crystals can be supported by multiplexing GPIO pins, and built-in PLL is used to generate the USB clock and the system clock frequency Fsys of the desired frequency.
- Power: Built-in 5V to 3.3V low dropout voltage regulator for modules such as USB, supporting 5V or 3.3V, even 6V or 2.8V supply voltage.
- Sleep: Low-power sleep, USB, UART0, UART1, SPI0, comparator and some GPIO external wake-up.
- Unique ID number, which supports ID number and check.

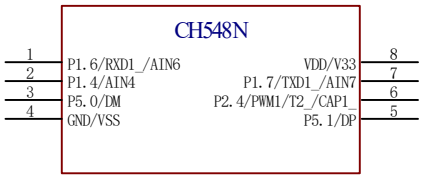
3. Packages

Package form	Shaping width		Pin spacing		Description	Order model
LQFP48	7*7mm		0.5mm	19.7mil	Low-profile Quad Flat Package	CH549L
QFN28_4×4	4*4mm		0.4mm	15.7mil	Quad Flat No-Lead Package	CH549F
SOP16	3.9mm	150mil	1.27mm	50mil	Small Outline Package	CH549G
LQFP48	7*7mm		0.5mm	19.7mil	Low-profile Quad Flat Package	CH548L
SOP16	3.9mm	150mil	1.27mm	50mil	Small Outline Package	CH548G
SOP8	3.9mm	150mil	1.27mm	50mil	Small Outline Package	CH548N









4. Pin Definitions

Pin No.			Pin name	Other functions (Left function is the top priority.)	Other function description
SOP16	QFN28	LQFP48			
15	23	41	VDD	VCC	I/O power input and the external power input of internal USB power regulator require an external 0.1uF power decoupling capacitor.
16	24	42	V33	V3	Internal USB power regulator output and internal USB power input. When the power supply voltage is less than 3.6V, connect the VDD input external power supply. When the power supply voltage is greater than 3.6V, external 0.1uF power supply decoupling capacitor.
14	0	18	GND	VSS	Ground
-	-	40	P0.0	AIN8	AIN8~AIN15: 8 channel ADC analog signal / touch key input. RXD_, TXD_: RXD, TXD pin mapping. RXD2, TXD2: UART2 serial data input, serial data output. RXD3, TXD3: UART3 serial data input, serial data output.
-	-	39	P0.1	AIN9	
-	-	38	P0.2	RXD_/AIN10	
-	-	37	P0.3	TXD_/AIN11	
-	22	36	P0.4	RXD2/AIN12	
-	21	35	P0.5	TXD2/AIN13	
-	20	34	P0.6	RXD3/AIN14	
-	19	33	P0.7	TXD3/AIN15	
-	25	43	P1.0	T2/CAP1/AIN0	AIN0 to AIN7: 8-channel ADC analog signal/touch key input. T2: External count input/clock output for Timer/Counter 2. T2EX: Timer/Counter2 reload/capture input. CAP1, CAP2: Timer/Counter 2 capture inputs 1 and 2. SCS, MOSI, MISO, SCK: SPI0 interface, SCS is the chip select input, MOSI is the host output/slave input, MISO is the host input/slave output, SCK is the serial clock. UCC1, UCC2: USB type-C bidirectional configuration channel. VBUS: USB type-C bus voltage detection input. PWM0_, RXD1_, TXD1_: PWM0/RXD1/TXD1 pin mapping.
1	26	44	P1.1	T2EX/CAP2/AIN1	
-	-	45	P1.2	AIN2	
-	-	46	P1.3	AIN3	
2	27	47	P1.4	SCS/UCC1/AIN4	
3	28	48	P1.5	MOSI/PWM0_/UCC2/AIN5	
4	1	1	P1.6	MISO/RXD1_/VBUS/AIN6	
5	2	2	P1.7	SCK/TXD1_/AIN7	
-	-	21	P2.0	PWM5	PWM0~PWM7: 8 channel PWM output. INT0_: INT0 pin mapping. T2_/CAP1_: T2/CAP1 pin mapping. T2EX_/CAP2_: T2EX/CAP2 pin mapping. RXD1, TXD1: UART1 serial data input, serial data output.
-	-	22	P2.1	PWM4	
10	12	23	P2.2	PWM3/INT0_	
-	-	24	P2.3	PWM2	
11	13	25	P2.4	PWM1/T2_/CAP1_	
-	-	26	P2.5	PWM0/T2EX_/CAP2_	
-	14	27	P2.6	PWM6/RXD1	

-	15	28	P2.7	PWM7/TXD1	
7	4	4	P3.0	RXD	RXD, TXD: UART0 serial data input, serial data output. INT0, INT1: External interrupt 0, external interrupt 1 input. T0, T1: Timer0, Timer1 external input. CAP0: Timer/counter 2 capture input 0. INT3: External interrupt 3.
8	5	7	P3.1	TXD	
-	6	8	P3.2	INT0	
-	7	9	P3.3	INT1	
9	8	10	P3.4	T0	
-	9	11	P3.5	T1	
-	-	12	P3.6	CAP0	
-	-	13	P3.7	INT3	
-	-	20	P4.0		XI, XO: External crystal oscillation input, inverse output.
-	-	19	P4.1		
-	-	15	P4.2		
-	-	14	P4.3		
-	-	6	P4.4		
-	-	5	P4.5		
-	10	16	P4.6	XI	
-	11	17	XO		
13	18	32	P5.0	DM/UDM	DM, DP: The D-and D+ signal end of the USB host or USB device. The resistors are fully built-in, so it is recommended that the external resistors are no longer in series.
12	17	31	P5.1	DP/UDP	
-	-	30	P5.4	ALE/CKO	ALE/CKO: Pseudo-address latch signal output or clock output. HVOD: Support 12V high voltage open-drain output.
-	16	29	P5.5	HVOD	
6	3	3	P5.7	RST	External reset input, built-in pull-down resistor.

Note: CH548N VDD and V33 have been shorted internally, VDD can only 3V~3.6V when using USB, 2.7V~6.5V when USB is not used.

5. Special Function Register

The following abbreviations may be used to describe registers in this manual:

Acronym	Description
RO	Indicate access type: read-only
WO	Indicate access type: write-only, invalid value read
RW	Indicate access type: readable and writable
H	End with it indicates hexadecimal number.
B	End with it indicates binary number.

5.1 SFR Introduction and Address Distribution

CH549 uses special function registers SFR and xSFR to control, manage devices and set operating modes.

SFR occupies the 80h-FFh address range of internal data storage space and can only be accessed through direct address instructions. Registers with addresses of x0h or x8h can be addressed by bits, so as to avoid modifying the values of other bits when accessing a specific bit; registers with non-8x addresses can only be accessed by bytes.

Some SFR can write data only in safe mode, but read-only in non-safe mode, such as GLOBAL_CFG,

CLOCK_CFG, WAKE_CTRL, POWER_CFG.

Some SFR have one or more aliases, for example: SPI0_CK_SE/SPI0_S_PRE、UDEV_CTRL/UHOST_CTRL、UEP1_CTRL/UH_SETUP, UEP2_CTRL/UH_RX_CTRL, UEP2_T_LEN/UH_EP_PID, UEP3_CTRL/UH_TX_CTRL, UEP3_T_LEN/UH_TX_LEN, UEP2_3_MOD/UH_EP_MOD, UEP2_DMA_H/UH_RX_DMA_H, UEP2_DMA_L/UH_RX_DMA_L, UEP2_DMA/UH_RX_DMA, UEP3_DMA_H/UH_TX_DMA_H, UEP3_DMA_L/UH_TX_DMA_L, UEP3_DMA/UH_TX_DMA, ROM_ADDR_L/ROM_DATA_LL, ROM_ADDR_H/ROM_DATA_LH, ROM_DATA_HL/ROM_DAT_BUF, ROM_DATA_HH/ROM_BUF_MOD.

Some addresses correspond to multiple independent SFR, for example: SAFE_MOD/CHIP_ID, ROM_CTRL/ROM_STATUS.

CH549 contains all the registers of the 8051 standard SFR, while adding other device control registers. SFR details are shown in the table below.

Table 5.1 Table of special function registers

SFR	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F
0xF8	SPI0_STAT	SPI0_DATA	SPI0_CTRL	SPI0_CK_SE SPI0_S_PRE	SPI0_SETUP	A_INV	RESET_KEEP	WDOG_COUNT
0xF0	B	TKEY_CTRL	ADC_CTRL	ADC_CFG	ADC_DAT_L	ADC_DAT_H	ADC_CHAN	ADC_PIN
0xE8	IE_EX	IP_EX	UEP4_1_MOD	UEP2_3_MOD UH_EP_MOD	UEP0_DMA_L	UEP0_DMA_H	UEP1_DMA_L	UEP1_DMA_H
0xE0	ACC	USB_INT_EN	USB_CTRL	USB_DEV_AD	UEP2_DMA_L UH_RX_DMA_L	UEP2_DMA_H UH_RX_DMA_H	UEP3_DMA_L UH_TX_DMA_L	UEP3_DMA_H UH_TX_DMA_H
0xD8	USB_INT_FG	USB_INT_ST	USB_MIS_ST	USB_RX_LEN	UEP0_CTRL	UEP0_T_LEN	UEP4_CTRL	UEP4_T_LEN
0xD0	PSW	UDEV_CTRL UHOST_CTRL	UEP1_CTRL UH_SETUP	UEP1_T_LEN	UEP2_CTRL UH_RX_CTRL	UEP2_T_LEN UH_EP_PID	UEP3_CTRL UH_TX_CTRL	UEP3_T_LEN UH_TX_LEN
0xC8	T2CON	T2MOD	RCAP2L	RCAP2H	TL2	TH2	T2CAP1L	T2CAP1H
0xC0	P4	T2CON2	P4_MOD_OC	P4_DIR_PU	P0_MOD_OC	P0_DIR_PU	T2CAP0L	T2CAP0H
0xB8	IP	CLOCK_CFG	POWER_CFG		SCON1	SBUF1	SBAUD1	SIF1
0xB0	P3	GLOBAL_CFG	GPIO_IE	INTX	SCON2	SBUF2	SBAUD2	SIF2
0xA8	IE	WAKE_CTRL	PIN_FUNC	P5	SCON3	SBUF3	SBAUD3	SIF3
0xA0	P2	SAFE_MOD CHIP_ID	XBUS_AUX	PWM_DATA3	PWM_DATA4	PWM_DATA5	PWM_DATA6	PWM_DATA7

0x98	SCON	SBUF	PWM_DATA2	PWM_DATA1	PWM_DATA0	PWM_CTRL	PWM_CK_SE	PWM_CTRL2
0x90	P1	USB_C_CTRL	P1_MOD_OC	P1_DIR_PU	P2_MOD_OC	P2_DIR_PU	P3_MOD_OC	P3_DIR_PU
0x88	TCON	TMOD	TL0	TL1	TH0	TH1	ROM_DATA_HL ROM_DAT_BUF	ROM_DATA_HH ROM_BUF_MOD
0x80	P0	SP	DPL	DPH	ROM_ADDR_L ROM_DATA_LL	ROM_ADDR_H ROM_DATA_LH	ROM_CTRL ROM_STATUS	PCON

Note:

(1) The red text indicates that it can be addressed by bit;

(2) The following is the description of the color box

	Register address
	SPI0 related register
	ADC related register
	USB related register
	Timing / counter 2 related register
	Port setting related register
	PWMX related register
	UART1/2/3 related register
	Timing / counter 0 and 1 related register
	Flash-ROM related register

5.2 SFR Classification and Reset Value

Table 5.2 Description and reset value of SFR and xSFR

Function	Name	Address	Description	Reset value
System setting related registers	B	F0h	B register	0000 0000b
	ACC	E0h	Accumulator	0000 0000b
	A_INV	FDh	High and low inverted value of accumulator	0000 0000b
	PSW	D0h	Program status register	0000 0000b
	GLOBAL_CFG	B1h	Global configuration register (CH549 Bootloader)	1110 0000b
			Global configuration register (CH549 application)	1100 0000b
			Global configuration register (CH548 Bootloader)	1010 0000b
			Global configuration register (CH548 application)	1000 0000b
	CHIP_ID	A1h	CH549 chip ID identification code (read-only)	0100 1001b
			CH548 chip ID identification code (read-only)	0100 1000b
	SAFE_MOD	A1h	Safe mode control register (write-only)	0000 0000b
	DPH	83h	Data address pointer high 8 bits	0000 0000b
	DPL	82h	Data address pointer low 8 bits	0000 0000b
	DPTR	82h	16-bit SFR consists of DPL and DPH	0000h

	SP	81h	Stack pointer	0000 0111b
Clock, sleep and power control related registers	WDOG_COUNT	FFh	Watchdog count register	0000 0000b
	RESET_KEEP	FEh	Reset keep register (power on reset)	0000 0000b
	POWER_CFG	BAh	Power management configuration register	0000 0xxxb
	CLOCK_CFG	B9h	System clock configuration register	1000 0011b
	WAKE_CTRL	A9h	Wake-up control register	0000 0000b
	PCON	87h	Power control register (power on reset)	0001 0000b
Interrupt control related registers	IP_EX	E9h	Extended interrupt priority control register	0000 0000b
	IE_EX	E8h	Extended interrupt enable register	0000 0000b
	GPIO_IE	C7h	GPIO interrupt enable register	0000 0000b
	IP	B8h	Interrupt priority control register	0000 0000b
	INTX	B3h	Extended external interrupt control register	0000 0000b
	IE	A8h	Interrupt enable register	0000 0000b
Flash-ROM related registers	ROM_DATA_HH	8Fh	High bytes of high words in flash-ROM data register (read-only)	xxxx xxxxb
	ROM_DATA_HL	8Eh	Low bytes of high words in flash-ROM data register (read-only)	xxxx xxxxb
	ROM_DATA_HI	8Eh	16-bit SFR consists of ROM_DATA_HL and ROM_DATA_HH	xxxxh
	ROM_BUF_MOD	8Fh	Buffer mode register for flash-ROM erase and write operations	xxxx xxxxb
	ROM_DAT_BUF	8Eh	Data buffer register for flash-ROM erase and write operations	xxxx xxxxb
	ROM_STATUS	86h	flash-ROM status register (read only)	0000 0000b
	ROM_CTRL	86h	flash-ROM control register (write only)	0000 0000b
	ROM_ADDR_H	85h	flash-ROM address register high	xxxx xxxxb
	ROM_ADDR_L	84h	flash-ROM address register low	xxxx xxxxb
	ROM_ADDR	84h	16-bit SFR consists of ROM_ADDR_L and ROM_ADDR_H	xxxxh
	ROM_DATA_LH	85h	High bytes of low words in flash-ROM data register (read-only)	xxxx xxxxb
	ROM_DATA_LL	84h	Low bytes of low words in flash-ROM data register (read-only)	xxxx xxxxb
	ROM_DATA_LO	84h	16-bit SFR consists of ROM_DATA_LL and ROM_DATA_LH	xxxxh
Port setting related registers	XBUS_AUX	A2h	External bus auxiliary setting register	0000 0000b
	PIN_FUNC	AAh	Pin function selection register	0000 0000b
	P0_DIR_PU	C5h	P0 port direction control and pull-up enable register	1111 1111b
	P0_MOD_OC	C4h	P0 port output mode register	1111 1111b
	P4_DIR_PU	C3h	P4 port direction control and pull-up enable register	1111 1111b
	P4_MOD_OC	C2h	P4 port output mode register	1111 1111b

	P3_DIR_PU	97h	P3 port direction control and pull-up enable register	1111 1111b
	P3_MOD_OC	96h	P3 port output mode register	1111 1111b
	P2_DIR_PU	95h	P2 port direction control and pull-up enable register	1111 1111b
	P2_MOD_OC	94h	P2 port output mode register	1111 1111b
	P1_DIR_PU	93h	P1 port direction control and pull-up enable register	1111 1111b
	P1_MOD_OC	92h	P1 port output mode register	1111 1111b
	P5	ABh	P5 port input and output register	0010 0000b
	P4	C0h	P4 port input and output register	1111 1111b
	P3	B0h	P3 port input and output register	1111 1111b
	P2	A0h	P2 port input and output register	1111 1111b
	P1	90h	P1 port input and output register	1111 1111b
	P0	80h	P0 port input and output register	1111 1111b
Timing/counter 0 and 1 related registers	TH1	8Dh	Timer1 count high	xxxx xxxxb
	TH0	8Ch	Timer0 count high	xxxx xxxxb
	TL1	8Bh	Timer1 count low	xxxx xxxxb
	TL0	8Ah	Timer0 count low	xxxx xxxxb
	TMOD	89h	Timer0/1 mode register	0000 0000b
	TCON	88h	Timer0/1 control register	0000 0000b
UART0 related registers	SBUF	99h	UART0 data register	xxxx xxxxb
	SCON	98h	UART0 control register	0000 0000b
Timing/counter 2 related registers	T2CAP1H	CFh	Timer2 captures 1 high bytes of data (read-only)	xxxx xxxxb
	T2CAP1L	CEh	Timer2 captures 1 low bytes of data (read-only)	xxxx xxxxb
	T2CAP1	CEh	16-bit SFR consists of T2CAP1L and T2CAP1H	xxxxh
	TH2	CDh	Timer2 counter high	0000 0000b
	TL2	CCh	Timer2 counter low	0000 0000b
	T2COUNT	CCh	16-bit SFR consists of T2CAP2L and T2CAP2H	0000h
	RCAP2H	CBh	Count reload/capture 2 data register high	0000 0000b
	RCAP2L	CAh	Count reload/capture 2 data register low	0000 0000b
	RCAP2	CAh	16-bit SFR consists of RCAP2L and RCAP2H	0000h
	T2MOD	C9h	Timer2 mode register	0000 0000b
	T2CON	C8h	Timer2 control register	0000 0000b
	T2CAP0H	C7h	Timer2 captures 0 data high (read-only)	xxxx xxxxb
	T2CAP0L	C6h	Timer2 captures 0 data low (read-only)	xxxx xxxxb
	T2CAP0	C6h	16-bit SFR consists of T2CAP0L and T2CAP0H	xxxxh
	T2CON2	C1h	Timer2 extended control register	0000 0000b
PWMX related registers	PWM_DATA7	A7h	PWM7 data register	xxxx xxxxb
	PWM_DATA6	A6h	PWM6 data register	xxxx xxxxb
	PWM_DATA5	A5h	PWM5 data register	xxxx xxxxb
	PWM_DATA4	A4h	PWM4 data register	xxxx xxxxb
	PWM_DATA3	A3h	PWM3 data register	xxxx xxxxb

	PWM_CTRL2	9Fh	PWM extended control register	0000 0000b
	PWM_CK_SE	9Eh	PWM clock frequency division setting register	0000 0000b
	PWM_CTRL	9Dh	PWM control register	0000 0010b
	PWM_DATA0	9Ch	PWM0 data register	xxxx xxxxb
	PWM_DATA1	9Bh	PWM1 data register	xxxx xxxxb
	PWM_DATA2	9Ah	PWM2 data register	xxxx xxxxb
SPI0 related registers	SPI0_SETUP	FCh	SPI0 setting register	0000 0000b
	SPI0_S_PRE	FBh	SPI0 slave mode preset data register	0010 0000b
	SPI0_CK_SE	FBh	SPI0 clock frequency division setting register	0010 0000b
	SPI0_CTRL	FAh	SPI0 control register	0000 0010b
	SPI0_DATA	F9h	SPI0 data transceiver register	xxxx xxxxb
	SPI0_STAT	F8h	SPI0 status register	0000 1000b
UART1 related registers	SIF1	BFh	UART1 interrupt status register	0000 0000b
	SBAUD1	BEh	UART1 baud rate setting register	xxxx xxxxb
	SBUF1	BDh	UART1 data register	xxxx xxxxb
	SCON1	BCh	UART1 control register	0100 0000b
UART2 related registers	SIF2	B7h	UART2 interrupt status register	0000 0000b
	SBAUD2	B6h	UART2 baud rate setting register	xxxx xxxxb
	SBUF2	B5h	UART2 data register	xxxx xxxxb
	SCON2	B4h	UART2 control register	0000 0000b
UART3 related registers	SIF3	AFh	UART3 interrupt status register	0000 0000b
	SBAUD3	AEh	UART3 baud rate setting register	xxxx xxxxb
	SBUF3	ADh	UART3 data register	xxxx xxxxb
	SCON3	ACh	UART3 control register	0000 0000b
ADC/TKEY related registers	ADC_PIN	F7h	ADC pin digital input control register	0000 0000b
	ADC_CHAN	F6h	ADC analog signal channel selection register	0000 0000b
	ADC_DAT_H	F5h	High bytes of ADC result data (read only)	0000 xxxxb
	ADC_DAT_L	F4h	Low bytes of ADC result data (read only)	xxxx xxxxb
	ADC_DAT	F4h	16-bit SFR consists of ADC_DAT_L and ADC_DAT_H	0xxxh
	ADC_CFG	F3h	ADC configuration register	0000 0000b
	ADC_CTRL	F2h	ADC control and status register	x000 000xb
	TKEY_CTRL	F1h	Touch button charging pulse width control register (write only)	0000 0000b
USB related registers	UEP1_DMA_H	EFh	Endpoint 1 buffer start address high byte	0000 0xxxb
	UEP1_DMA_L	EEh	Endpoint 1 buffer start address low byte	xxxx xxxxb
	UEP1_DMA	EEh	16-bit SFR consists of UEP1_DMA_L and UEP1_DMA_H	0xxxh
	UEP0_DMA_H	EDh	Endpoint 0/4 buffer start address high byte	0000 0xxxb
	UEP0_DMA_L	ECh	Endpoint 0/4 buffer start address low byte	xxxx xxxxb
	UEP0_DMA	ECh	16-bit SFR consists of UEP0_DMA_L and UEP0_DMA_H	0xxxh
	UEP2_3_MOD	EBh	Endpoint 2/3 mode control register	0000 0000b

	UH_EP_MOD	EBh	USB host endpoint mode control register	0000 0000b
	UEP4_1_MOD	EAh	Endpoint 1/4 mode control register	0000 0000b
	UEP3_DMA_H	E7h	Endpoint 3 buffer start address high byte	0000 0xxxb
	UEP3_DMA_L	E6h	Endpoint 3 buffer start address low byte	xxxx xxxxb
	UEP3_DMA	E6h	16-bit SFR consists of UEP3_DMA_L and UEP3_DMA_H	0xxxh
	UH_TX_DMA_H	E7h	USB host transmit buffer start address high byte	0000 0xxxb
	UH_TX_DMA_L	E6h	USB host transmit buffer start address low byte	xxxx xxxxb
	UH_TX_DMA	E6h	16-bit SFR consists of UH_TX_DMA_L and UH_TX_DMA_H	0xxxh
	UEP2_DMA_H	E5h	Endpoint 2 buffer start address high byte	0000 0xxxb
	UEP2_DMA_L	E4h	Endpoint 2 buffer start address low byte	xxxx xxxxb
	UEP2_DMA	E4h	16-bit SFR consists of UEP2_DMA_L and UEP2_DMA_H	0xxxh
	UH_RX_DMA_H	E5h	USB host receive buffer start address high byte	0000 0xxxb
	UH_RX_DMA_L	E4h	USB host receive buffer start address low byte	xxxx xxxxb
	UH_RX_DMA	E4h	16-bit SFR consists of UH_RX_DMA_L and UH_RX_DMA_H	0xxxh
	USB_DEV_AD	E3h	USB device address register	0000 0000b
	USB_CTRL	E2h	USB control register	0000 0110b
	USB_INT_EN	E1h	USB interrupt enable register	0000 0000b
	UEP4_T_LEN	DFh	Endpoint 4 transmit length register	0xxx xxxxb
	UEP4_CTRL	DEh	Endpoint 4 control register	0000 0000b
	UEP0_T_LEN	DDh	Endpoint 0 transmit length register	0xxx xxxxb
	UEP0_CTRL	DCh	Endpoint 0 control register	0000 0000b
	USB_RX_LEN	DBh	USB receive length register (read-only)	0xxx xxxxb
	USB_MIS_ST	DAh	USB miscellaneous status Register (read-only)	xx10 1000b
	USB_INT_ST	D9h	USB interrupt status register (read-only)	00xx xxxxb
	USB_INT_FG	D8h	USB interrupt flag register	0010 0000b
	UEP3_T_LEN	D7h	Endpoint 3 transmit length register	0xxx xxxxb
	UH_TX_LEN	D7h	USB host transmit length register	0xxx xxxxb
	UEP3_CTRL	D6h	Endpoint 3 control register	0000 0000b
	UH_TX_CTRL	D6h	USB host transmit endpoint control register	0000 0000b
	UEP2_T_LEN	D5h	Endpoint 2 transmit length register	0000 0000b
	UH_EP_PID	D5h	USB host token setting register	0000 0000b
	UEP2_CTRL	D4h	Endpoint 2 control register	0000 0000b
	UH_RX_CTRL	D4h	USB host receive endpoint control register	0000 0000b
	UEP1_T_LEN	D3h	Endpoint 2 transmit length register	0xxx xxxxb
	UEP1_CTRL	D2h	Endpoint 1 control register	0000 0000b
	UH_SETUP	D2h	USB host auxiliary setting register	0000 0000b
	UDEV_CTRL	D1h	USB device port control register	00xx 0000b
	UHOST_CTRL	D1h	USB host port control register	00xx 0000b
	USB_C_CTRL	91h	USB type-C configuration channel control	0000 0000b

			register	

5.3 General-purpose 8051 Register

Table 5.3.1 List of general-purpose 8051 registers

Name	Address	Description	Reset value
A_INV	FDh	High and low inverted value of accumulator	00h
B	F0h	B register	00h
A、ACC	E0h	Accumulator	00h
PSW	D0h	Program status register	00h
GLOBAL_CFG	B1h	Global configuration register (CH549 Bootloader)	E0h
		Global configuration register (CH549 application)	C0h
		Global configuration register (CH548 Bootloader)	A0h
		Global configuration register (CH548 application)	80h
CHIP_ID	A1h	CH549 chip ID identification code (read-only)	49h
		CH548 chip ID identification code (read-only)	48h
SAFE_MOD	A1h	Safe mode control register (write-only)	00h
PCON	87h	Power control register (power on reset)	10h
DPH	83h	Data address pointer high 8 bits	00h
DPL	82h	Data address pointer low 8 bits	00h
DPTR	82h	16-bit SFR consists of DPL and DPH	0000h
SP	81h	Stack pointer	07h

B Register (B):

Bit	Name	Access	Description	Reset value
[7:0]	B	RW	Arithmetic register, mainly used for multiplication and division operations, bit-addressable.	00h

A accumulator (A, ACC):

Bit	Name	Access	Description	Reset value
[7:0]	A/ACC	RW	Arithmetic accumulator, bitwise addressable	00h

Program status register (PSW):

Bit	Name	Access	Description	Reset value
7	CY	RW	Carry mark: When performing arithmetic and logical operation instructions, it is used to record the carry or borrow of the highest bit; when performing an 8-bit addition operation, the highest bit carries, the position is otherwise cleared; when performing an 8-bit subtraction operation, if it is borrowed, the position is otherwise cleared; the logic instruction can make the position or zero.	0
6	AC	RW	Auxiliary carry mark bit: When recording the addition and subtraction operation, there are carry or borrow from the lower 4	0

			bits to the higher 4 bits, AC setting, otherwise zero	
5	F0	RW	Bit-addressable universal flag bit 0: The user can define it by himself and can be cleared or set by software.	0
4	RS1	RW	Register bank selection bit high bit	0
3	RS0	RW	Register bank selection bit low bit	0
2	OV	RW	Overflow flag bit: When the addition and subtraction operation, the result of the operation exceeds 8 binary digits, then OV is set to 1, and the flag overflows, otherwise 0	0
1	F1	RW	Bit-addressable universal flag bit 1: The user can define it and can be zeroed or set by software	0
0	P	RO	Parity flag bit: Record the parity of 1 in accumulator An after instruction execution, odd 1 means P setting, even 1 means P clear zero	0

The state of the processor is stored in the state register PSW, and PSW supports bit-by-bit addressing. The status word includes carry flag bits, auxiliary carry flag bits for BCD code processing, parity flag bits, overflow flag bits, and RS0 and RS1 for working register group selection. The area where the working register group is located can be accessed directly or indirectly.

Table 5.3.2 RS1 and RS0 operating register group selection table

RS1	RS0	Operating register group
0	0	0 group (00h-07h)
0	1	1 group (08h-0Fh)
1	0	2 group (10h-17h)
1	1	3 group (18h-1Fh)

Table 5.3.3 Affects the operation of flag bits (X indicates that flag bits are related to the result of the operation)

Operation	CY	OV	AC	Operation	CY	OV	AC
ADD	X	X	X	SETB C	1		
ADDC	X	X	X	CLR C	0		
SUBB	X	X	X	CPL C	X		
MUL	0	X		MOV C, bit	X		
DIV	0	X		ANL C, bit	X		
DA A	X			ANL C,/bit	X		
RRC A	X			ORL C, bit	X		
RLC A	X			ORL C,/bit	X		
CJNE	X						

Data address pointer (DPTR):

Bit	Name	Access	Description	Reset value
[7:0]	DPL	RW	Data pointer low byte	00h
[7:0]	DPH	RW	Data pointer high byte	00h

DPL and DPH form a 16-bit data pointer DPTR, which is used to access xSFR, xBUS, xRAM data memory or program memory. The actual DPTR corresponds to two groups of physical 16-bit data pointers in DPTR0 and DPTR1, which are dynamically selected by DPS in XBUS_AUX.

Stack pointer (SP):

Bit	Name	Access	Description	Reset value
[7:0]	SP	RW	Stack pointer, mainly used for program calls and interrupt calls as well as data in and out of the stack	07h

Stack specific functions: protect breakpoints and protect the site, according to the first-in-first-out principle of management. When entering the stack, the SP pointer is automatically added to save data or breakpoint information; when leaving the stack, the SP pointer is taken to point to the data unit, and the SP pointer is automatically minus 1. The initial value of SP after reset is 07h, and the corresponding default stack storage starts at 08h.

5.4 Unique Register

High and Low Inverted Values of the Accumulator (A_INV):

Bit	Name	Access	Description	Reset value
[7:0]	A_INV	RO	The inverted values of the high and low bits of the accumulator, the result of the reverse order of bit 0 ~ bit 7 of A_INV, bit 7 and bit 6 ~ 0 of ACC are bit 0 and bit 1 ~ 7, respectively.	00h

Global Configuration Register (GLOBAL_CFG), which is writable only in safe mode:

Bit	Name	Access	Description	Reset value
[7:6]	Reserved	RO	For CH549, a fixed value of 11	11b
[7:6]	Reserved	RO	For CH548, a fixed value of 10	10b
5	bBOOT_LOAD	RO	Bootloader status bit, which is used to distinguish the ISP bootstrapper state or the application state: set 1 when the power is powered on and clear 0 when the software is reset. For a chip with an ISP bootstrapper, the bit 1 indicates that it has never been reset by software, and it is usually the state of the ISP bootstrap that runs after power is powered on; a bit of 0 indicates that it has been reset by software, usually the state of the application.	1
4	bSW_RESET	RW	Software reset control bit: Setting 1 causes software reset and hardware automatic zeroing	0
3	bCODE_WE	RW	Flash-ROM write allowed bit: If this bit is 0, it is write protected; if it is 1, Flash-ROM is writable and erasable	0
2	bDATA_WE	RW	Write allowed bit in DataFlash area of Flash-ROM: If this bit is 0, write-protected; if 1, DataFlash area is writable and erasable	0
1	Reserved	RO		0
0	bWDOG_EN	RW	Watchdog reset enable bit: This bit is 0 watchdog can only be used as timer; this bit 1 allows watchdog reset when timing overflows	0

Chip ID Identification Code (CHIP_ID):

Bit	Name	Access	Description	Reset value
[7:0]	CHIP_ID	RO	For CH549, the fixed value is 49h, which is used to identify the chip.	49h
[7:0]	CHIP_ID	RO	For CH548, the fixed value is 48h, which is used to identify the chip.	48h

Safe Mode Control Register (SAFE_MOD):

Bit	Name	Access	Description	Reset value
[7:0]	SAFE_MOD	WO	Used to enter or terminate safe mode	00h

Some SFR can only write data in safe mode, while it is always read-only in non-safe mode. Steps to enter safe mode:

(1) Write to the register for 55 hours

(2) Then write AAh

(3) Since then, about 13 to 23 main frequency cycles of the system are in safe mode, and one or more security classes SFR or ordinary SFR can be rewritten during the validity period.

(4) Automatically terminate the security mode after the expiration of the above validity period

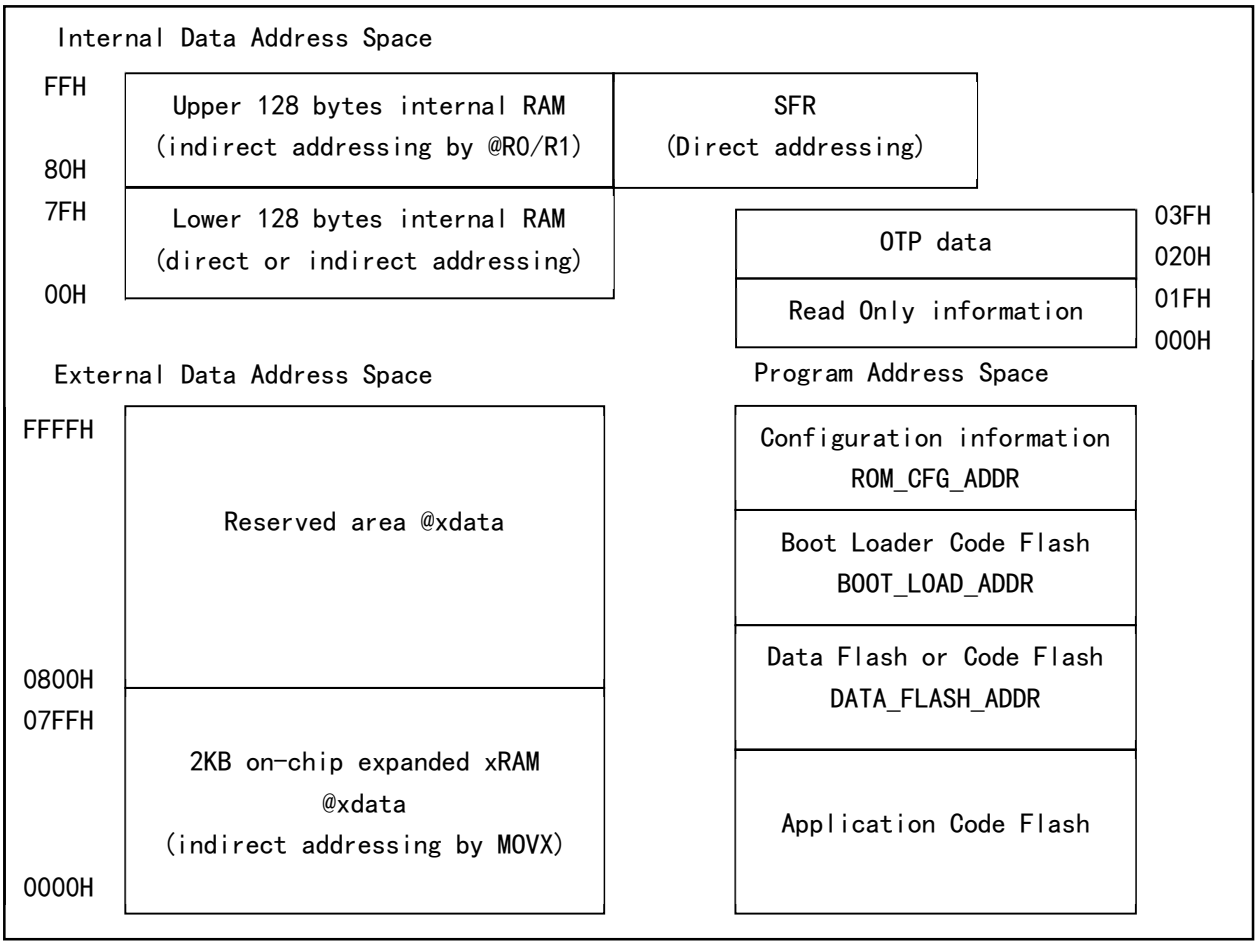
(5) Or write any value to the register to terminate the safe mode in advance.

6. Memory Structure

6.1 Memory Space

CH549 addressing space is divided into program storage space, internal data storage space, external data storage space, read-only space and OTP space.

Figure 6.1 Memory structure diagram



6.2 Program Memory Space

The total storage space of the program is 64KB, which is all used for flash-ROM, including the Code Flash area where the instruction code is saved, the Data Flash area where the non-volatile data is stored, and the Configuration Information area of the configuration information.

Data Flash (EEPROM) addresses range from F000h to F3FFH, and supports single-byte read (8-bit), single-byte write (8-bit), block write (1'64 bytes) and block erase (64 bytes). The data remains unchanged after the chip is powered off, and can also be used as a Code Flash.

Code Flash includes application code for low-address areas and bootstrap code for high-address areas, which can also be combined with Data Flash to save a single application code.

For the application code area of CH548, Code Flash, only 32KB.

The configuration information Configuration Information has a total of 16 bits of data, which is set by the programmer as needed, referring to Table 6.2.

Table 6.2 Description of flash-ROM configuration information

Bit address	Bit name	Description	Recommended value

15	Code_Protect	Code and data protection mode in flash-ROM: 0-allow read; 1-disable programmer read, program secret	0/1
14	No_Boot_Load	Enable BootLoader boot code boot mode: 0-start from the application at 0000h address; 1-start from the Bootloader at F400h address	1
13	En_Long_Reset	Additional delayed reset during enable power-on reset: 0-standard short reset, 1-wide reset, additional 44mS reset time	0
12	En_P5.7_RESET	Enable P5.7 as manual reset input pin: 0-disable; 1-enable RST	1
11		Reserved	0
10		Reserved	0
9	Must_1	(Automatically set to 1 by the programmer as needed)	1
8	Must_0	(Automatically set to 0 by the programmer as needed)	0
[7:3]	All_0	(Automatically set to 00000b by the programmer as needed)	00000b
[2:0]	LV_RST_VOL (Vpot)	Select the threshold voltage of the power supply low voltage detection reset module LVR (error 4%): 000 or 001 select 2.4V; 010 select 2.7V; 011 select 3.0V; 100 select 3.6V; 101 select 4.0V; 110 select 4.3V; 111 select 4.6V	000b

6.3 Data Memory Space

The internal data storage space is 256bytes, which is all used for SFR and iRAM, in which iRAM is used for stack and fast data storage, which can be subdivided into working register R0-R7, bit variable bdata, byte variable data, idata and so on.

The external data storage space is a total of 64KB, as shown in figure 6.1. except that part of it is used for 2KB on-chip expansion xRAM, the remaining address range from 0800h to FFFFh is reserved.

32 bytes of read-only information and 32 bytes of OTP data, as shown in figure 6.1, need to be accessed through dedicated operations.

6.4 flash-ROM Register

Table 6.4 List of flash-ROM registers

Name	Address	Description	Reset value
ROM_DATA_HH	8Fh	High bytes of high words in flash-ROM data register (read-only)	xxh
ROM_DATA_HL	8Eh	Low bytes of high words in flash-ROM data register (read-only)	xxh
ROM_DATA_HI	8Eh	16-bit SFR consists of ROM_DATA_HL and ROM_DATA_HH	xxxxh
ROM_BUF_MOD	8Fh	Buffer mode register for flash-ROM erase and write operations	xxh
ROM_DAT_BUF	8Eh	Data buffer register for flash-ROM erase and write operations	xxh
ROM_STATUS	86h	Flash-ROM status register (read-only)	00h
ROM_CTRL	86h	Flash-ROM control register (write-only)	00h
ROM_ADDR_H	85h	Flash-ROM address register high byte	xxh
ROM_ADDR_L	84h	Flash-ROM address register low byte	xxh

ROM_ADDR	84h	16-bit SFR consists of ROM_ADDR_L and ROM_ADDR_H	xxxxh
ROM_DATA_LH	85h	High bytes of low word in flash-ROM data register (read only)	xxh
ROM_DATA_LL	84h	Low bytes of low word in flash-ROM data register (read only)	xxh
ROM_DATA_LO	84h	16-bit SFR consists of ROM_DATA_LL and ROM_DATA_LH	xxxxh

Flash-ROM Address Register (ROM_ADDR):

Bit	Name	Address	Description	Reset value
[7:0]	ROM_ADDR_H	RW	flash-ROM address high byte	xxh
[7:0]	ROM_ADDR_L	RW	flash-ROM address low byte	xxh

Flash-ROM Data Registers (ROM_DATA_HI, ROM_DATA_LO):

Bit	Name	Address	Description	Reset value
[7:0]	ROM_DATA_HH	RO	The high byte of the flash-ROM data register high word (16 bits)	xxh
[7:0]	ROM_DATA_HL	RO	The low byte of the flash-ROM data register high word (16 bits)	xxh
[7:0]	ROM_DATA_LH	RO	The high byte of the flash-ROM data register low word (16 bits)	xxh
[7:0]	ROM_DATA_LL	RO	The low byte of the flash-ROM data register low word (16 bits)	xxh

Buffer Mode Register for flash-ROM Erase and Write Operations (ROM_BUF_MOD):

Bit	Name	Address	Description	Reset value
7	bROM_BUF_BYTE	RW	Buffer mode for flash-ROM erase and write operations (erase or program): this bit selects the block programming mode for 0, and the data to be written is stored in the xRAM pointed by DPTR. During programming, CH549 automatically fetches data from xRAM and temporarily stores it in ROM_DAT_BUF and then writes to flash-ROM. It supports 1 to 64 bytes of data length, the actual length = MASK_ROM_ADR_END-ROM_ADDR_L [5:0] + 1. Select single-byte programming or 64-byte block erase mode for 1, and the data to be written is stored directly in ROM_DAT_BUF.	x
6	Reserved	RW	Reserved	x
[5:0]	MASK_ROM_ADDR	RW	In flash-ROM block programming mode, the	xxh

			lower 6 bits (including this address) of the end address of the flash-ROM block programming operation; In flash-ROM single-byte programming or 64-byte block erase mode, 00h is recommended for retention	

Data Buffer Register for flash-ROM Erase and Write Operations (ROM_DAT_BUF):

Bit	Name	Address	Description	Reset value
[7:0]	ROM_DAT_BUF	RW	Data buffer register for flash-ROM erase and write operations	xxh

Flash-ROM Control Register (ROM_CTRL):

Bit	Name	Address	Description	Reset value
[7:0]	ROM_CTRL	WO	flash-ROM control register	00h

Flash-ROM Status Register (ROM_STATUS):

Bit	Name	Address	Description	Reset value
7	Reserved	RO	Reserved	1
6	bROM_ADDR_OK	RO	Flash-ROM operation address valid status bit: 0: The parameter is invalid; 1: The address is valid.	0
[5:2]	Reserved	RO	Reserved	0000b
1	bROM_CMD_ERR	RO	Flash-ROM operation command error status bit: 0: Indicates a valid command; 1: Indicates an unknown command or timeout	0
0	Reserved	RO	Reserved	0

6.5 Flash-ROM Operation Steps

1. Erase flash-ROM and change all data bits in the target block to 0:

(1) Enable safe mode, SAFE_MOD = 55h; SAFE_MOD = 0AAh;

(2) Set the global configuration register GLOBAL_CFG to enable write (bCODE_WE or bDATA_WE corresponding to code or data);

(3) Set the address register ROM_ADDR to write the 16-bit destination address, which is only valid for 10 bits higher;

(4) Set the buffer mode register ROM_BUF_MOD of the erase-write operation to 80h, and select 64-byte block erase mode.

(5) Optionally, set the data buffer register ROM_DAT_BUF of the erase and write operation to 00h;

(6) Set the operation control register ROM_CTRL to 0A6h, perform the block erase operation, and the program is automatically suspended during the operation;

(7) When the program resumes running after the operation is completed, the status of the operation can be checked by querying the status register ROM_STATUS. If multiple blocks are to be erased, the loop (3), (4), (5), (6), (7) steps, and steps (3), (4), (5) can be switched sequentially;

(8) Enter the safe mode again, SAFE_MOD = 55h; SAFEDEMOD = 0AAh;
(9) Set the global configuration register GLOBAL_CFG to enable write protection (bCODE_WE=0, bDATA_WE=0).

2. Write flash-ROM in a single byte to change some data bits in the target byte from 0 to 1 (the bit data cannot be changed from 1 to 0):
(1) Enable safe mode, SAFE_MOD = 55h; SAFE_MOD = 0AAh;
(2) Set the global configuration register GLOBAL_CFG to enable write (bCODE_WE or bDATA_WE corresponding to code or data);
(3) Set the address register ROM_ADDR to write the 16-bit target address;
(4) Set the buffer mode register ROM_BUF_MOD for erase-write operation to 80h, and select single-byte programming mode;
(5) Set the data buffer register ROM_DAT_BUF of the erase and write operation to the byte data to be written;
(6) Set the operation control register ROM_CTRL to 09Ah to perform the write operation, and the program is automatically suspended during the operation;
(7) When the program resumes running after the operation is completed, the status of the operation can be checked by querying the status register ROM_STATUS. If multiple data are to be written, the steps (3), (4), (5), (6), (7), and steps (3), (4), (5) can be switched sequentially;
(8) Enter the safe mode again, SAFE_MOD = 55ht SAFEDEMOD = 0Aah;
(9) Set the global configuration register GLOBAL_CFG to enable write protection (bCODE_WE=0, bDATA_WE=0).

3. Write flash-ROM in blocks to change some data bits in multiple target bytes from 0 to 1 (the bit data cannot be changed from 1 to 0):
(1) Enable safe mode, SAFE_MOD = 55h; SAFEDEMOD = 0Aah;
(2) Set the global configuration register GLOBAL_CFG to enable write (bCODE_WE or bDATA_WE corresponding to code or data);
(3) Set the address register ROM_ADDR to write a 16-bit starting destination address, such as 1357h;
(4) Set the buffer mode register ROM_BUF_MOD of the erase and write operation to the lower 6 bits of the end target address, which should be greater than or equal to the starting target address of ROM_ADDR_L [5:0]. Select the data block programming mode, for example, if the end address is 1364h, then ROM_BUF_MOD should be set to 24 hours (64h&3Fh) and calculate the number of bytes of the data block = 0Dh;
(5) Allocate a 64-byte-aligned buffer area in xRAM, such as 0580h~05BFh, specify the offset address in the buffer area with the lower 6 bits of the starting destination address, get the xRAM buffer start address of this data block programming operation, store the block to be written from the xRAM buffer start address, and put the xRAM buffer start address into DPTR, for example, DPTR=0580h+ (57h&3Fh) = 0597h. The actual programming operation only uses the xRAM of the 0597h~05A4h address;
(6) Set the operation control register ROM_CTRL to 09Ah to perform the write operation, and the program is automatically suspended during the operation;
(7) When the program resumes running after the operation is completed, the status of the operation can be checked by querying the status register ROM_STATUS. If multiple data are to be written, the steps (3), (4), (5), (6), (7), and steps (3), (4), (5) can be switched sequentially.
(8) Enter the safe mode again, SAFE_MOD = 55h; SAFEDEMOD = 0AAh;
(9) Set the global configuration register GLOBAL_CFG to enable write protection (bCODE_WE=0, bDATA_WE=0).

4. Read flash-ROM:
Read the code or data of the target address directly using the MOVC instruction or through a pointer to the program's storage space.

5. Write the OTP data region in a single byte, changing some data bits in the target byte from 0 to 1 (the bit data cannot be changed from 1 to 0):
(1) Enable safe mode, SAFE_MOD = 55hth SAFEDEMOD = 0AAh;
(2) Set the global configuration register GLOBAL_CFG to enable write enable (bDATA_WE);
(3) Set the address register ROM_ADDR and write to the destination address (20h~3Fh). In fact, only the upper 4 bits of the lower 6 bits are valid;
(4) Set the buffer mode register ROM_BUF_MOD for erase-write operation to 80h, and select single-byte programming mode;
(5) Set the data buffer register ROM_DAT_BUF of the erase and write operation to the byte data to be written;
(6) Set the operation control register ROM_CTRL to 099h, perform the write operation, and the program is automatically suspended during the operation;
(7) When the program resumes running after the operation is completed, the status of the operation can be checked by querying the status register ROM_STATUS. If multiple data are to be written, the steps (3), (4), (5), (6), (7), and steps (3), (4), (5) can be switched sequentially;
(8) Enter the safe mode again, SAFE_MOD = 55ht SAFEDEMOD = 0AAh;
(9) Set the global configuration register GLOBAL_CFG to enable write protection (bCODE_WE=0, bDATA_WE=0).

6. Read read-only information area or OTP data area in 4 bytes:
(1) Set the address register ROM_ADDR to write a 4-byte aligned destination address (00h~3Fh), which is only valid for the lower 6 bits;
(2) Set the operation control register ROM_CTRL to 08Dh, perform the read operation, and automatically suspend the program during the operation;
(3) The program resumes running after the operation is completed. Query the status register ROM_STATUS to view the status of the operation;
(4) 4 bytes of data are obtained from flash-ROM data registers ROM_DATA_HI and ROM_DATA_LO.

7. Note: when erasing and writing flash-ROM/EEPROM, it is recommended that it be carried out only at the ambient temperature of-20℃ ~ 85℃. If the program erase and write operation is carried out beyond the above temperature range, although it is normal in general, it does not rule out the possibility of reducing the data retention capacity TDR and reducing the erase times NEPCE or even affect the accuracy of the data.

6.6 On-board Program and ISP Download

When configuring the information Code_Protect=0, the code and data in the CH549 chip flash-ROM can be read and written by an external programmer through the synchronous serial interface; when the configuration information Code_Protect=1, the code and data in the flash-ROM are protected and cannot be read, but can be erased, and the code protection will be removed if the power is rebooted after erasing.
When the CH549 chip is preset with the BootLoader bootstrap, CH549 can support various ISP download methods such as USB or asynchronous serial port to load the application; but in the absence of the bootstrap, CH549 can only be written into the bootstrap or application by an external special programmer. In order to support on-board programming, 4 connection pins between CH549 and programmer need to be reserved in the circuit, and the least

necessary connection pins are 3: P1.4, P1.6, P1.7.

Table 6.6.1 Connection pins to the programmer

Pin	GPIO	Description
RST	P5.7	Programmed reset control pin (optional), high to allow entry into programmed state
SCS	P1.4	Programmed chip select input pin (necessary), default high, active low
SCK	P1.7	Programmed clock input pin (necessary)
MISO	P1.6	Data output pin in programming state (necessary)

6.7 Unique ID

Each single-chip microcomputer leaves the factory with a unique ID number, that is, the chip identification number. The ID data and its checksum have a total of 8 bytes and are stored in the area where the offset address of the read-only information area is 10h. Please refer to the C language example program for specific operation.

Table 6.7.1 Chip ID address table

Offset address	ID data description
10h, 11h	ID first word data, in order, the lowest byte of the ID number, the next lowest byte
12h, 13h	ID second word data, in order, the next highest byte and the highest byte of the ID number
14h, 15h	ID last word data, in order, is the second highest byte and highest byte of the 48-bit ID number
16h, 17h	The 16-bit sum of the first, second and last word of the ID data, used for ID checksum

The ID number can be used with the download tool to encrypt the target program. For general applications, you only need to use the first 32 bits of the ID number.

6.8 Calibration Information for Temperature Sensor (TS)

The calibration information of the temperature sensor is located in the area where the offset address of the read-only information area is 0Ch. For specific operation, please refer to the C language example program.

7. Power Management, Sleep and Reset

7.1 External Power in

The CH549 chip has a low dropout voltage regulator LDO from 5V to 3.3V, and the 3.3V power supply is used in modules such as USB. CH549 supports external 5V or 3.3V or even 2.8V power supply voltage input, the two power supply voltage input modes refer to the following table.

External power voltage	VDD voltage: external voltage 2.8V~5V	V33 voltage: internal USB voltage 3.3V (Notes: V33 will be automatically shorted to VDD during sleep)
3.3V or 2.8V Including <3.6V	3.3V voltage input to I/O and LDO. A decoupling capacitor not less than 0.1uF to the ground necessarily.	Short VDD input as internal USB power. A decoupling capacitor not less than 0.1uF to the ground necessarily.
5V Including >3.6V	5V voltage input to I/O and LDO. A decoupling capacitor not less than 0.1uF to the ground necessarily.	Internal voltage regulator 3.3V output and 3.3V internal USB power input. A decoupling capacitor not less than 0.1uF to the ground necessarily.

After the power is powered on or the system is reset, the CH549 is running by default. On the premise that the performance meets the requirements, properly reducing the main frequency of the system can reduce the power consumption at run time. When CH549 does not need to run at all, you can set the PD in PCON to sleep, and you can choose to wake up externally through USB, UART0, UART1, SPI0 and some GPIO during sleep.

7.2 Power and Sleep Control Register

Table 7.2.1 Power and sleep control registers

Name	Address	Description	Reset value
WDOG_COUNT	FFh	Watchdog count register	00h
RESET_KEEP	FEh	Reset keep register	00h
POWER_CFG	BAh	Power management configuration register	0xh
WAKE_CTRL	A9h	Wake-up control register	00h
PCON	87h	Power control register	10h

Watchdog count register (WDOG_COUNT):

Bit	Name	Access	Description	Reset value
[7:0]	WDOG_COUNT	RW	Watchdog current count, count full 0FFh turn 00h when overflow, overflow automatically set interrupt flag bWDOG_IF_TO to 1	00h

Reset keep register (RESET_KEEP):

Bit	Name	Access	Description	Reset value
[7:0]	RESET_KEEP	RW	Reset the hold register, the value can be artificially modified, except that the power-on reset can clear it, any other reset will not affect the value.	00h

Power Management Configuration Register (POWER_CFG), only can be written in safe mode:

Bit	Name	Access	Description	Reset value
7	bPWR_DN_MODE	RW	Sleep power off mode selection: 0: Power off/deep sleep mode, saving more power, but wake up slowly. 1: Standby/normal sleep mode, wake up quickly.	0
6	bUSB_PU_RES	RW	USB pull-up resistance selection: 0: 1.5KΩ, for the case when V33 is 3.3V. 1: 7KΩ, for the case when V33 is 5V.	0
5	bLV_RST_OFF	RW	Low voltage reset detection module OFF: 0: Enable supply voltage detection and generate reset signal at low voltage. 1: Low voltage detection module off.	0
4	bLDO_3V3_OFF	RW	USB voltage regulator LDO OFF control (auto OFF during sleep): 0: 3.3V voltage is generated by VDD power supply for USB and other modules. 1: Disable LDO and internally short V33 to VDD.	0
3	bLDO_CORE_VOL	RW	Core voltage mode: 0: Normal voltage mode. 1: Boost voltage mode, with better performance, and support higher system clock.	0
[2:0]	MASK_ULLDO_VOL	RW	Data keep supply voltage selection in power off/deep sleep mode: 000: 2.0V. 001: 1.9V. 010: 1.8V. 011: 1.7V. 100: 1.6V. 101: 1.5V. 110: 1.4V. 111: 1.3V. The above are relative reference values which do not need to be adjusted under a 5V supply; If 3.3V supply is used, it is recommended to read first, subtract 2 from the lower 3 bits (if the original value is less than 2 the result is cleared to 0) and write back in safe mode in order to select the relative higher two data holding voltages.	xxxb

Wake-up Control Register (WAKE_CTRL), only can be written in safe mode:

Bit	Name	Access	Description	Reset value
7	bWAK_BY_USB	RW	USB event wake-up enable: 1: Enable; 0: Disable.	0
6	bWAK_RXD1_LO	RW	UART1 pin RXD1 low-level input event wake-up enable: 0: Disable; 1: Enable. Select RXD1 or RXD1_ according to bUART1_PIN_X=0/1.	0
5	bWAK_P1_5_LO	RW	P1.5 low-level wake-up enable 0: Disable; 1: Enable.	0

4	bWAK_P1_4_LO	RW	P1.4 low-level wake-up enable 0: Disable; 1: Enable.	0
3	bWAK_P0_3_LO	RW	P0.3 low-level wake-up enable 0: Disable; 1: Enable.	0
2	bWAK_P57H_INT3L	RW	P5.7 high-level and INT3 low-level wake-up enable 0: Disable; 1: Enable.	0
1	bWAK_INT0E_P33L	RW	INT0 edge change and P3.3 low-level wake-up enable. 0: Disable; 1: Enable. INT0 selects INT0 or INT0_ according to bINT0_PIN_X=0/1.	0
0	bWAK_RXD0_LO	RW	UART0 pin RXD0 low-level input wake-up enable. 0: Disable; 1: Enable. Select RXD0 or RXD0_ according to bUART0_PIN_X=0/1.	0

The wake-up enable of the voltage comparator is controlled by bCMP_EN. When bCMP_EN is 1, if the comparator results in inverse change, it will wake up automatically.

Power Control Register (PCON):

Bit	Name	Access	Description	Reset value
7	SMOD	RW	Baud rate selection for UART0 mode 1/2/3 when timer1 is used to generate UART0 baud rate: 0: Slow mode. 1: Fast mode.	0
6	Reserved	RO	Reserved	0
5	bRST_FLAG1	R0	Recent reset flag high bit	0
4	bRST_FLAG0	R0	Recent reset flag low bit	1
3	GF1	RW	General purpose flag bit 1 User-defined. Can be reset and set by software	0
2	GF0	RW	General purpose flag bit 0 User-defined. Can be reset and set by software	0
1	PD	RW	Sleep mode enable, set to 1 and sleep, hardware automatically clears when waking up. It is strongly recommended to turn off global interrupts (EA=0) before sleep.	0
0	Reserved	RO	Reserved	0

Table 7.2.2 Description of recent reset flag

bRST_FLAG1	bRST_FLAG0	复位标志描述
0	0	Software reset, source: bSW_RESET=1 and (bBOOT_LOAD=0 or bWDOG_EN=1)
0	1	Power on reset or low voltage detection reset, source: voltage on VDD is lower than checking voltage
1	0	Watchdog reset, source: bWDOG_EN=1 and watchdog timeout overflows

1	1	External input manual reset by RST pin, source: En_P5.7_RESET=1 and P5.7 high-level input

7.3 Reset Control

CH549 has 5 reset sources: power-on reset and power supply low-voltage detection reset, external reset, software reset, watchdog reset, the latter three belong to thermal reset.

7.3.1 Power on Reset and Low Voltage Detection Reset

The power-on reset POR is generated by the on-chip power-on detection circuit, and the Tpor is automatically delayed by the hardware to maintain the reset state, and the CH549 runs after the delay is over.

The power supply low voltage detection reset LVR is generated by the on-chip voltage detection circuit. The LVR circuit continuously monitors the power supply voltage of the VDD pin and produces a low voltage reset when it is lower than the detection level Vpot, and the hardware automatically delays the Tpor to maintain the reset state, and the CH549 runs after the delay is over.

Only power-on reset and power low-voltage detection reset make CH549 reload configuration information and clear reset _ KEEP, other hot resets do not affect.

7.3.2 External Reset

The external reset is generated by a high level applied to the RST pin. The reset process is triggered when the configuration information En_P5.7_RESET is 1 and the duration of the high level on the RST pin is greater than the Trst. When the external high-level signal is withdrawn, the hardware automatically delays the Trdl to maintain the reset state, and after the delay ends, the CH549 starts to execute from the 0 address.

7.3.3 Software Reset

CH549 supports internal software reset so that the CPU state can be actively reset and re-run without external intervention. Setting the bSW_RESET in the global configuration register GLOBAL_CFG to 1, the software can reset, and automatically delay the Trdl to maintain the reset state. After the delay ends, the CH549 starts from the 0 address, and the bSW_RESET bit is automatically zeroed by the hardware.

When bSW_RESET is set to 1, if bBOOT_LOAD=0 or bWDOG_EN=1, then bRST_FLAG1/0 will be indicated as software reset after reset; when bSW_RESET is set to 1, if bBOOT_LOAD=1 and bWDOG_EN=0, then bRST_FLAG1/0 will not generate a new reset flag, but will keep the previous reset flag unchanged.

For the chip with the ISP boot program, after the power is reset, the boot program is run first, and the program resets the chip according to the need to switch to the application program state. This software reset only causes the bBOOT_LOAD to zero and does not affect the state of the bRST_FLAG1/0 (due to the bBOOT_LOAD=1 before the reset), so when switching to the application state, the bRST_FLAG1/0 still indicates the power-on reset state.

7.3.4 Watchdog Reset

The watchdog reset occurs when the watchdog timer overruns. The watchdog timer is an 8-bit counter whose clock frequency is the system main frequency Fsys/131072. It produces an overflow signal when the full 0FFh turns to 00h.

The watchdog timer overflow signal will trigger the interrupt flag bWDOG_IF_TO 1, which is automatically zeroed when the WDOG_COUNT is reloaded or when the corresponding interrupt service program is entered.

Different timing period Twdc is realized by writing different initial counting values to WDOG_COUNT. Under the 12MHz dominant frequency, the watchdog timing period Twdc is about 2.8s for 00h writing and 1.4s for 80h writing.

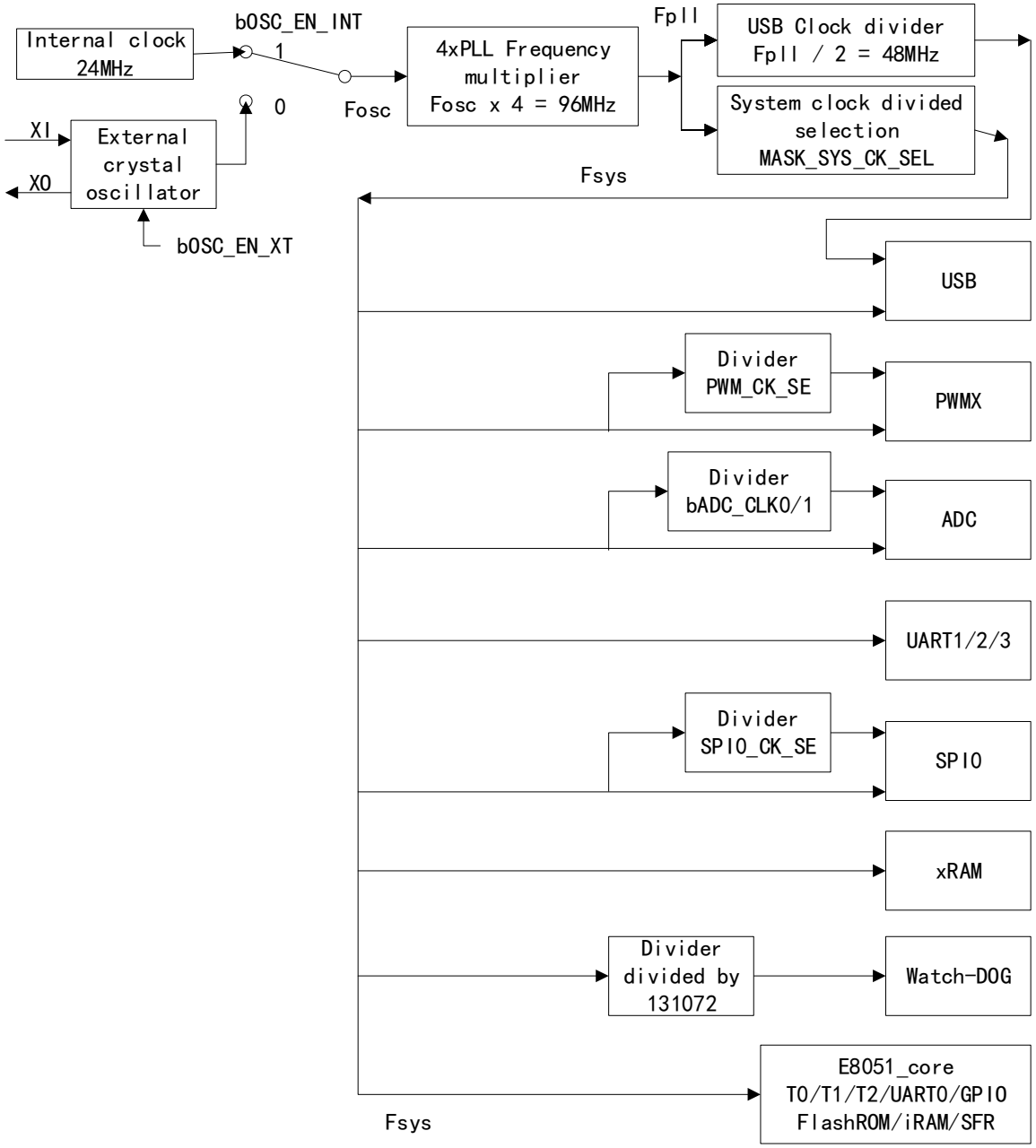
If the watchdog timer overflows bWDOG_EN=1, then the watchdog reset is generated, and the Trdl is automatically

delayed to maintain the reset state. After the delay ends, the CH549 is executed from address 0.
In order to avoid being reset by watchdog during bWDOG_EN=1, WDOG_COUNT must be reset in time to avoid overflow.

8. System Clock

8.1 Clock Block Diagram

Figure 8.1.1 Clock system and structure diagram



After selecting one of the two clocks, the internal clock or the external clock is used as the original clock Fosc, and then the Fpll high frequency clock is generated after PLL frequency doubling. finally, the system clock Fsys and the clock Fusb4x of the USB module are obtained through two groups of frequency dividers. The system clock Fsys is provided directly to each module of CH549.

8.2 Register Description

Table 8.2.1 Clock Control Register

Name	Address	Description	Reset value
CLOCK_CFG	B9h	System clock configuration register	83h

System Clock Configuration Register (CLOCK_CFG), only can be written in safe mode:

Bit	Name	Access	Description	Reset value
7	bOSC_EN_INT	RW	Internal clock oscillator enable, a 1 enables the internal clock oscillator and selects the internal clock; a 0 disables the internal clock oscillator and selects the external crystal oscillator to provide the clock.	1
6	bOSC_EN_XT	RW	External crystal oscillator enable, this bit is 1 to enable the P4.6/XO pin as XI/XO and enable the oscillator, an external quartz crystal or ceramic oscillator is required between XI and XO; this bit is 0 to disable the external oscillator.	0
5	bWDOG_IF_TO	RO	The watchdog timer interrupt flag bit, a 1 in this bit indicates an interrupt, triggered by the timer overflow signal; a 0 in this bit indicates no interrupt. This bit is automatically cleared when the watchdog count register WDOG_COUNT is reloaded or when the corresponding interrupt service program is entered.	0
[4:3]	Reserved	RO	Reserved	00b
[2:0]	MASK_SYS_CK_SEL	RW	System clock frequency selection, refer to Table 8.2.2.	011b

Table 8.2.2 System clock frequency selection

MASK_SYS_CK_SEL	System main frequency Fsys	Relation with Fxt	Fsys when Fosc=24MHz
000b	Fpll / 512	Fxt / 128	187.5KHz
001b	Fpll / 128	Fxt / 32	750KHz
010b	Fpll / 32	Fxt / 8	3MHz
011b	Fpll / 8	Fxt / 2	12MHz
100b	Fpll / 6	Fxt / 1.5	16MHz
101b	Fpll / 4	Fxt / 1	24MHz
110b	Fpll / 3	Fxt / 0.75	32MHz
111b	Fpll / 2	Fxt / 0.5	Reserved, for custom chips only, to be used with bLDO_CORE_VOL=1

8.3 Clock Configuration

When the CH549 chip is powered on, the internal clock is used by default, and the internal clock frequency is 24MHz. Either the internal clock or the external crystal oscillator clock can be selected through the CLOCK_CFG.

If the external crystal oscillator is turned off, the XI pin can be used as a P4.6 normal I/O port. If an external crystal oscillator is used to provide a clock, then the crystal should be straddled between the XI and XO pins, and the oscillating capacitors should be connected to the GND for the XI and XO pins, respectively; if the clock signal is input directly from the outside, it should be input from the XI pin with the XO pin suspended.
Original clock frequency Fosc = bOSC_EN_INT? 24MHz: Fxt
PLL frequency: Fpll = Fosc * 4
USB clock: Fusb4x = Fpll / 2
System clock frequency (Fsys) is obtained by divided Fpll, please refer to Table 8.2.2.
Default status after reset, Fosc=24MHz, Fpll=96MHz, Fusb4x=48MHz, and Fsys=12MHz.

The steps to switch to an external crystal oscillator to provide a clock are as follows:
(1) Enter safe mode, step 1: SAFE_MOD = 55h; step 2: SAFE_MOD = AAh
(2) Use the bit OR operation to set the bOSC_EN_XT in the CLOCK_CFG to 1, keep the other bits unchanged, and enable the crystal oscillator
(3) Delay several milliseconds, usually 5mS~10mS, waiting for the crystal oscillator to work stably
(4) Enter safe mode again, step 1 SAFE_MOD = 55h; step 2 SAFE_MOD = AAh
(5) Use the "bit and" operation to clear the bOSC_EN_INT in the CLOCK_CFG, leave the other bits unchanged, and switch to the external clock
(6) Turn off safe mode and write any value to SAFE_MOD to terminate safe mode early.

The steps to modify the main frequency of the system are as follows:
(1) Enter safe mode, step 1: SAFE_MOD = 55h; step 2: SAFE_MOD = AAh
(2) Write a new value to CLOCK_CFG
(3) Turn off safe mode and write any value to SAFE_MOD to terminate safe mode early.

Remarks:
(1) If using USB module, then Fusb4x must be 48MHz; and when using full-speed USB, the system main frequency Fsys is not less than 6MHz; when using low-speed USB, the system main frequency Fsys is not lower than 1.5MHz.
(2) Give priority to the lower system clock frequency Fsys, so as to reduce the dynamic power consumption of the system and widen the working temperature range.

9. Interrupt

The CH549 chip supports 16 groups of interrupt signal sources, including 6 groups of interrupts compatible with standard MCS51: INT0, T0, INT1, T1, UART0, T2, and extended 10 groups of interrupts: SPI0, INT3, USB, ADC/UART2, UART1, PWMX/UART3, GPIO, WDOG, among which GPIO interrupts can be selected from 7 I/O pins.

Interrupt service programs should be as concise as possible, try not to call functions and subroutines, and try not to read and write xdata variables and code constants.

9.1 Register Description

Table 9.1.1 List of interrupt vector

Interrupt	Entry address	Interrupt No.	Description	Default priority
INT_NO_INT0	0x0003	0	External interrupt 0	High priority ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ Low priority
INT_NO_TMR0	0x000B	1	Timer0 interrupt	
INT_NO_INT1	0x0013	2	External interrupt 1	
INT_NO_TMR1	0x001B	3	Timer1 interrupt	
INT_NO_UART0	0x0023	4	UART0 interrupt	
INT_NO_TMR2	0x002B	5	Timer2 interrupt	
INT_NO_SPI0	0x0033	6	SPI0 interrupt	
INT_NO_INT3	0x003B	7	External interrupt 3	
INT_NO_USB	0x0043	8	USB interrupt	
INT_NO_ADC INT_NO_UART2	0x004B	9	ADC interrupt (when bU2IE=0); UART2 interrupt (when bU2IE=1)	
INT_NO_UART1	0x0053	10	UART1 interrupt	
INT_NO_PWMX INT_NO_UART3	0x005B	11	PWMX interrupt (when bU3IE=0); UART3 interrupt (when bU3IE=1)	
INT_NO_GPIO	0x0063	12	GPIO Interrupt	
INT_NO_WDOG	0x006B	13	Watchdog timer interrupt	

Table 9.1.2 List of interrupt registers

Name	Address	Description	Reset value
IP_EX	E9h	Extended interrupt priority control register	00h
IE_EX	E8h	Extended interrupt enable register	00h
GPIO_IE	CFh	GPIO interrupt enable register	00h
IP	B8h	Interrupt priority control register	00h
INTX	B3h	Extended external interrupt control register	00h
IE	A8h	Interrupt enable register	00h

Interrupt Enable Register (IE):

Bit	Name	Access	Description	Reset value
7	EA	RW	Global interrupt enable control bit 1: Interrupt is enabled when E_DIS is 0.	0

			0: All interrupt requests are disabled.	
6	E_DIS	RW	Global interrupt disable control bit 1: All interrupt requests are disabled; 0: Interrupt is enabled when EA is 1. This bit is usually used to disable interrupt temporarily during flash-ROM operation.	0
5	ET2	RW	Timer2 interrupt enable bit 1: T2 interrupt is enabled; 0: T2 interrupt is disabled.	0
4	ES	RW	UART0 interrupt enable bit 1: UART0 interrupt is enabled; 0: UART0 interrupt is disabled.	0
3	ET1	RW	Timer1 interrupt enable bit 1: T1 interrupt is enabled; 0: T1 interrupt is disabled.	0
2	EX1	RW	External interrupt1 enable bit 1: INT1 interrupt is enabled; 0: INT1 interrupt is disabled.	0
1	ET0	RW	Timer0 interrupt enable bit 1: T0 interrupt is enabled; 0: T0 interrupt is disabled.	0
0	EX0	RW	External interrupt0 enable bit 1: INT0 interrupt is enabled; 0: INT0 interrupt is disabled.	0

Extended Interrupt Enable Register (IE_EX):

Bit	Name	Access	Description	Reset value
7	IE_WDOG	RW	Watchdog timer interrupt enable 1: WDOG interrupt is enabled. 0: WDOG interrupt is disabled.	0
6	IE_GPIO	RW	GPIO interrupt enable 1: GPIO interrupt is enabled. 0: GPIO interrupt is disabled.	0
5	IE_PWMX IE_UART3	RW	PWMX interrupt enable when bU3IE=0: 1: PWMX interrupt is enabled. 0: PWMX interrupt is disabled. UART3 interrupt enable when bU3IE=1: 1: UART3 interrupt is enabled. 0: UART3 interrupt is disabled.	0
4	IE_UART1	RW	UART1 interrupt enable 1: UART1 interrupt is enabled. 0: UART1 interrupt is disabled.	0
3	IE_ADC IE_UART2	RW	ADC interrupt enable when bU2IE=0: 1: ADC interrupt is enabled.	0

			0: ADC interrupt is disabled. UART2 interrupt enable when bU2IE=1: 1: UART2 interrupt is enabled. 0: UART2 interrupt is disabled.	
2	IE_USB	RW	USB interrupt enable 1: USB interrupt is enabled. 0: USB interrupt is disabled.	0
1	IE_INT3	RW	External interrupt 3 enable 1: INT3 interrupt is enabled. 0: INT3 interrupt is disabled.	0
0	IE_SPI0	RW	SPI0 interrupt enable 1: SPI0 interrupt is enabled. 0: SPI0 interrupt is disabled.	0

GPIO Interrupt Enable Register (GPIO_IE):

Bit	Name	Access	Description	Reset value
7	bIE_IO_EDGE	RW	GPIO edge interrupt mode enable: 0: Level interrupt mode. bIO_INT_ACT=1 and interrupt will be requested constantly if there is a valid GPIO input level. Otherwise bIO_INT_ACT=0 and no interrupt request occurs with invalid GPIO input level. 1: Edge interrupt mode. There are interrupt flag bIO_INT_ACT and interrupt request with valid GPIO input edge, bIO_INT_ACT cannot be cleared by software, but it is automatically cleared when reset or interrupt program is running in level interrupt mode.	0
6	bIE_RXD1_LO	RW	1: UART1 RX pin interrupt is enabled (valid with low level in level mode or falling edge in edge mode). 0: UART1 RX pin interrupt is disabled. Select RXD1 or RXD1_ according to bUART1_PIN_X=0/1.	0
5	bIE_P1_5_LO	RW	1: P1.5 interrupt is enabled (valid with low level in level mode or falling edge in edge mode). 0: P1.5 interrupt is disabled.	0
4	bIE_P1_4_LO	RW	1: P1.4 interrupt is enabled (valid with low level in level mode or falling edge in edge mode). 0: P1.4 interrupt is disabled.	0
3	bIE_P0_3_LO	RW	1: P0.3 interrupt is enabled (valid with low level in level mode or falling edge in edge mode). 0: P0.3 interrupt is disabled.	0
2	bIE_P5_7_HI	RW	1: P5.7 interrupt is enabled (valid with high level in level mode or rising edge in edge mode). 0: P1.5 interrupt is disabled.	0
1	bIE_P4_6_LO	RW	1: P4.6 interrupt is enabled (valid with low level in level mode or falling edge in edge mode). 0: P4.6 interrupt is disabled.	0

0	bIE_RXD0_LO	RW	1: UART0 RX pin interrupt is enabled (valid with low level in level mode or falling edge in edge mode). 0: UART0 RX pin interrupt is disabled. Select RXD0 or RXD0_ based on bUART0_PIN_X=0/1.	0

Extended External Interrupt Register (INTX):

Bit	Name	Access	Description	Reset value
7	Reserved	RO	Reserved	0
6	Reserved	RO	Reserved	0
5	bIX3	RW	INT3 Input signal polarity 0: Default polarity (triggered by low level or falling edge). 1: Reverse polarity (triggered by high level or rising edge).	0
4	Reserved	RO	Reserved	0
3	bIE3	RW	INT3 interrupt request flag Auto reset after it enters interrupt.	0
2	bIT3	RW	INT3 trigger mode control 0: Triggered by low or high level. 1: Triggered by falling or rising edge.	0
1	Reserved	RO	Reserved	0
0	Reserved	RO	Reserved	0

Interrupt Priority Control Register (IP):

Bit	Name	Access	Description	Reset value
7	PH_FLAG	RO	High priority interrupt running flag	0
6	PL_FLAG	RO	Low priority interrupt running flag	0
5	PT2	RW	Timer2 interrupt priority control bit	0
4	PS	RW	UART0 interrupt priority control bit	0
3	PT1	RW	Timer1 interrupt priority control bit	0
2	PX1	RW	External interrupt 1 priority control bit	0
1	PT0	RW	Timer0 interrupt priority control bit	0
0	PX0	RW	External interrupt 0 priority control bit	0

Extended Interrupt Priority Control Register (IP_EX):

Bit	Name	Access	Description	Reset value
7	bIP_LEVEL	RO	Current interrupt nesting level flag bit 0: No interrupt or dual interrupt nesting. 1: Single interrupt nesting.	0
6	bIP_GPIO	RW	GPIO interrupt priority control bit	0
5	bIP_PWMX bIP_UART3	RW	PWMX interrupt priority control bit when bU3IE=0. UART3 interrupt priority control bit when bU3IE=1.	0
4	bIP_UART1	RW	UART1 interrupt priority control bit	0
3	bIP_ADC bIP_UART2	RW	ADC interrupt priority control bit when bU2IE=0. UART2 interrupt priority control bit when bU2IE=1.	0

2	bIP_USB	RW	USB interrupt priority control bit	0
1	bIP_INT3	RW	External interrupt 3 interrupt priority control bit	0
0	bIP_SPI0	RW	SPI0 interrupt priority control bit	0

IP and IP_EX registers are used to set the interrupt priority. If a bit is set to 1, the corresponding interrupt source is set to a high priority; if a bit is cleared 0, the corresponding interrupt source is set to a low priority. For sibling interrupt sources, the system has a default priority order, which is shown in Table 9.1.1. Where the combination of PH_FLAG and PL_FLAG represents the priority of the current interrupt.

Table 9.1.3 Current interrupt priority status indication

PH_FLAG	PL_FLAG	Current interrupt priority status
0	0	No current interrupts
0	1	Currently executing a low priority interrupt
1	0	Currently executing a high priority interrupt
1	1	Unexpected status, unknown error

10. I/O Port

10.1 GPIO Introduction

The CH549 provides up to 44 I/O pins, some of which are multiplexed. Among them, the input and output of port P0~P4 can be addressed bit by bit. If the pin is not configured for multiplexing, the default is the general-purpose I/O pin state. When used as a general-purpose digital I/O, all of the I/O ports have a true "read-modify-write" function, supporting SETB or CLR bit operation instructions to independently change the direction of certain pins or port electrical equality.

10.2 GPIO Register

All registers and bits in this section are expressed in a common format: the lowercase "n" represents the serial number of the port (n = 0, 1, 2, 3, 4), while the lowercase "x" represents the sequence number of the bit (x0,1, 2, 3, 4, 5, 6, 7).

Table 10.2.1 List of GPIO Registers

Name	Address	Description	Reset value
P0	80h	P0 input/output register	FFh
P0_DIR_PU	C5h	P0 direction control and pull-up enable register	FFh
P0_MOD_OC	C4h	P0 output mode register	FFh
P1	90h	P1 input/output register	FFh
P1_DIR_PU	93h	P1 direction control and pull-up enable register	FFh
P1_MOD_OC	92h	P1 output mode register	FFh
P2	A0h	P2 input/output register	FFh
P2_DIR_PU	95h	P2 direction control and pull-up enable register	FFh
P2_MOD_OC	94h	P2 output mode register	FFh
P3	B0h	P3 input/output register	FFh
P3_DIR_PU	97h	P3 direction control and pull-up enable register	FFh
P3_MOD_OC	96h	P3 output mode register	FFh
P4	C0h	P4 input/output register	FFh
P4_DIR_PU	C3h	P4 direction control and pull-up enable register	FFh
P4_MOD_OC	C2h	P4 output mode register	FFh
P5	ABh	P5 input/output register	20h
PIN_FUNC	AAh	Pin function selection register	00h
XBUS_AUX	A2h	Bus auxiliary setting register	00h

Pn Input/Output Register (Pn):

Bit	Name	Access	Description	Reset value
[7:0]	Pn.0~Pn.7	RW	Pn.x pin state input and data output bits, support addressing by bit. *Notes: P4.7 is the internal bit, the write operation must be set to 1, and the read operation is meaningless.*	FFh

Pn Output Mode Register (Pn_MOD_OC):

Bit	Name	Access	Description	Reset value

[7:0]	Pn_MOD_OC	RW	Pn.x pin output mode setting: 0: Push-pull output; 1: Open-drain output.	FFh

Pn Direction Control and Pull-up Enable Register (Pn_DIR_PU):

Bit	Name	Access	Description	Reset value
[7:0]	Pn_DIR_PU	RW	Pn.x direction control in push-pull output mode: 0: Input. 1: Output. Pn.x pull-up resistor enable control in open-drain output mode: 0: Disable the pull-up resistor; 1: Enable the pull-up resistor.	FFh

Port Pn configuration is realized by Pn_MOD_OC[x] and Pn_DIR_PU[x], details as follows.

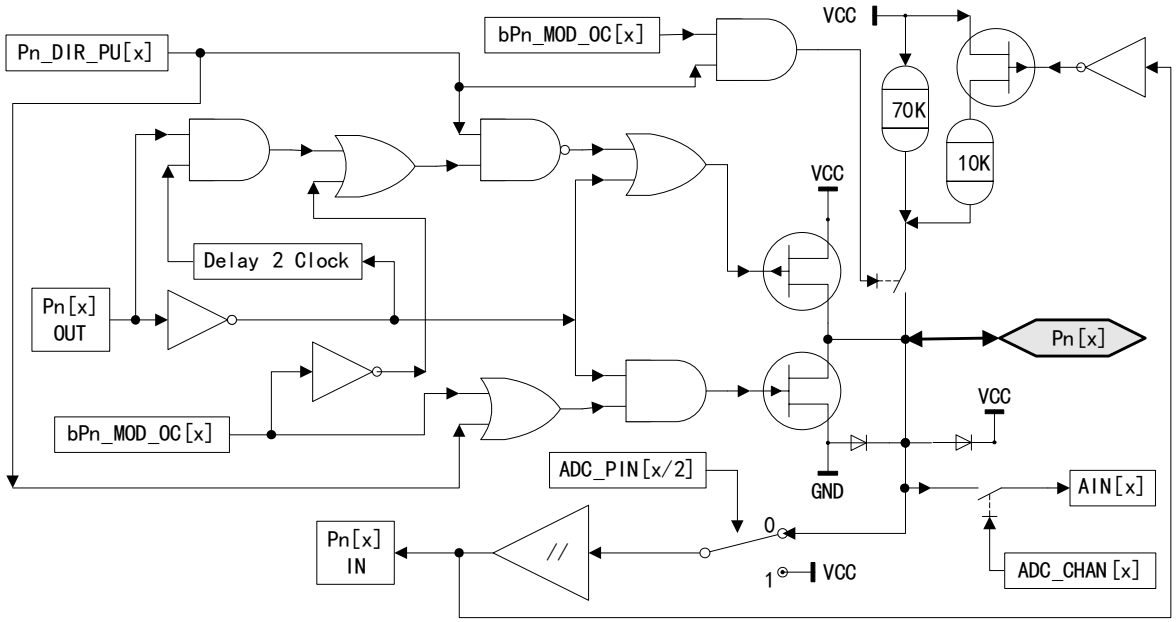
Table 10.2.2 Port configuration register combination

Pn_MOD_OC	Pn_DIR_PU	Working mode description
0	0	High impedance input mode, pins without pull-up resistor
0	1	Push-pull output mode with symmetry driving ability, a port can output or absorb large current in this mode
1	0	Open-drain output, support high impedance input, pins without pull-up resistor
1	1	Standard bi-direction mode (standard 8051), open-drain output, support input, pins with pull-up resistor. It will automatically generate 2 clock period of high level to accelerate conversion when output transfer from low level to high level

The P1~P4 port supports pure input or push-pull output and standard bidirectional modes. Each pin has an internal pull-up resistor that can be freely controlled and a protective diode connected to the VDD and GND.

Figure 10.2.1 is the equivalent schematic diagram of the P0.x pin of the P0 port and the P1.x pin of the P1 port, which can be applied to the P2, P3 and P4 ports without AIN, ADC_PIN and ADC_CHAN.

Figure 10.2.1 Equivalent schematic diagram of I/O pins



P5 Input/Output Register (P5):

Bit	Name	Access	Description	Reset value
7	P5.7	R0	P5.7 pin state input bit	0
6	Reserved	RO	Reserved	0
5	P5.5	RW	P5.5 pin data output bit (open-drain output, support high voltage): 0: Output low level. 1: No output (high impedance, supports external pull-up resistor).	1
4	P5.4	RW	P5.4 pin data output bit: 0: Output low level. 1: Output high level.	0
3	Reserved	RO	Reserved	0
2	Reserved	RO	Reserved	0
1	P5.1	R0	P5.1 pin state input bit, built-in controllable pull-down resistor	0
0	P5.0	R0	P5.0 pin state input bit, built-in controllable pull-down resistor	0

10.3 GPIO Alternate Functions and Mapping

The CH549 part of the I/O pin has the alternate function, and after power-on, the default is the general-purpose I/O pin. After enabling different functional modules, the corresponding pins are configured as functional pins corresponding to their respective functional modules.

Pin Function Selection Register (PIN_FUNC):

Bit	Name	Access	Description	Reset value

7	bPWM0_PIN_X	RW	PWM0 pin mapping enable 0: PWM0 enables P2.5. 1: PWM0 enables P1.5.	0
6	bIO_INT_ACT	R0	GPIO interrupt request activation state: When bIE_IO_EDGE=0, 1: GPIO with valid level and interrupt request. 0: GPIO with invalid level. When bIE_IO_EDGE=1, this bit is used as edge interrupt flag, 1: Valid edge is detected and this bit cannot be reset by software, but can only be reset automatically when reset or in level interrupt mode or when it enters corresponding interrupt service program.	0
5	bUART1_PIN_X	RW	UART1 pin mapping enable 0: RXD1/TXD1 enable P2.6/P2.7. 1: RXD1/TXD1 enable P1.6/P1.7.	0
4	bUART0_PIN_X	RW	UART0 pin mapping enable 0: RXD0/TXD0 enable P3.0/P3.1. 1: RXD0/TXD0 enable P0.2/P0.3.	0
3	Reserved	RO	Reserved	0
2	bINT0_PIN_X	RW	INT0 pin mapping enable 0: INT0 enables P3.2. 1: INT0 enables P2.2.	0
1	bT2EX_PIN_X	RW	T2EX/CAP2 pin mapping enable 0: T2EX/CAP2 enables P1.1. 1: T2EX/CAP2 enables P2.5.	0
0	bT2_PIN_X	RW	T2/CAP1 pin mapping enable 0: T2/CAP1 enables P1.0. 1: T2/CAP1 enables P2.4.	0

Table 10.3.1 List of GPIO pins alternate functions

GPIO	Other functions: left-to-right priority
P0[0]	AIN8、P0.0
P0[1]	AIN9、P0.1
P0[2]	RXD_/bRXD_、AIN10、P0.2
P0[3]	TXD_/bTXD_、AIN11、P0.3
P0[4]	RXD2/bRXD2、AIN12、P0.4
P0[5]	TXD2/bTXD2、AIN13、P0.5
P0[6]	RXD3/bRXD3、AIN14、P0.6
P0[7]	TXD3/bTXD3、AIN15、P0.7
P1[0]	T2/bT2、CAP1/bCAP1、AIN0、P1.0
P1[1]	T2EX/bT2EX、CAP2/bCAP2、AIN1、P1.1
P1[2]	AIN2、P1.2

P1[3]	AIN3、P1.3
P1[4]	SCS/bSCS、UCC1/bUCC1、AIN4、P1.4
P1[5]	MOSI/bMOSI、PWM0_/bPWM0_、UCC2/bUCC2、AIN5、P1.5
P1[6]	MISO/bMISO、RXD1_/bRXD1_、VBUS/bVBUS、AIN6、P1.6
P1[7]	SCK/bSCK、TXD1_/bTXD1_、AIN7、P1.7
P2[0]	PWM5/bPWM5、P2.0
P2[1]	PWM4/bPWM4、P2.1
P2[2]	PWM3/bPWM3、INT0_/bINT0、P2.2
P2[3]	PWM2/bPWM2、P2.3
P2[4]	PWM1/bPWM1、T2_/bT2_、CAP1_/bCAP1_、P2.4
P2[5]	PWM0/bPWM0、T2EX_/bT2EX_、CAP2_/bCAP2_、P2.5
P2[6]	PWM6/bPWM6、RXD1/bRXD1、P2.6
P2[7]	PWM7/bPWM7、TXD1/bTXD1、P2.7
P3[0]	RXD/bRXD、P3.0
P3[1]	TXD/bTXD、P3.1
P3[2]	INT0/bINT0、P3.2
P3[3]	INT1/bINT1、P3.3
P3[4]	T0/bT0、P3.4
P3[5]	T1/bT1、P3.5
P3[6]	CAP0/bCAP0、P3.6
P3[7]	INT3/bINT3、P3.7
P4[0]	P4.0
P4[1]	P4.1
P4[2]	P4.2
P4[3]	P4.3
P4[4]	P4.4
P4[5]	P4.5
P4[6]	XI、P4.6
P5[0]	UDM/bUDM、P5.0
P5[1]	UDP/bUDP、P5.1
P5[4]	bALE/bCKO、P5.4
P5[5]	bHVOD、P5.5
P5[7]	RST/bRST、P5.7

The priority described in the above table, from left to right, refers to the priority of multiple functional modules competing for the use of the GPIO. For example, the P2.6/P2.7 port is set for UART1, and if only RXD1 is needed, then P2.7 can still be used for higher priority PWM7 functions.

11. External Bus (xBUS)

CH549 does not provide bus signals to the outside of the chip and does not support external buses, but it can access the on-chip xRAM normally.

External Bus Auxiliary Configuration Register (XBUS_AUX):

Bit	Name	Access	Description	Reset value
7	bUART0_TX	R0	UART0 Tx status 1: It is transmitting.	0
6	bUART0_RX	R0	UART0 Rx status 1: It is receiving.	0
5	bSAFE_MOD_ACT	R0	Safe mode status 1: It is in safe mode.	0
4	bALE_CLK_EN	RW	ALE pin clock output enable 1: Enable P5.4 output divided system frequency. 0: Clock signal is disabled.	0
3	bALE_CLK_SEL	RW	When bALE_CLK_EN=1, ALE pin clock frequency is selected; If the bit is 0, select 12 frequency division. If the bit is 1, select 4 frequency division	0
3	GF2	RW	General flag bit 2 when bALE_CLK_EN=0: User-defined. Can be reset and set by software.	0
2	bDPTR_AUTO_INC	RW	Enable DPTR add by 1 automatically after MOVX_@DPTR command.	0
1	Reserved	RO	Reserved	0
0	DPS	RW	Dual DPTR data pointer selection: 0: DPTR0. 1: DPTR1.	0

Table 11.1 P5.4 alternate ALE/CKO output status

P5[4]	bALE_CLK_EN	bALE_CLK_SEL	P5.4 引脚功能描述
0	0	0	Output low level (default)
0	1	0	Fsys/12
0	1	1	Fsys/4
1	X	X	Output high level

12. Timer

12.1 Timer0/1

Timer0/1 is two 16-bit timing / counters. Through TCON and TMOD, Timer0 and Timer1, TCON are configured for timing / counter T0 and T1 startup control and overflow interrupt control as well as external interrupt control. Each timer is a 16-bit timing unit composed of two 8-bit registers. The high byte counter of timer 0 is TH0, and the low byte is TL0; timer 1. The high byte counter is TH1, and the low byte is TL1. Timer 1 can also be used as a baud rate generator for UART0.

Table 12.1.1 List of Timer0/1registers

Name	Address	Description	Reset value
TH1	8Dh	Timer1 count high byte	xxh
TH0	8Ch	Timer0 count high byte	xxh
TL1	8Bh	Timer1 count low byte	xxh
TL0	8Ah	Timer0 count low byte	xxh
TMOD	89h	Timer0/1 method register	00h
TCON	88h	Timer0/1 control register	00h

Timer/Counter 0/1 Control Register (TCON):

Bit	Name	Access	Description	Reset value
7	TF1	RW	Timer1 overflow interrupt flag Auto reset after it enters Timer1 interrupt service.	0
6	TR1	RW	Timer1 startup/stop bit Set 1 to start. Set and reset by software.	0
5	TF0	RW	Timer0 overflow interrupt flag Auto reset after it enters Timer0 interrupt.	0
4	TR0	RW	Timer0 startup/stop bit Set 1 to start. Set and reset by software.	0
3	IE1	RW	INT1 interrupt request flag Auto reset after it enters interrupt.	0
2	IT1	RW	INT1 trigger mode control 0: Low level action. 1: Falling edge action.	0
1	IE0	RW	INT0 interrupt request flag Auto reset after it enters interrupt.	0
0	IT0	RW	INT0 trigger mode control 0: Low level action. 1: Falling edge action.	0

Timer/Counter 0/1 Mode Register (TMOD):

Bit	Name	Access	Description	Reset value
7	bT1_GATE	RW	Gate enable bit control, whether Timer1 start is affected by the external interrupt signal INT1. 0: Timer1 will start or not independent of INT1;	0

			1: It will only start if the INT1 pin is high and TR1 is 1.	
6	bT1_CT	RW	Counter or timer mode selection for Timer1: 0: Timer, use internal clock. 1: Counter, use T1 pin falling edge as clock	0
5	bT1_M1	RW	Timer/Counter1 mode high bit	0
4	bT1_M0	RW	Timer/Counter1 mode low bit	0
3	bT0_GATE	RW	Gate enable bit control, whether Timer0 start is affected by the external interrupt signal INT0. 0: Timer0 will start or not independent of INT0; 1: It will only start if the INT0 pin is high and TR0 is 1.	0
2	bT0_CT	RW	Counter or timer mode selection for Timer0: 0: Timer, use internal clock. 1: Counter, use T0 pin falling edge as clock	0
1	bT0_M1	RW	Timer/Counter0 mode high bit	0
0	bT0_M0	RW	Timer/Counter0 mode low bit	0

Table 12.1.2 Timern operating mode selection for bTn_M1 and bTn_M0 (n=0, 1)

bTn_M1	bTn_M0	Timern operating mode (n=0, 1)
0	0	Mode 0: 13-bit timer or counter n by cascaded THn and lower 5 bits of TLn, the upper 3 bits of TLn are ignored. When the counts of all 13 bits change from 1 to 0, set the overflow flag TFn and reset the initial value.
0	1	Mode 1: 16-bit timer or counter n by cascaded THn and TLn. When the counts of all 16 bits change from 1 to 0, set the overflow flag TFn and reset the initial value.
1	0	Mode 2: 8-bit overload timer/counter n, TLn is used for count unit, and THn is used as the overload count unit. When the counts of all 8 bits change from 1 to 0, set the overflow flag TFn and automatically load the initial value from THn.
1	1	Mode 3: For timer/counter 0, it is divided into TL0 and TH0. TL0 is used as an 8-bit timer/counter, occupying all control bits of Timer0. TH0 is also used as an 8-bit timer, occupying TR1, TF1 and interrupt resources of Timer1. In this case, Timer1 is still available, but the startup control bit TR1 and overflow flag bit TF1 cannot be used. For timer/counter 1, it stops after it enters mode3.

Timern Count Low Byte (TLn) (n=0, 1):

Bit	Name	Access	Description	Reset value
[7:0]	TLn	RW	Timern count low byte	xxh

Timern Count High Byte (THn) (n=0, 1):

Bit	Name	Access	Description	Reset value
[7:0]	THn	RW	Timern count high byte	xxh

12.2 Timer2

Timer2 is a 16-bit automatic overload timer / counter and is configured through T2CON and T2MOD registers. The high byte counter of timer 2 is TH2 and the low byte is TL2. Timer2 can be used as the baud rate generator of UART0. It also has the function of 3-channel signal level capture. The capture count is stored in RCAP2, T2CAP1 and T2CAP0 registers.

Table 12.2.1 List of Timer2 registers

Name	Address	Description	Reset value
TH2	CDh	Timer2 counter high byte	00h
TL2	CCh	Timer2 counter low byte	00h
T2COUNT	CCh	16-bit SFR consists of TL2 and TH2	0000h
T2CAP1H	CFh	Timer2 captures 1 data in high bytes (read-only)	xxh
T2CAP1L	CEh	Timer2 captures 1 data in low bytes (read-only)	xxh
T2CAP1	CEh	16-bit SFR consists of T2CAP1L and T2CAP1H	xxxxh
T2CAP0H	C7h	Timer2 captures 0 data in high bytes (read-only)	xxh
T2CAP0L	C6h	Timer2 captures 0 data in low bytes (read-only)	xxh
T2CAP0	C6h	16-bit SFR consists of T2CAP0L and T2CAP0H	xxxxh
RCAP2H	CBh	Count reload/capture 2 data register high byte	00h
RCAP2L	CAh	Count reload/capture 2 data register low byte	00h
RCAP2	CAh	16-bit SFR consists of RCAP2L and RCAP2H	0000h
T2MOD	C9h	Timer2 method register	00h
T2CON	C8h	Timer2 control register	00h
T2CON2	C1h	Timer2 extended control register	00h

Timer/Counter2 Control Register (T2CON):

Bit	Name	Access	Description	Reset value
7	TF2	RW	When bT2_CAP1_EN=0, it is the overflow interrupt flag of Timer2. When the Timer2 count is changed from 16 bits to all zeros, the overflow flag is set to 1, which needs to be cleared by the software. When RCLK=1 or TCLK=1, the bit will not be set to 1.	0
7	CAP1F	RW	When bT2_CAP1_EN=1, it is the Timer2 capture 1 interrupt flag, triggered by the T2 effective edge, and requires software zeroing.	0
6	EXF2	RW	The external trigger flag of Timer2, which is set to 1 by the effective edge of T2EX when EXEN2=1, which requires software to clear zero.	0
5	RCLK	RW	UART0 Rx clock selection 0: Timer1 overflow pulse. 1: Timer2 overflow pulse.	0
4	TCLK	RW	UART0 Tx clock selection 0: Timer1 overflow pulse. 1: Timer2 overflow pulse.	0
3	EXEN2	RW	T2EX trigger enable	0

			0: Ignore T2EX. 1: Enable trigger reload or capture by T2EX edge.	
2	TR2	RW	Timer2 startup/stop bit Set 1 to start. Set and reset by software.	0
1	C_T2	RW	Timer2 clock source selection 0: Internal clock. 1: Edge counter based on T2 falling edge.	0
0	CP_RL2	RW	Timer2 function select bit, if RCLK or TCLK is 1, this bit should be forced to 0. 0: Timer2 acts as a timer/counter and can automatically reload the count initial value when the counter overflows or the T2EX level changes; 1: Timer2's capture 2 function is enabled to capture the valid edge of T2EX.	0

Timer/Counter2 Method Register (T2MOD):

Bit	Name	Access	Description		Reset value
7	bTMR_CLK	RW	Fastest internal clock mode for T0/T1/T2 under faster clock mode: 0: Use divided clock. 1: Use original Fsys as clock without dividing. This bit has no effect on selecting standard clock timer		0
6	bT2_CLK	RW	Timer2 internal clock frequency selection bit, this bit is 0 to select standard clock, timing/counting mode is Fsys/12, UART0 clock mode is Fsys/4; this bit is 1 to select fast clock, timing/counting mode is Fsys/4 (bTMR_CLK=0) or Fsys (bTMR_CLK=1), UART0 clock mode is Fsys/2 (bTMR_CLK=0) or Fsys (bTMR_CLK=1)		0
5	bT1_CLK	RW	Timer1 internal clock frequency selection: 0 = Standard clock, Fsys/12. 1 = Faster clock, Fsys/4 if bTMR_CLK = 0, or Fsys if bTMR_CLK = 1.		0
4	bT0_CLK	RW	Timer0 internal clock frequency selection: 0 = Standard clock, Fsys/12. 1 = Faster clock, Fsys/4 if bTMR_CLK = 0, or Fsys if bTMR_CLK = 1.		0
3	bT2_CAP_M1	RW	Timer2 capture mode high bit	Capture mode selection: X0: From falling edge to falling edge. 01: From any edge to any edge (level change). 11: From rising edge to rising edge.	0
2	bT2_CAP_M0	RW	Timer2 capture mode low bit		0
1	T2OE	RW	Timer2 clock output enable 0: Disable output. 1: Enable clock output at T2 pin, frequency = TF2/2.		0

0	bT2_CAP1_EN	RW	Capture 1 mode enabled when RCLK=0, TCLK=0, CP_RL2=1, 1: Enable capture 0 function to capture T2 valid edges; 0: Disable capture 0	0

Count Reload/Capture 2 Data Register (RCAP2):

Bit	Name	Access	Description	Reset value
[7:0]	RCAP2H	RW	High byte of reload value in timer/counter mode. High byte of timer captured by CAP2 in capture mode.	00h
[7:0]	RCAP2L	RW	Low byte of reload value in timer/counter mode. Low byte of timer captured by CAP2 in capture mode	00h

12.3 PWM Register

The PWM_DATA registers in this section are expressed in a common format: the lowercase "n" indicates the serial number of the port (n=0~7).

Table 12.3.1 List of PWMX registers

Name	Address	Description	Reset value
PWM_CK_SE	9Eh	PWM clock divisor setting register	00h
PWM_CTRL	9Dh	PWM control register	02h
PWM_CTRL2	9Fh	PWM extended control register	00h
PWM_DATA0	9Ch	PWM0 data register	xxh
PWM_DATA1	9Bh	PWM1 data register	xxh
PWM_DATA2	9Ah	PWM2 data register	xxh
PWM_DATA3	A3h	PWM3 data register	xxh
PWM_DATA4	A4h	PWM4 data register	xxh
PWM_DATA5	A5h	PWM5 data register	xxh
PWM_DATA6	A6h	PWM6 data register	xxh
PWM_DATA7	A7h	PWM7 data register	xxh

PWMn Data Register (PWM_DATAn):

Bit	Name	Access	Description	Reset value
[7:0]	PWM_DATAn	RW	Store the current data of PWMn. Duty cycle of PWMn output active level = PWM_DATAn/PWM_CYCLE	xxh

PWM Control Register (PWM_CTRL):

Bit	Name	Access	Description	Reset value
7	Reserved	RO	Reserved	0
6	bPWM1_POLAR	RW	PWM1 output polarity control 0: Default low and active high. 1: Default high and active low.	0
5	bPWM0_POLAR	RW	PWM0 output polarity control 0: Default low and active high. 1: Default high and active low.	0

4	bPWM_IF_END	RW	PWM cycle end interrupt flag 1: There is a PWM cycle end interrupt. Write 1 to reset, or reload PWM_DATA0 data to reset.	0
3	bPWM1_OUT_EN	RW	PWM1 output enable 1: Enable PWM1 output.	0
2	bPWM0_OUT_EN	RW	PWM0 output enable 1: Enable PWM0 output.	0
1	bPWM_CLR_ALL	RW	1: Clear PWM count and FIFO. Reset by software.	1
0	bPWM_MOD_6BIT	RW	PWM data width mode: 0: 8-bit data, and PWM cycle is 256. 1: 6-bit data, and PWM cycle is 64.	0

PWM Extended Control Register (PWM_CTRL2):

Bit	Name	Access	Description	Reset value
7	Reserved	RO	Reserved	0
6	Reserved	RO	Reserved	0
5	bPWM7_OUT_EN	RW	PWM7 output enable 1: Enable PWM7 output.	0
4	bPWM6_OUT_EN	RW	PWM6 output enable 1: Enable PWM6 output.	0
3	bPWM5_OUT_EN	RW	PWM5 output enable 1: Enable PWM5 output.	0
2	bPWM4_OUT_EN	RW	PWM4 output enable 1: Enable PWM4 output.	0
1	bPWM3_OUT_EN	RW	PWM3 output enable 1: Enable PWM3 output.	0
0	bPWM2_OUT_EN	RW	PWM2 output enable 1: Enable PWM2 output.	0

PWM Clock Divisor Setting Register (PWM_CK_SE):

Bit	Name	Access	Description	Reset value
[7:0]	PWM_CK_SE	RW	Set PWM clock frequency division factor	00h

12.4 PWM Function

CH549 provides 8-channel PWM, which can dynamically modify the output duty cycle of PWM. After integral low-pass filtering through simple RC resistance and capacitance, various output voltages can be obtained, which is equivalent to low-speed digital-to-analog converter DAC. Among them, PWM0 and PWM1 can also choose reverse polarity output and the default output polarity is low level or high level.

PWM_CYCLE = bPWM_MOD_6BIT ? 64 : 256

PWMn output duty cycle= PWM_DATAn / PWM_CYCLE

The range of duty cycle is 0 to 99.6% in 8-bit data mode and 0 to 100% duty cycle in 6-bit data mode (100% if the PWM_DATAn value is greater than PWM_CYCLE).

In practical application, it is recommended to allow PWM pin output and set PWM output pin to push-pull output mode.

12.5 Timer

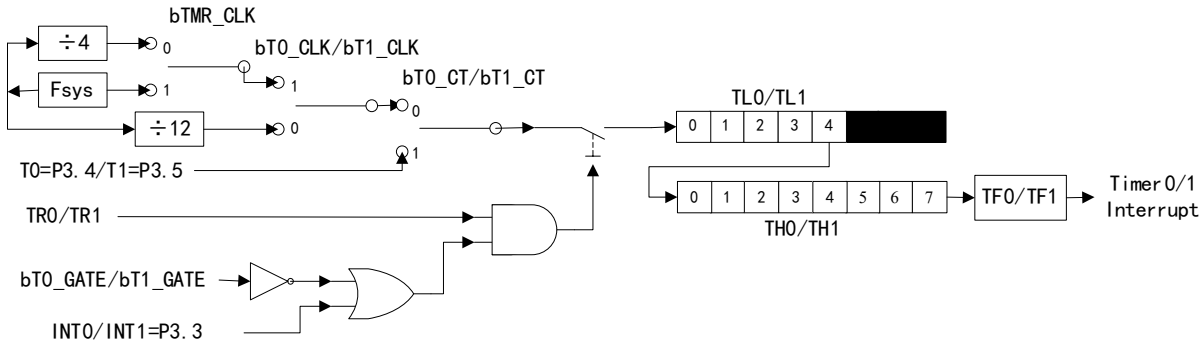
12.5.1 Timer0/1

(1) Set the T2MOD to choose the internal clock rate of Timer. If the bTn_CLK (n=0/1) is 0, then the clock corresponding to Timer0/1 is Fsys/12;. If the clock is 1, then bTMR_CLK=0 or 1 chooses Fsys/4 or Fsys as the clock.

(2) Sets the operating mode of the TMOD configuration Timer.

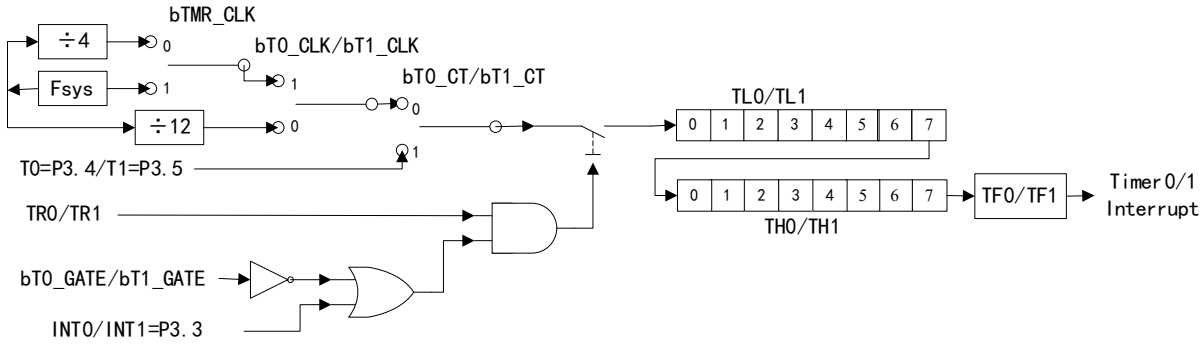
Mode 0:13-bit timer / counter

Figure 12.5.1.1 Timer0/1 mode0



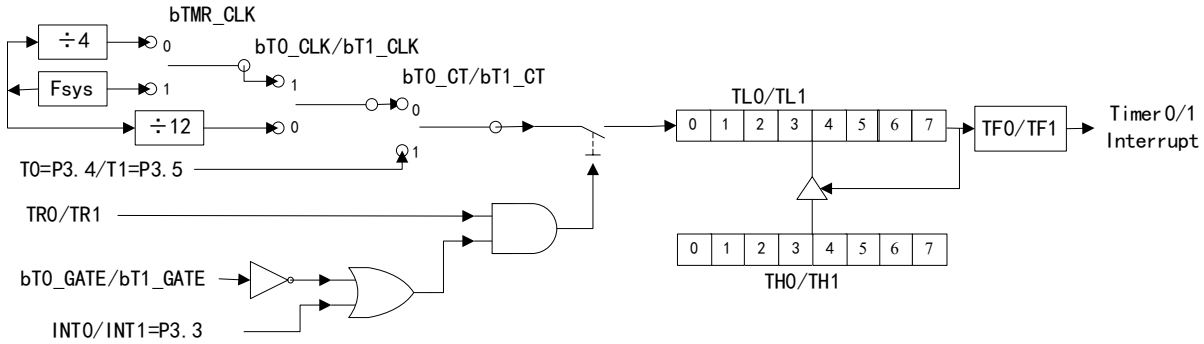
Mode1: 16-bit timer/counter

Figure 12.5.1.2 Timer0/1 mode1



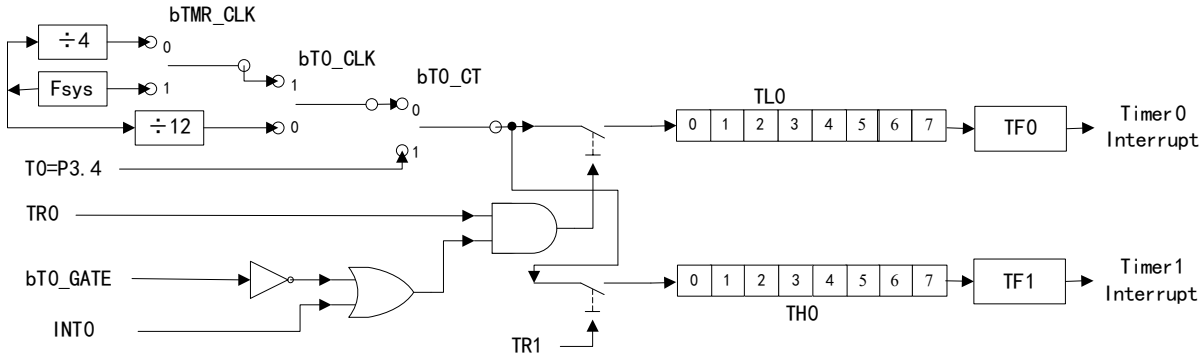
Mode2: Auto-reload 8-bit timer/counter

Figure 12.5.1.3 Timer0/1 mode2



Mode 3: Timer0 is decomposed into two independent 8-bit timing / counters and borrows the TR1 control bit of Timer1; Timer1 passes whether to start mode 3 instead of the borrowed TR1 control bit, and if Timer1 enters mode 3, the Timer1 stops running.

Figure 12.5.1.4 Timer0 mode3



(3) Set the initial values of the timer / counter TLn and THn (n=0/1).

(4) Set the bit TRn (n=0/1) in TCON to turn on or off the timing / counter, which can be detected by the bit TFn (n=0/1) query or by interrupt mode.

12.5.2 Timer2

Timer2 16-bit overload timing / counter mode:

(1) Set the bit RCLK and TCLK in T2CON to 0, and select the non-serial baud rate generator mode.

(2) Set the bit C_T2 in the T2CON to 0 to choose to use the internal clock, turn to step 3; you can also set 1 to select the falling edge of the T2 pin as the counting clock, skipping step 3.

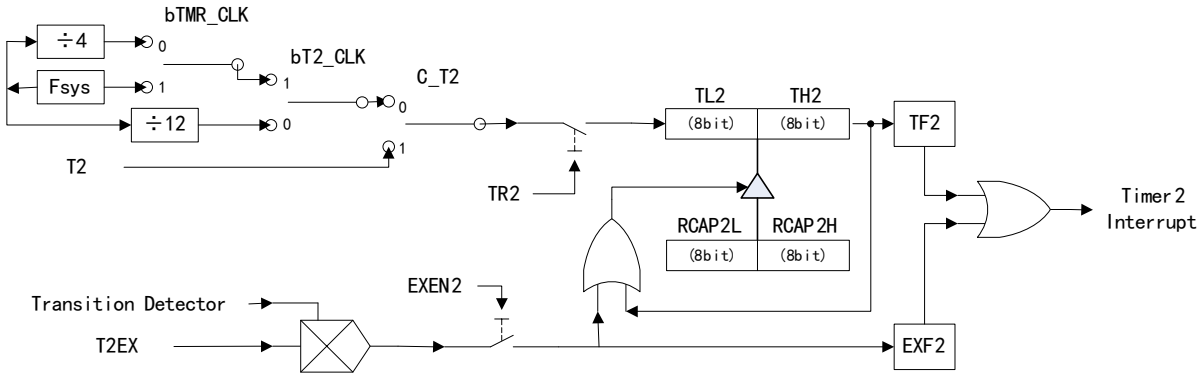
(3) Set T2MOD to choose the internal clock rate of Timer. If bT2_CLK is 0, then the clock of Timer2 is Fsys/12; If bT2_CLK is 1, then bTMR_CLK=0 or 1 choose Fsys/4 or Fsys as the clock.

(4) Set the bit CP_RL2 of T2CON to 0, and select the 16-bit overload timing / counter function of Timer2.

(5) Set RCAP2L and RCAP2H as the overload values after the timer overflow, set TL2 and TH2 as the initial values of the timer (usually the same as RCAP2L and RCAP2H), set TR2 to 1, and turn on Timer2.

(6) The current timer / counter status can be obtained by querying TF2 or timer 2 interrupt.

Fig.12.5.2.1 Timer2 16-bit reload timer/counter



Timer2 clock output mode:

Referring to the 16-bit overload timing / counter mode, and setting the bit T2OE in the T2MOD to 1, the binary clock of the TF2 frequency can be output from the T2 pin.

Timer2 serial port 0 baud rate generator mode:

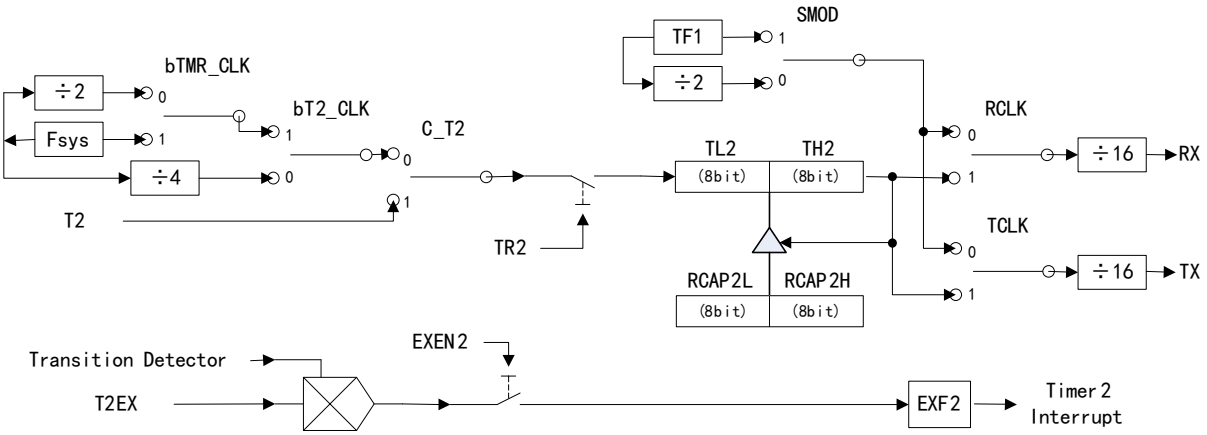
(1) Set the bit C_T2 in the T2CON to 0 to choose to use the internal clock, or set the falling edge of the T2 pin as the clock, set the bit RCLK and TCLK in the T2CON to 1 or one of them as needed, and select the serial baud

rate generator mode.

(2) Set T2MOD to choose the internal clock rate of Timer. If bT2_CLK is 0, then the clock of Timer2 is Fsys/4;. If bT2_CLK is 1, then bTMR_CLK=0 or 1 choose Fsys/2 or Fsys as the clock.

(3) Set RCAP2L and RCAP2H as the overload values after the timer overflow, set TR2 to 1, and turn on Timer2.

Figure 12.5.2.2 Timer2 UART0 baud rate generator



Timer2 signal channel capture mode:

(1) Set the bit RCLK and TCLK in T2CON to 0, and select the non-serial baud rate generator mode.

(2) Set the bit C_T2 in the T2CON to 0 to choose to use the internal clock, turn to step (3), or choose the falling edge of the T2 pin as the counting clock, skip step (3).

(3) Set T2MOD to choose the internal clock rate of Timer. If bT2_CLK is 0, then the clock of Timer2 is Fsys/12;. If bT2_CLK is 1, then bTMR_CLK=0 or 1 choose Fsys/4 or Fsys as the clock.

(4) Set the bits of T2MOD bT2_CAP_M1 and bT2_CAP_M0 to select the corresponding edge snap mode.

(5) Set the bit CP_RL2 of T2CON to 1, and select the capture function of Timer2 to the T2EX pin.

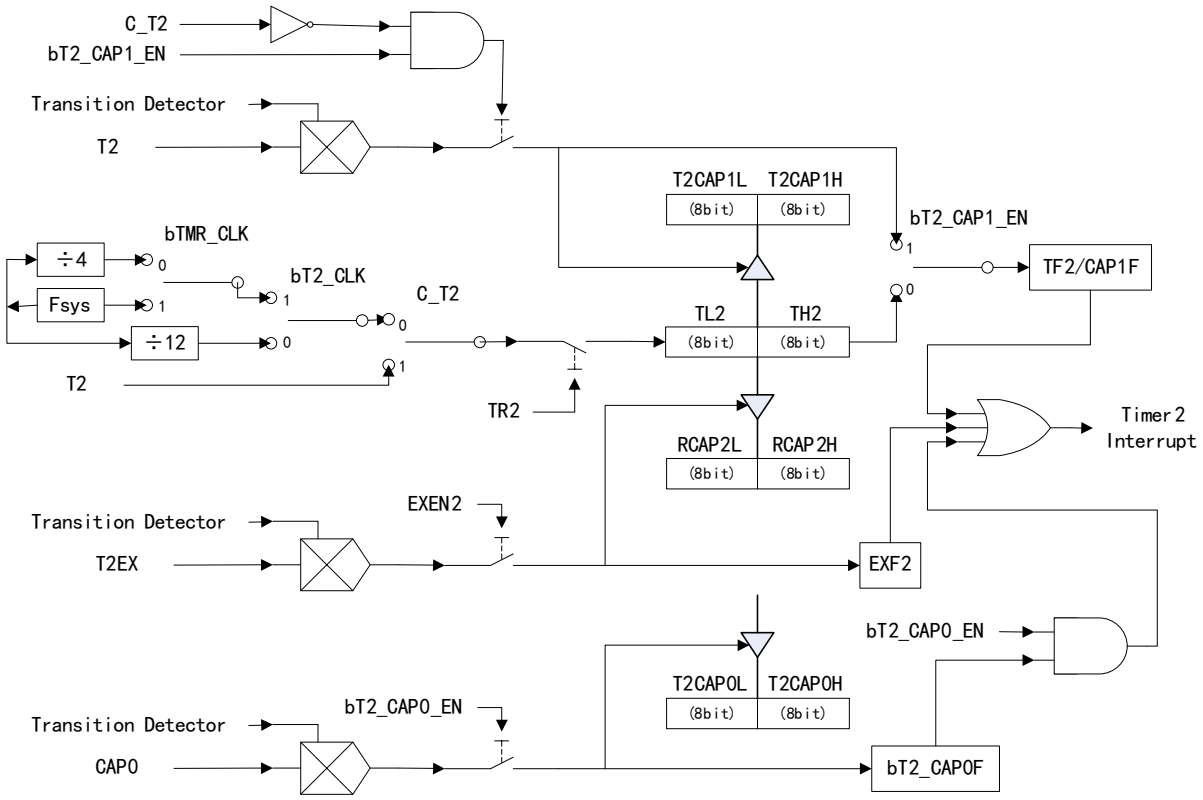
(6) Set TL2 and TH2 as the initial values of the timer, set TR2 to 1, and turn on Timer2.

(7) When CAP2 capture is complete, RCAP2L and RCAP2H will save the count values of TL2 and TH2 at that time and set EXF2 to generate an interrupt, and the difference between the next captured RCAP2L and RCAP2H and the previous captured RCAP2L and RCAP2H will be the width of the signal between the two active edges.

(8) If the bit C_T2 in the T2CON is 0 and the bit bT2_CAP1_EN in the T2MOD is 1, the capture of the T2 pin by Timer2 will be enabled at the same time. When the CAP1 capture is complete, T2CAP1L and T2CAP1H will save the count values of the TL2 and TH2 at that time, and set the CAP1F, causing an interruption.

(9) If the bit bT2_CAP0_EN in T2CON2 is 1, then Timer2's capture of CAP0 pins will be enabled at the same time. When CAP0 capture is complete, T2CAP0L and T2CAP0H will save the count values of TL2 and TH2 at that time, and set bT2_CAP0F, resulting in an interruption.

Figure 12.5.2.3 Timer2 capture mode



13. Universal Asynchronous Receiver Transmitter (UART)

13.1 UART Introduction

The CH549 chip provides 4 full-duplex UART: UART0~UART3. CH548 provides only UART0 and UART1.

UART0 is a standard MCS51 serial port, and its data receiving and sending are realized through SBUF accessing physically separate receiving / sending registers. The data written to the SBUF is loaded into the transmit register, and the read operation to the SBUF corresponds to the receive buffer register.

UART1 is a simplified MCS51 serial port, and its data receiving and sending are realized through SBUF1 accessing physically separate receiving / sending registers. The data written to the SBUF1 is loaded into the transmit register, and the read operation to the SBUF1 corresponds to the receive buffer register. Compared with UART0, UART1 removes the multi-computer communication mode and fixed baud rate, and UART1 has an independent baud rate generator.

UART2 adds an interrupt enable bit to replace ADC interrupts on the basis of UART1.

UART3 and UART2, also on the basis of UART1, add an interrupt enable bit to replace PWMX interrupts.

13.2 UART Register

Table 13.2.1 List of UART registers

Name	Address	Description	Reset value
SBUF	99h	UART0 data register	xxh
SCON	98h	UART0 control register	00h
SCON1	BCh	UART1 control register	40h
SBUF1	BDh	UART1 data register	xxh
SBAUD1	BEh	UART1 baud rate setting register	xxh
SIF1	BFh	UART1 interrupt status register	00h
SCON2	B4h	UART2 control register	00h
SBUF2	B5h	UART2 data register	xxh
SBAUD2	B6h	UART2 baud rate setting register	xxh
SIF2	B7h	UART2 interrupt status register	00h
SCON3	ACh	UART3 control register	00h
SBUF3	ADh	UART3 data register	xxh
SBAUD3	AEh	UART3 baud rate setting register	xxh
SIF3	AFh	UART3 interrupt status register	00h

13.2.1 UART0 Register Description

UART0 Control Register (SCON):

Bit	Name	Access	Description	Reset value
7	SM0	RW	UART0 mode bit0, data bit selection: 0: 8-bit data. 1: 9-bit data.	0
6	SM1	RW	UART0 mode bit1, baud rate selection: 0: Fixed. 1: Variable, generated by T1 or T2.	0
5	SM2	RW	UART0 Multi-machine communication control bit: When receiving data in modes 2 and 3, when SM2=1, if RB8 is 0, then	0

			RI is not set to 1 and reception is invalid; if RB8 is 1, then RI is set to 1 and reception is valid; when SM2=0, RI is set when receiving data and reception is valid, regardless of whether RB8 is 0 or 1; In mode 1, if SM2=1, then reception is only valid if a valid stop bit is received; In mode 0, the SM2 bit must be set to 0.	
4	REN	RW	UART0 receive enable 0: Disable. 1: Enable.	0
3	TB8	RW	Bit 9 of the sent data, in modes 2 and 3, TB8 is used to write bit 9 of the sent data, which can be a parity bit; in multi-machine communication, it is used to indicate whether the host is sending an address byte or a data byte, TB8=0 for data, TB8=1 for address.	0
2	RB8	RW	Bit 9 of the received data, in modes 2 and 3, RB8 is used to store bit 9 of the received data; in mode 1, if SM2=0, then RB8 is used to store the received stop bit; in mode 0, RB8 is not used.	0
1	TI	RW	Transmit interrupt flag bit, set by hardware after a data byte has been transmitted and needs to be cleared by software.	0
0	RI	RW	Receive interrupt flag bit, set by hardware after a data byte is received, needs to be cleared by software.	0

Table 13.2.1.1 UART0 working mode

SM0	SM1	Description
0	0	Mode 0, shift register method, baud rate fixed at Fsys/12
0	1	Mode 1, 8-bit asynchronous communication method, variable baud rate, generated by timer T1 or T2
1	0	Mode 2, 9-bit asynchronous communication method, baud rate is Fsys/128 (SMOD=0) or Fsys/32 (SMOD=1)
1	1	Mode 3, 9-bit asynchronous communication method, variable baud rate, generated by timer T1 or T2

In modes 1 and 3, when RCLK=0 and TCLK=0, the UART0 baud rate is generated by timer T1. T1 should be set to mode 2 automatic reload 8-bit timer mode, bT1_CT and bT1_GATE must both be 0, divided into the following types of clock cases.

Table 13.2.1.2 Calculation formula of UART0 baud rate

bTMR_CLK	bT1_CLK	SMOD	Description
1	1	0	TH1 = 256 - Fsys / 32 / baud rate
1	1	1	TH1 = 256 - Fsys / 16 / baud rate
0	1	0	TH1 = 256 - Fsys / 4 / 32 / baud rate
0	1	1	TH1 = 256 - Fsys / 4 / 16 / baud rate
X	0	0	TH1 = 256 - Fsys / 12 / 32 / baud rate
X	0	1	TH1 = 256 - Fsys / 12 / 16 / baud rate

In modes 1 and 3, when RCLK=1 or TCLK=1, the UART0 baud rate is generated by timer T2. T2 should be set to

16-bit automatic reload baud rate generator mode, C_T2 and CP_RL2 must both be 0, divided into the following types of clock cases.

Table 13.2.1.3 Calculation formula of UART0 baud rate

bTMR_CLK	bT2_CLK	Description
1	1	RCAP2 = 65536 - Fsys / 16 / baud rate
0	1	RCAP2 = 65536 - Fsys / 2 / 16 / baud rate
X	0	RCAP2 = 65536 - Fsys / 4 / 16 / baud rate

UART0 Data Register (SBUF):

Bit	Name	Access	Description	Reset value
[7:0]	SBUF	RW	UART0 data registers, including sending and receiving two physically separate registers. Transmit data registers corresponding to write data to SBUF; receive data registers corresponding to read data from SBUF.	xxh

13.2.2 UART1 Register Description

UART1 Control Register (SCON1):

Bit	Name	Access	Description	Reset value
7	bU1SM0	RW	UART1 working method selection 0: 8-bit data. 1: 9-bit data.	0
6	Reserved	RO	Reserved	1
5	bU1SMOD	RW	UART1 baud rate selection: 0: Slow mode. 1: Fast mode.	0
4	bU1REN	RW	UART1 receive enable 0: Disable. 1: Enable.	0
3	bU1TB8	RW	The 9th transmitted data bit, can be a parity bit in 9-bit data mode. In 8-bit data mode, TB8 is ignored.	0
2	bU1RB8	RW	The 9th received data bit. In 9-bit data mode, RB8 is used to store the 9th bit of the received data. In 8-bit data mode, RB8 is used to store the received stop bit.	0
1	bU1TIS	WO	Write 1, and the transmit interrupt flag bit will be preset to 1, and the read value is always 0.	0
0	bU1RIS	WO	Write 1, and the receive interrupt flag bit will be preset to 1, and the read value is always 0.	0

The UART1 baud rate is generated by the SBAUD1 setting, which is divided into two cases according to the choice of bU1SMOD:

When bU1SMOD=0, SBAUD1 = 256 - Fsys / 32 / baud rate.

When bU1SMOD=1, SBAUD1 = 256 - Fsys / 16 / baud rate.

UART1 Interrupt Status Register (SIF1):

Bit	Name	Access	Description	Reset value
[7:2]	Reserved	RO	Reserved	000000b
1	bU1TI	RW	Transmit interrupt flag bit, set by hardware after a byte is transmitted. Write 1 to reset by software (writing 0 to this bit will be ignored)	0
0	bU1RI	RW	Receive interrupt flag bit, set by hardware after a byte is received effectively. Write 1 to reset by software (writing 0 to this bit will be ignored)	0

Note: Writing 1 to the interrupt flag bit to zero ensures that only the specified flag bit is cleared and does not affect other interrupt flags under the same register (other interrupt flags may have been 1 before the write operation, or may become 1 during the write operation). Same as below.

UART1 Data Register (SBUF1):

Bit	Name	Access	Description	Reset value
[7:0]	SBUF1	RW	UART1 data registers, including transmitting and receiving two physically separate registers. Transmit data registers corresponding to write data to SBUF1; receive data registers corresponding to read data from SBUF1	xxh

13.2.3 UART2 Register Description

UART2 Control Register (SCON2):

Bit	Name	Access	Description	Reset value
7	bU2SM0	RW	UART2 working mode selection 0: 8-bit data. 1: 9-bit data.	0
6	bU2IE	RW	UART2 interrupt enable 0: UART2 request interrupt disabled, and the interrupt flag can be inquired. 1: UART2 interrupt enabled, and the original ADC interrupt is disabled for replacement.	0
5	bU2SMOD	RW	UART2 baud rate selection: 0: Slow mode. 1: Fast mode.	0
4	bU2REN	RW	UART2 receive enable 0: Disable. 1: Enable.	0
3	bU2TB8	RW	The 9th transmitted data bit. In 9-bit data mode, TB8 is used to write the 9th transmitted data bit, which can be a parity bit. In 8-bit data mode, TB8 is ignored.	0
2	bU2RB8	RW	The 9th received data bit. In 9-bit data mode, RB8 is used to store the 9th received data bit. In 8-bit data mode, RB8 is used to store the received stop bit.	0
1	bU2TIS	WO	Write 1, and the transmit interrupt flag bit will be preset to 1, and	0

			the read value is always 0.	
0	bU2RIS	WO	Write 1, and the receive interrupt flag bit will be preset to 1, and the read value is always 0.	0

UART2 baud rate is generated by SBAUD2, and it can be divided into 2 cases according to bU2SMOD:
When bU2SMOD=0, SBAUD2 = 256 - Fsys / 32 / baud rate.
When bU2SMOD=1, SBAUD2 = 256 - Fsys / 16 / baud rate.

UART2 Interrupt Status Register (SIF2):

Bit	Name	Access	Description	Reset value
[7:2]	Reserved	RO	Reserved	000000b
1	bU2TI	RW	Transmit interrupt flag bit, set by hardware after a byte is transmitted. Write 1 to reset by software (writing 0 to this bit will be ignored).	0
0	bU2RI	RW	Receive interrupt flag bit, set by hardware after a byte is received effectively. Write 1 to reset by software (writing 0 to this bit will be ignored).	0

UART2 Data Register (SBUF2):

Bit	Name	Access	Description	Reset value
[7:0]	SBUF2	RW	UART2 data registers, including transmitting and receiving two physically separate registers. Transmit data registers corresponding to write data to SBUF2; receive data registers corresponding to read data from SBUF2	xxh

13.2.4 UART3 Register Description

UART3 Control Register (SCON3):

Bit	Name	Access	Description	Reset value
7	bU3SM0	RW	UART3 working mode selection 0: 8-bit data. 1: 9-bit data.	0
6	bU3IE	RW	UART3 interrupt enable 0: UART3 request interrupt disabled, and the interrupt flag can be inquired. 1: UART3 interrupt enabled, and the original PWMX interrupt is disabled for replacement.	0
5	bU3SMOD	RW	UART3 baud rate selection 0: Slow mode. 1: Fast mode.	0
4	bU3REN	RW	UART3 receive enable 0: Disable. 1: Enable.	0
3	bU3TB8	RW	The 9th transmitted data bit. In 9-bit data mode, TB8 is used to write	0

			the 9th transmitted data bit, which can be a parity bit. In 8-bit data mode, TB8 is ignored.	
2	bU3RB8	RW	The 9th received data bit. In 9-bit data mode, RB8 is used to store the 9th received data bit. In 8-bit data mode, RB8 is used to store the received stop bit.	0
1	bU3TIS	WO	Write 1, the transmit interrupt flag bit will be preset to 1, and the read value is always 0.	0
0	bU3RIS	WO	Write 1, the receive interrupt flag bit will be preset to 1, and the read value is always 0.	0

UART3 baud rate is generated by SBAUD3, and it can be divided into 2 cases according to bU3SMOD:
When bU3SMOD=0, SBAUD3 = 256 - Fsys / 32 / baud rate;
When bU3SMOD=1, SBAUD3 = 256 - Fsys / 16 / baud rate.

UART3 Interrupt Status Register (SIF3):

Bit	Name	Access	Description	Reset value
[7:2]	Reserved	RO	Reserved	000000b
1	bU3TI	RW	Transmit interrupt flag bit, set by hardware after a byte is transmitted. Write 1 to reset by software (writing 0 to this bit will be ignored).	0
0	bU3RI	RW	Receive interrupt flag bit, set by hardware after a byte is received effectively. Write 1 to reset by software (writing 0 to this bit will be ignored).	0

UART3 Data Register (SBUF3):

Bit	Name	Access	Description	Reset value
[7:0]	SBUF3	RW	UART3 data register, including physically separated transmit register and receive register. The transmit register is used to write data to SBUF3. The receive register is used to read data from SBUF3.	xxh

13.3 UART Application

UART0 application:
(1). Select UART0 baud rate generator from T1 or T2, and set counter.
(2). Enable T1 or T2.
(3). Set SM0, SM1, SM2 in SCON to select UART0 working mode. Set REN to 1 and enable UART0 receiver.
(4). Set UART interrupt or query R1 and T1 interrupt status.
(5). Read/write SBUF to receive/transmit data, and the allowed receive baud rate error should be not more than 2%.

UART1 application:
(1). Select bU1SMOD and set SBAUD1 based on the baud rate.
(2). Set bU1SM0 in SCON1 to select UART1 working mode. Set bU1REN to 1 and enable UART1 receiver.
(3). Set UART1 interrupt or query bU1RI and bU1TI interrupt status (only write 1 to the specified bit to reset).
(4). Read/write to SBUF1 to receive/transmit data, and the allowed baud rate error should be not more than 2%.

UART2 application (UART3 application):

(1). Select bU2SMOD and set SBAUD2 based on the baud rate.

(2). Set bU2SM0 in SCON2 to select UART2 working mode. Set bU2REN to 1 and enable UART2 receiver.

(3). Query bU2RI and bU2TI interrupt status (write 1 to the specified bit to reset), or enable UART2 interrupt and set bU2IE to 1 to replace ADC (PWMX for UART3) interrupt.

(4). Read/write to SBUF2 to receive/transmit data, and the allowed baud rate error should be not more than 2%.

14. Synchronous Serial Interface (SPI)

14.1 SPI Introduction

CH549 chip provides SPI interface for high-speed synchronous data transmission with peripherals.

(1). Support master mode and slave mode;

(2). Support mode0 and mode3 clock mode;

(3). Optional 3-wire full-duplex mode or 2-wire half-duplex mode;

(4). Optional MSB first or LSB first;

(5). Clock frequency is variable, up to half of the system clock frequency;

(6). Built-in 1-byte receiver FIFO and 1-byte transmitter FIFO;

(7). Support the first byte pre-load data in slave mode to facilitate the host to obtain the returned data immediately in the first byte.

14.2 SPI Register

Table 14.2.1 List of SPI registers

Name	Address	Description	Reset value
SPI0_SETUP	FCh	SPI0 setting register	00h
SPI0_S_PRE	FBh	SPI0 slave mode preset data register	20h
SPI0_CK_SE	FBh	SPI0 clock divisor setting register	20h
SPI0_CTRL	FAh	SPI0 control register	02h
SPI0_DATA	F9h	SPI0 data register	xxh
SPI0_STAT	F8h	SPI0 status register	08h

SPI0 Setup Register (SPI0_SETUP):

Bit	Name	Access	Description	Reset value
7	bS0_MODE_SLV	RW	SPI0 master/slave mode selection 0: Master mode; 1: Slave mode/device mode.	0
6	bS0_IE_FIFO_OV	RW	FIFO overflow interrupt enable in slave mode 1: FIFO overflow interrupt is enabled; 0: FIFO overflow will not result in interrupt.	0
5	bS0_IE_FIRST	RW	The first receive byte interrupt in slave mode enable: 1: The first receive byte will trigger interrupt in slave mode. 0: The first receive byte will not trigger interrupt.	0
4	bS0_IE_BYTE	RW	Data byte transfer completion interrupt enable: 1: Byte transfer completion interrupt is enabled. 0: Byte transfer completion interrupt will not result in interrupt.	0
3	bS0_BIT_ORDER	RW	Data byte bit order control: 0: MSB in first. 1: LSB in first.	0
2	Reserved	RO	Reserved	0

1	bS0_SLV_SELT	R0	CS activation status in slave mode: 0: Not selected at present. 1: Selected at present.	0
0	bS0_SLV_PRELOAD	R0	Preload data state in slave mode 1: It is in preload state before data transmission while CS is valid	0

SPI0 Clock Divisor Setting Register (SPI0_CK_SE):

Bit	Name	Access	Description	Reset value
[7:0]	SPI0_CK_SE	RW	SPI0 clock divisor setting in master mode	20h

SPI0 Slave Mode Preset Data Register (SPI0_S_PRE)

Bit	Name	Access	Description	Reset value
[7:0]	SPI0_S_PRE	RW	Pre-load first transfer data in slave mode	20h

SPI0 Control Register (SPI0_CTRL):

Bit	Name	Access	Description	Reset value
7	bS0_MISO_OE	RW	SPI0 MISO output enable: 1: Enable output. 0: Disable output.	0
6	bS0_MOSI_OE	RW	SPI0 MOSI output enable: 1: Enable output. 0: Disable output.	0
5	bS0_SCK_OE	RW	SPI0 SCK output enable: 1: Enable output. 0: Disable output.	0
4	bS0_DATA_DIR	RW	SPI0 data direction: 0: Output data, only regard FIFO writing as valid operation, start a SPI transmission. 1: Input data, reading or writing FIFO are all valid, start a SPI transmission.	0
3	bS0_MST_CLK	RW	SPI0 master clock mode: 0: Mode0, default low level when SCK is free. 1: Mode3, SCK default high level.	0
2	bS0_2_WIRE	RW	SPI0 2-wire half-duplex mode enable: 0: 3-wire full-duplex mode, including SCK, MOSI, and MISO. 1: 2-wire half-duplex mode, including SCK, MISO.	0
1	bS0_CLR_ALL	RW	1: Clear SPI0 interrupt flag and FIFO. Reset by software.	1
0	bS0_AUTO_IF	RW	Clear byte receiving completion interrupt flag automatically by FIFO valid operation enable bit: 1: It will clear byte receiving completion interrupt flag	0

			S0_IF_BYTE automatically when there is valid FIFO read/write operation.	

SPI0 Data Register (SPI0_DATA):

Bit	Name	Access	Description	Reset value
[7:0]	SPI0_DATA	RW	Including physically separated receive FIFO and transmit FIFO. The receive FIFO is used for read operation. The transmit FIFO is used for write operation. SPI transmission can be started by valid read/write operation	xxh

SPI0 Status Register (SPI0_STAT):

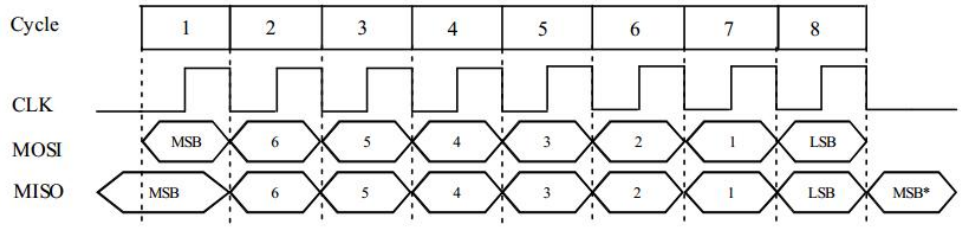
Bit	Name	Access	Description	Reset value
7	S0_FST_ACT	R0	1: First byte has been received in slave mode	0
6	S0_IF_OV	RW	FIFO overflow flag in slave mode: 1: FIFO overflow interrupt. 0: No interrupt Directly write 0 to reset, or write 1 to the corresponding bit in the register to reset. Transmit FIFO empty triggers interrupt when bS0_DATA_DIR=0. Receive FIFO full triggers interrupt when bS0_DATA_DIR=1.	0
5	S0_IF_FIRST	RW	The first byte received completion interrupt flag in slave mode: 1: The first byte has been received. Directly write 0 to reset, or write 1 to the corresponding bit in the register to reset.	0
4	S0_IF_BYTE	RW	Data byte transfer completion interrupt flag 1: One byte has been transferred. Directly write 0 to reset, or write 1 to the corresponding bit in the register to reset. Valid FIFO operation while bS0_AUTO_IF=1 can also reset it.	0
3	S0_FREE	R0	SPI0 free flag 1: No SPI shifting at present, usually in free period between data bytes.	1
2	S0_T_FIFO	R0	SPI0 transmit FIFO count, the valid value is 0 or 1	0
1	Reserved	R0	Reserved	0
0	S0_R_FIFO	R0	SPI0 receive FIFO count, the valid value is 0 or 1	0

14.3 SPI Transfer Format

SPI host mode supports mode 0 and mode 3, which can be selected by setting the bit bSn_MST_CLK in the SPI control register SPIn_CTRL. CH549 always samples MISO data at the rising edge of CLK. The data transmission format is shown in the following figure.

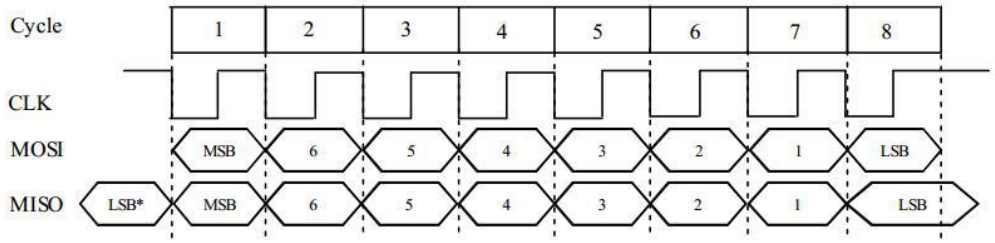
Mode0: bSn_MST_CLK = 0

Figure 14.3.1 SPI mode0 timing diagram



Mode3: bSn_MST_CLK = 1

Figure 14.3.2 SPI mode3 timing diagram



14.4 SPI Configuration

14.4.1 SPI Master Mode Configuration

In SPI host mode, the SCK pin outputs a serial clock, and the chip-selected output pin can be specified as any I/O pin.

SPI0 configuration steps:

(1) Set the SPI clock frequency division setting register SPI0_CK_SE and configure the SPI clock frequency.

(2) Set the bit bS0_MODE_SLV of the SPI setting register SPI0_SETUP to 0 and configure it in host mode.

(3) Set the bit bS0_MST_CLK of the SPI control register SPI0_CTRL to mode 0 or 3 as needed.

(4) Set the bit bS0_SCK_OE and bS0_MOSI_OE of SPI control register SPI0_CTRL to 0, set P1 port direction bSCK and bMOSI as output, bMISO as input, and chip selection pin as output.

Data transmission process:

(1) Write the SPI0_DATA register, write the data to be transmitted to the FIFO, and automatically start a SPI transfer.

(2) Waiting for the S0_FREE to be 1 means that the sending is complete, and you can continue to send the next byte.

Data reception process:

(1) Write the SPI0_DATA register and write any data such as 0FFh to the FIFO to initiate a SPI transfer.

(2) Waiting for the S0_FREE to be 1 means that the reception is complete, and the SPI0_DATA can be read to get the received data.

(3) If bS0_DATA_DIR is previously set to 1, the above read operation will also start the next SPI transfer, otherwise it will not start.

14.4.2 SPI Slave Mode Configuration

Only SPI0 supports slave mode, where the SCK pin is used to receive the serial clock of the connected SPI host.

(1) Set the bit bS0_MODE_SLV of the SPI0 setting register SPI0_SETUP to 1 and configure it in slave mode.

(2) Set the bits bS0_SCK_OE and bS0_MOSI_OE of SPI0 control register SPI0_CTRL to 0, set bS0_MISO_OE

to 1, set P1 port direction bSCK, bMOSI and bMISO and chip selection pins as inputs. When the SCS chip is selected as valid (low level), the MISO will automatically enable the output. At the same time, it is recommended to set the MISO pin to the high resistance input mode (P1_MOD_OC [6] = 0, P1_DIR_PU [6] = 0), so that the MISO will not output during the invalid chip selection, so that it is convenient to share the SPI bus.

(3) Optionally, set the SPI slave mode preset data register SPI0_S_PRE, which is automatically loaded into the buffer for external output for the first time after being selected by the chip. After 8 serial clocks, that is, the first data byte is transferred and exchanged, the CH549 gets the first byte of data sent by the external SPI host (possibly a command code), and the external SPI host exchanges the preset data (possibly the status value) in the SPI0_S_PRE. The bit 7 of register SPI0_S_PRE will be automatically loaded on the MISO pin during the low level of SCK after the SPI chip selection is valid. for SPI mode 0, if CH549 presets bit 7 of SPI0_S_PRE, then the external SPI host will be able to get the preset value of bit 7 of SPI0_S_PRE by querying the MISO pin when the SPI chip selection is valid but has not yet transferred data. Thus the value of bit 7 of SPI0_S_PRE can be obtained by simply validating the SPI chip selection.

Data transmission process:

Query S0_IF_BYTE or wait for an interrupt. After each SPI data byte transfer is complete, write the SPI0_DATA register and write the data to be sent to FIFO. Or wait for S0_FREE to change from 0 to 1, and then continue to send the next byte.

Data reception process:

Query the S0_IF_BYTE or wait for the interrupt. After each SPI data byte transfer is complete, read the SPI0_DATA register to get the received data from the FIFO. Query S0_R_FIFO to know if there are any remaining bytes in the FIFO.

15. Analog to Digital Converter (ADC) and Touch-key (TKEY)

15.1 Introduction to ADC and CMP

CH549 chip provides 12-bit analog-to-digital converter, including ADC and CMP module.

The ADC has 16 external analog signal input channels and 4 internal input channels (reference voltage), which can be collected time-sharing and support the analog input voltage range from 0 to VDD.

The forward input of the CMP reuses the above ADC input, and the inverse input has two external analog signal input channels and two internal reference voltage input channels, which can be compared in time sharing. There are more than 68 kinds of cross combinations, and the analog input voltage range from 0 to VDD is supported.

15.2 ADC and CMP Register

Table 15.2.1 List of ADC registers

Name	Address	Description	Reset value
ADC_CTRL	F2h	ADC control and status register	xxh
ADC_CFG	F3H	ADC configuration register	00h
ADC_DAT_H	F5h	ADC result data high byte (read only)	0xh
ADC_DAT_L	F4h	ADC result data low byte (read only)	xxh
ADC_DAT	F4h	16-bit SFR consists of ADC_DAT_L and ADC_DAT_H	0xxxh
ADC_CHAN	F6h	ADC analog signal channel selection register	00h
ADC_PIN	F7h	ADC pin digital input control register	00h

ADC Control and Status Register (ADC_CTRL):

Bit	Name	Access	Description	Reset value
7	bCMPDO	RO	CMP result output bit after synchronous delay, the status of bCMPO after synchronous delay with bCMP_IF	x
6	bCMP_IF	RW	CMP result change interrupt flag 1: CMP result has changed. Write 1 to reset.	0
5	bADC_IF	RW	ADC conversion completion interrupt flag 1: An ADC conversion is completed. Write 1 to reset or write TKEY_CTRL to reset.	0
4	bADC_START	RW	ADC start control, set 1 to start an ADC conversion. Reset automatically at the end of ADC conversion.	0
3	bTKEY_ACT	RO	Touch-key detection activation state 1: Capacitor is being charged and the ADC is being measured.	0
[2:1]	Reserved	R0	Reserved	00b
0	bCMPO	RO	CMP result real-time output 0: Voltage on positive input is lower than voltage on inverted input. 1: Voltage on positive input is higher than voltage on inverted input.	x

ADC Configuration Register (ADC_CFG):

Bit	Name	Access	Description	Reset value
[7:6]	Reserved	R0	Reserved	00b
5	bADC_AIN_EN	RW	CMP positive input and ADC input channel external AIN enable 1: One of 16 AIN is selected by MASK_ADC_CHAN. 0: Disable external AIN.	0
4	bVDD_REF_EN	RW	Internal reference voltage enable 1: Internal reference voltage is generated by multiple series resistors to the supply voltage. 0: Disable divider resistance.	0
3	bADC_EN	RW	ADC power control 0: ADC power off, and enter sleep state. 1: ADC power on.	0
2	bCMP_EN	RW	CMP power control 0: CMP power off, and enter sleep state. 1: CMP power on. At the same time, the wake-up function of the voltage comparator is automatically enabled, and if the comparator results in reverse changes during sleep, it will wake up automatically.	0
1	bADC_CLK1	RW	ADC reference clock frequency selection high bit	0
0	bADC_CLK0	RW	ADC reference clock frequency selection low bit	0

Table 15.2.2 ADC reference clock frequency selection

bADC_CLK1	bADC_CLK0	ADC reference clock frequency	Time required to complete an ADC	Applicable scope
0	0	750KHz	512 Fosc	Rs<=16KΩ or Cs>=0.08uF
0	1	1.5MHz	256 Fosc	Rs<=8KΩ or Cs>=0.08uF
1	0	3MHz	128 Fosc	VDD>=3V and (Rs<=4KΩ or Cs>=0.08uF)
1	1	6MHz	64 Fosc	VDD>=4.5V and (Rs<=2KΩ or Cs>=0.08uF)

Note: VDD refers to the power supply voltage, Cs refers to the parallel capacitance of the signal source, and Rs refers to the series internal resistance of the signal source (sampling time is only 3 reference clocks). The internal resistance of the internal reference voltage channel is large, so it is recommended to use a slower reference clock, or to abandon the previous data after multiple sampling.

ADC Analog Signal Channel Selection Register (ADC_CHAN):

Bit	Name	Access	Description	Reset value
[7:6]	MASK_CMP_CHAN	RW	CMP inverted input signal channel selection	00b
[5:4]	MASK_ADC_I_CH	RW	CMP positive input and ADC input internal signal channel selection	00b
[3:0]	MASK_ADC_CHAN	RW	The CMP positive input and the ADC input external signal channel are selected when bADC_AIN_EN=1,	0000b

			and the external signal channel is closed when bADC_AIN_EN=0.	

Table 15.2.3 CMP inverted input signal channel selection

bCMP_EN	bVDD_REF_EN	MASK_CMP_CHAN	CMP inverted input signal channel selection
0	x	xxb	Disconnect signal channel, suspended
1	0	00b	Disconnect signal channel, suspended
1	1	00b	Connect to internal reference voltage: 12.5% of VDD voltage
1	0	01b	Connect to internal reference voltage: 100% of VDD voltage
1	1	01b	Connect to internal reference voltage: 25% of VDD voltage
1	x	10b	Connect to external signal AIN1 (P1.1)
1	x	11b	Connect to external signal AIN2 (P1.2)

Table 15.2.4 CMP positive input and ADC input internal signal channel selection

bADC_EN	bADC_AIN_EN	bVDD_REF_EN	MASK_ADC_I_CH	CMP positive input and ADC input internal signal channel selection
x	x	0	00b	Disconnect internal signal channel, suspended
x	x	1	00b	Connect to internal reference voltage: 50% of VDD voltage
x	x	x	01b	Connect to internal reference voltage: V33 voltage
x	x	x	10b	Connect to internal voltage/with noise: 54.5% of V33 voltage
1	0	x	11b	Connect to internal signal: temperature sensor (TS), Please refer to the C example program for details
0	x	x	11b	Disconnect internal signal channel, suspended
x	1	x	11b	Disconnect internal signal channel, suspended

Table 15.2.5 CMP positive input and ADC input external signal channel selection

bADC_AIN_EN	MASK_ADC_CHAN	CMP positive input and ADC input external signal channel selection
0	xxxxb	Disconnect the external signal channel (AIN0~AIN15) , suspended
1	0000b	Connect to external signal AIN0 (P1.0)
1	0001b	Connect to external signal AIN1 (P1.1)
1	0010b	Connect to external signal AIN2 (P1.2)
1	0011b	Connect to external signal AIN3 (P1.3)
1	0100b	Connect to external signal AIN4 (P1.4)
1	0101b	Connect to external signal AIN5 (P1.5)

1	0110b	Connect to external signal AIN6 (P1.6)
1	0111b	Connect to external signal AIN7 (P1.7)
1	1000b	Connect to external signal AIN8 (P0.0)
1	1001b	Connect to external signal AIN9 (P0.1)
1	1010b	Connect to external signal AIN10 (P0.2)
1	1011b	Connect to external signal AIN11 (P0.3)
1	1100b	Connect to external signal AIN12 (P0.4)
1	1101b	Connect to external signal AIN13 (P0.5)
1	1110b	Connect to external signal AIN14 (P0.6)
1	1111b	Connect to external signal AIN15 (P0.7)

The voltage comparator CMP positive phase input and ADC input can only connect internal signals or external signals, and can also connect internal signals and external signals at the same time. When the internal and external signals are connected at the same time, the internal and external signals will communicate with each other, the turn-on resistance will be a series of 2 Rsw, and the internal reference voltage (with its internal resistance) will be connected to the external signal pin AIN0~AIN15 through the above 2 Rsw resistors, which is equivalent to providing a specific voltage pull-up resistance for the signal pin.

Ca is a sampling capacitor with a capacity of about 15pF. The resistance ratio of R2/R1 is 54.5 : 45.5. The 4R/2R/R resistance ratio is 4:2:1.

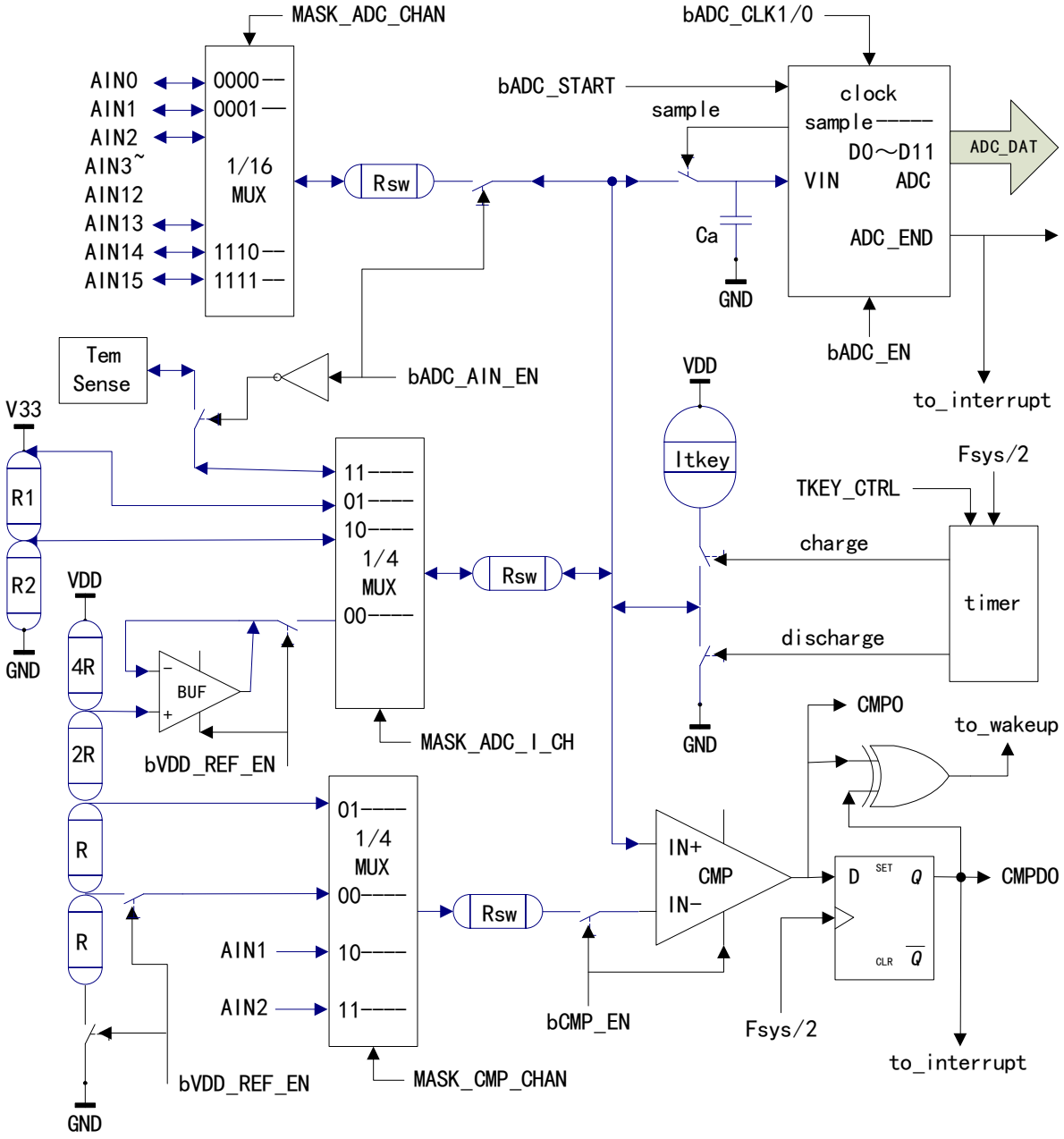
ADC Data Register (ADC_DAT):

Bit	Name	Access	Description	Reset value
[7:0]	ADC_DAT_H	RO	High byte of ADC sampling result data	0xh
[7:0]	ADC_DAT_L	RO	Low byte of ADC sampling result data	xxh

ADC Pin Digital Input Control Register (ADC_PIN):

Bit	Name	Access	Description	Reset value
7	bAIN14_15_DI_DIS	RW	AIN14 and AIN15 digital input disable 0: AIN14 and AIN15 digital input enabled.	0
6	bAIN12_13_DI_DIS	RW	AIN12 and AIN13 digital input disable 0: AIN12 and AIN13 digital input enabled.	0
5	bAIN10_11_DI_DIS	RW	AIN10 and AIN11 digital input disable 0: AIN10 and AIN11 digital input enabled.	0
4	bAIN8_9_DI_DIS	RW	AIN8 and AIN9 digital input disable 0: AIN8 and AIN9 digital input enabled.	0
3	bAIN6_7_DI_DIS	RW	AIN6 and AIN7 digital input disable 0: AIN6 and AIN7 digital input enabled.	0
2	bAIN4_5_DI_DIS	RW	AIN4 and AIN5 digital input disable 0: AIN4 and AIN5 digital input enabled.	0
1	bAIN2_3_DI_DIS	RW	AIN2 and AIN3 digital input disable 0: AIN2 and AIN3 digital input enabled.	0
0	bAIN0_1_DI_DIS	RW	AIN0 and AIN1 digital input disable 0: AIN0 and AIN1 digital input enabled.	0

Figure 15.2.1 ADC/CMP/TKEY structure diagram (blue lines to represent analog signals)



15.3 TKEY Register

Table 15.3.1 List of TKEY registers

Name	Address	Description	Reset value
TKEY_CTRL	F1h	Touch key charging pulse width control register	00h

Touchkey Charging Pulse Width Control Register (TKEY_CTRL):

Bit	Name	Access	Description	Reset value
[7:0]	TKEY_CTRL	WO	Touch key charging pulse width value, only the lower 7 bits are valid, counted in 2 times the system period (2/Fsys), the ADC is automatically activated to measure the voltage on the capacitor when timed.	00h

15.4 ADC and Touch-Key Function

ADC sampling mode configuration steps:

(1) Set the bADC_EN bit in the ADC_CFG register to 1, open the ADC module, and set the bADC_CLK0/1 selection frequency.

(2) Set the MASK_ADC_CHAN or MASK_ADC_I_CH in the ADC_CHAN register and select the external or internal signal channel.

(3) Optional, clear the interrupt flag bADC_IF. Optionally, if you use interrupt mode, you also need to enable interrupts here.

(4) Set the bADC_START in the ADC_CTRL register to start an ADC conversion.

(5) Wait for bADC_START to change to 0, or bADC_IF is set to 1 (if it was previously cleared), indicating that the ADC conversion is over, and the result data can be read through ADC_DAT. This data is the value of 4095 parts of the input voltage relative to the VDD power supply voltage. For example, the result data is 475, indicating that the input voltage is close to 475/4095 of the VDD voltage. If the VDD power supply voltage is uncertain, then another determined reference voltage value can be measured, and then the measured input voltage value and the VDD power supply voltage value can be calculated proportionally.

(6) If you set bADC_START again, you can start the next ADC conversion.

(7) If the higher ADC reference clock frequency leads to shorter sampling time, or the signal source series internal resistance is larger, or the supply voltage is lower, the Rsw internal resistance is larger, then it is possible that the Ca cannot sample enough signal voltage, which affects the ADC result. The solution is to discard the first ADC data, start the second ADC immediately and use its ADC result data, which is equivalent to sampling twice.

(8) When the precision is high, it is recommended to calibrate before use and use software to eliminate the inherent deviation.

CMP mode configuration steps:

(1) Set the bCMP_EN bit in the ADC_CFG register to 1 and open the voltage comparator module.

(2) Set the MASK_ADC_CHAN, MASK_CMP_CHAN and MASK_ADC_I_CH in the ADC_CHAN register, and select the positive input and inverse input signals respectively. You can choose a variety of combinations, such as AIN0~AIN15 and AIN1/AIN2 comparison, AIN0~AIN15 and internal reference voltage comparison, AIN1/AIN2 and internal reference voltage comparison and so on.

(3) Optional, clear the interrupt flag bCMP_IF. Optionally, if you use interrupt mode, you also need to enable interrupts here.

(4) The status of the bCMPO bit can be queried at any time to get the results of the current comparator.

(5) If bCMP_IF changes to 1, the result of the comparator has changed.

Touch-Key detection steps:

(1) Set the bADC_EN bit in the ADC_CFG register to 1, open the ADC module, and set the bADC_CLK0/1 selection frequency.

(2) Set the MASK_ADC_CHAN in the ADC_CHAN register and select the touch button signal channel.

(3) According to the actual capacitance of the touch button, the appropriate charging pulse width is selected and written into the TKEY_CTRL register. The simple calculation formula is as follows (assuming the external capacitance of the touch button Ckey=25pF, assuming VDD=5V, assuming Fsys=12MHz, rough calculation):
count=(Ckey+Cint)*0.7VDD/ITKEY/(2/Fsys)=(25p+15p)*0.35*5*12M/50u=17
TKEY_CTRL=count > 127 ? 127 : count

(4) Optionally, if you use interrupt mode, you also need to enable interrupts here.

(5) When the touch button capacitor charging time is up, CH549 automatically sets bADC_START to start ADC to measure the voltage on the capacitor.
(6) Wait for bTKEY_ACT to change to 0, or bADC_IF is set to 1, indicating the end of charging and ADC conversion, and the result data can be read through ADC_DAT. The software compares the value with the value when there is no key before, and determines whether the touch button is pressed or not according to the change of capacitance.
(7) Go to step (2) as needed and select another touch button signal channel for detection.
(8) If the actual capacitance of the touch button is greater than 40pF or the main frequency is one of 48MHz and 6MHz, then the internal automatic discharge time may be insufficient, and it may be necessary to discharge the above capacitance at a low level around the output 1uS of the GPIO.

The GPIO pin of the selected external analog signal channel must be set to high resistance input mode or open-drain output mode and in the state of output 1 (equivalent to high resistance input), Pn_DIR_ pu [x] = 0, and turn off pull-up resistance and pull-down resistance.

16. USB Controller

16.1 USB Introduction

CH549 has built-in USB controller and USB transceiver with the following features:

(1) Support USB Host functions and USB Device functions

(2) Support USB 2.0 full-speed 12Mbps or low-speed 1.5Mbps

(3) Support USB control transfer, batch transfer, interrupt transmission, synchronous/real-time transmission

(4) Support up to 64 bytes of packets, built-in FIFO, support interrupts and DMA.

The USB related registers of CH549 are divided into three parts, some of which are reused in host and device mode.

(1) USB global register;

(2) USB device controller register

(3) USB host controller register

16.2 Global Register

Table 16.2.1 USB global registers (those marked in grey are controlled by bUC_RESET_SIE reset)

Name	Address	Description	Reset value
USB_C_CTRL	91h	USB type-C configuration channel control register	0000 0000b
USB_INT_FG	D8h	USB interrupt flag register	0010 0000b
USB_INT_ST	D9h	USB interrupt status register (read-only)	00xx xxxxb
USB_MIS_ST	DAh	USB miscellaneous status Register (read-only)	xx10 1000b
USB_RX_LEN	DBh	USB receive length register (read-only)	0xxx xxxxb
USB_INT_EN	E1h	USB interrupt enable register	0000 0000b
USB_CTRL	E2h	USB control register	0000 0110b
USB_DEV_AD	E3h	USB device address register	0000 0000b

USB Type-C Configuration Channel Control Register (USB_C_CTRL):

Bit	Name	Access	Description	Reset value
7	bUCC_PD_MOD	RW	1: Enable USB PD BMC protocol output mode for UCC1 and UCC2 pins; 0: Disable.	0
6	bUCC2_PD_EN	RW	1: Enable the internal 5.1K pull-down resistance of the UCC2 pin; 0: Disable.	0
5	bUCC2_PU1_EN	RW	This bit is the internal pull-up resistance control high bit of the UCC2 pin.	0
4	bUCC2_PU0_EN	RW	This bit is the internal pull-up resistance control of the UCC2 pin to select the low bit	0
3	bVBUS_PD_EN	RW	1: Enable the internal 10K pull-down resistance of the VBUS pin; 0: Disable.	0
2	bUCC1_PD_EN	RW	1: Enable the internal 5.1K pull-down resistance of the UCC1 pin; 0: Disable.	0

1	bUCC1_PU1_EN	RW	This bit is the internal pull-up resistance control high bit of the UCC1 pin.	0
0	bUCC1_PU0_EN	RW	This bit is the internal pull-up resistance control of the UCC1 pin to select the low bit	0

The pull-up resistor inside the UCCn pin is selected by bUCCn_PU1_EN and bUCCn_PU0_EN.

bUCCn_PU1_EN	bUCCn_PU0_EN	Select the pull-up resistor inside the UCCn pin
0	0	Internal pull-up resistors are prohibited
0	1	Enable internal 56K Ω pull-up resistor, which means that a default USB current is provided
1	0	Enable internal 22K Ω pull-up resistor, indicating that 1.5A current can be provided
1	1	Enable internal 10K Ω pull-up resistor, indicating that 3A current can be provided

The above USB type-C pull-up resistors and pull-down resistors are independent of the port pull-up resistors controlled by the Pn_DIR_PU port direction control and pull-up enable registers. When a pin is used for USB type-C, the port pull-up resistor corresponding to the pin should be disabled, and it is recommended to enable the high-resistance input mode (to avoid the output of this pin to be either low or high) for this pin.

For detailed control and input detection of USBtype-C configuration channel, please refer to USBtype-C application instructions and routines; for USBPD power transmission control and CRC processing, please refer to USBPD subroutines, application instructions and routines. CH543 chip is recommended.

USB Interrupt Flag Register (USB_INT_FG):

Bit	Name	Access	Description	Reset value
7	U_IS_NAK	RO	1: Receive NAK busy response during current USB transfer. 0: Receive non-NAK response.	0
6	U_TOG_OK	RO	The current USB transfer DATA0/1 synchronization flag matching status 1: Indicates synchronization and valid data; 0: Indicates lack of synchronization and potentially invalid data.	0
5	U_SIE_FREE	RO	The idle status bit of the USB protocol processor 0: Busy, indicating an ongoing USB transfer; 1: USB idle.	1
4	UIF_FIFO_OV	RW	USB FIFO overflow interrupt flag 1: FIFO overflow interrupt. 0: No interrupt. Directly write 0 to reset, or write 1 to the corresponding bit in the register to reset.	0
3	UIF_HST_SOF	RW	USB SOF timing interrupt flag 1: SOF timing interrupt flag. The interrupt is triggered by the completion of SOF packet transmission. 0: No interrupt. Directly write 0 to reset, or write 1 to the corresponding bit in the register to reset.	0
2	UIF_SUSPEND	RW	USB bus suspend or wake-up event interrupt flag	0

			1: There is an interrupt, triggered by USB suspend event or wake-up event. 0: No interrupt. Directly write 0 to reset, or write 1 to the corresponding bit in the register to reset.	
1	UIF_TRANSFER	RW	USB transfer completion interrupt flag 1: There is an interrupt, triggered by USB transfer completion. 0: No interrupt. Directly write 0 to reset, or write 1 to the corresponding bit in the register to reset.	0
0	UIF_DETECT	RW	USB device connect or disconnect event interrupt flag 1: There is an interrupt, triggered by USB device connect or disconnect. 0: No interrupt. Directly write 0 to reset, or write 1 to the corresponding bit in the register to reset.	0
0	UIF_BUS_RST	RW	USB bus reset event interrupt flag 1: There is an interrupt, triggered by USB bus reset event. 0: No interrupt. Directly write 0 to reset, or write 1 to the corresponding bit in the register to reset.	0

USB Interrupt Status Register (USB_INT_ST):

Bit	Name	Access	Description	Reset value
7	bUIS_IS_NAK	RO	1: Receive NAK busy response during current USB transfer. The same as U_IS_NAK	0
6	bUIS_TOG_OK	RO	Current USB transfer DATA0/1 synchronization flag match state 1: Synchronization. 0: Out of synchronization. The same as U_TOG_OK	0
5	bUIS_TOKEN1	RO	Current USB transmission transaction token PID high bit	x
4	bUIS_TOKEN0	R0	Current USB transmission transaction token PID low bit	x
[3:0]	MASK_UIS_ENDP	RO	Endpoint serial number of the current USB transfer transaction 0000: Endpoint 0. ... 1111: Endpoint 15.	xxxxb
[3:0]	MASK_UIS_H_RES	R0	Response PID flag of current USB transfer 0000: No response or overtime; Others: Response to PID.	xxxxb

bUIS_TOKEN1 and bUIS_TOKEN0 make up MASK_UIS_TOKEN, the token PID used to identify the current USB transmission transaction in USB device mode: 00 for OUT packets; 01 for SOF packets; 10 for IN packets; 11 for SETUP packets.

USB Miscellaneous Status Register (USB_MIS_ST):

Bit	Name	Access	Description	Reset value
7	bUMS_SOF_PRES	RO	In USB host mode, the SOF packet indicates a status bit. 1: Indicates that the SOF packet will be sent. If there are other USB packets, it will be automatically delayed.	x
6	bUMS_SOF_ACT	RO	SOF packet transfer status in USB host mode 1: SOF package is transmitting out; 0: Transmit completed or idle.	x
5	bUMS_SIE_FREE	RO	USB SIE free state 0: Busy, and USB transfer is in progress. 1: Free. The same as U_SIE_FREE	1
4	bUMS_R_FIFO_RDY	RO	USB receive FIFO data ready state 0: Receive FIFO is empty. 1: Receive FIFO is not empty.	0
3	bUMS_BUS_RESET	RO	USB bus reset status 0: No USB bus reset at present. 1: USB bus reset is in progress.	1
2	bUMS_SUSPEND	RO	USB suspend status 0: There is USB activity at present. 1: No USB activity for some time, and request to be suspended.	0
1	bUMS_DM_LEVEL	RO	Record the status of the DM pin when the USB device is just connected to the USB port in USB host mode 0: Low level; 1: High level. Used to judge whether full-speed or low-speed	0
0	bUMS_DEV_ATTACH	RO	USB device connection status bit in USB host mode 1: The port is already connected to the USB device; 0: Not connected.	0

USB Receiving Length Register (USB_RX_LEN):

Bit	Name	Access	Description	Reset value
[7:0]	bUSB_RX_LEN	RO	The number of bytes received by USB endpoint currently	xxh

USB Interrupt Enable Register (USB_INT_EN):

Bit	Name	Access	Description	Reset value
7	bUIE_DEV_SOF	RW	1: Enable receiving SOF packet interrupt. 0: Disable.	0
6	bUIE_DEV_NAK	RW	1: Enable receiving NAK interrupt. 0: Disable.	0
5	Reserved	RO	Reserved	0
4	bUIE_FIFO_OV	RW	1: Enable FIFO overflow interrupt. 0: Disable.	0

3	bUIE_HST_SOF	RW	1: Enable USB host mode SOF timing interrupt; 0: Disable.	0
2	bUIE_SUSPEND	RW	1: Enable USB bus suspend or wake-up event interrupt. 0: Disable.	0
1	bUIE_TRANSFER	RW	1: Enable USB transfer completion interrupt. 0: Disable.	0
0	bUIE_DETECT	RW	1: Enable USB device connect or disconnect event interrupt in USB host mode; 0: Disable.	0
0	bUIE_BUS_RST	RW	1: Enable USB bus reset event interrupt. 0: Disable.	0

USB Control Register (USB_CTRL)

Bit	Name	Access	Description	Reset value
7	bUC_HOST_MODE	RW	USB work mode selection 0: Select USB DEVICE mode; 1: Select USB HOST mode	0
6	bUC_LOW_SPEED	RW	USB bus speed selection 0: Full-speed (12Mbps). 1: Low-speed (1.5Mbps).	0
5	bUC_DEV_PU_EN	RW	USB device enable and internal pull-up resistor enable 1: Enable USB device transfer and enable internal pull-up resistor.	0
5	bUC_SYS_CTRL1	RW	USB system control high bit	0
4	bUC_SYS_CTRL0	RW	USB system control low bit	0
3	bUC_INT_BUSY	RW	Auto pause enable bit before USB transfer completion interrupt flag is not reset 1: Auto pause and respond busy NAK before UIF_TRANSFER is not reset. 0: Not pause.	0
2	bUC_RESET_SIE	RW	USB SIE software reset control 1: Force reset USB SIE and most of USB control registers. Reset by software.	1
1	bUC_CLR_ALL	RW	1: Clear USB interrupt flag and FIFO. Reset by software.	1
0	bUC_DMA_EN	RW	1: Enable USB DMA and DMA interrupt. 0: Disable.	0

USB system control consists of bUC_SYS_CTRL1 and bUC_SYS_CTRL0.

bUC_HOST_MODE	bUC_SYS_CTRL1	bUC_SYS_CTRL0	USB system control description
0	0	0	Disable USB device function and turn off internal

			pull-up resistor
0	0	1	Enable USB device function, turn off internal pull-up, add external pull-up
0	1	X	Enable USB device function, enable internal 1.5KΩ pull-up resistor. The pull-up resistance takes precedence over the pull-down resistance and can also be used in GPIO mode.
1	0	0	Select USB host mode, normal working state
1	0	1	Select USB host mode to force DP/DM to output SE0 status
1	1	0	Select USB host mode to force DP/DM to output J status
1	1	1	Select USB host mode to force DP/DM to output K status / Wake up

USB Device Address Register (USB_DEV_AD):

Bit	Name	Access	Description	Reset value
7	bUDA_GP_BIT	RW	USB general-purpose flag. User-defined. Can be reset and set by software.	0
[6:0]	MASK_USB_ADDR	RW	The address of the currently operating USB device in host mode; the address of the USB device in device mode.	00h

16.3 Device Register

In USB device mode, CH549 provides five sets of bi-directional endpoints 0, 1, 2, 3, 4, and the maximum big data packet length of all endpoints is 64 bytes.

Endpoint 0 is the default endpoint that supports controlling transmission, transmitting and receiving sharing a 64-byte data buffer.

Endpoint 1, endpoint 2, and endpoint 3 each include a transmitting endpoint IN and a receiving endpoint OUT, each with an independent 64-byte or double 64-byte data buffer, which supports control transmission, batch transmission, interrupt transmission and real-time / synchronous transmission.

Endpoint 4 includes a transmitting endpoint IN and a receiving endpoint OUT, each with a separate 64-byte data buffer that supports control transmission, batch transmission, interrupt transmission and real-time / synchronous transmission.

Each set of endpoints has a control register UEPn_CTRL and a transmit length register UEPn_T_LEN (n=0/1/2/3/4), which are used to set the synchronous trigger bit of the endpoint, the response to OUT and IN transactions, the length of data sent, and so on.

The USB bus pull-up resistance necessary for USB devices can be set by the software at any time. When the bUC_DEV_PU_EN in the USB control register USB_CTRL is set to 1, CH549 connects the pull-up resistors for the DP pin or DM pin of the USB bus internally according to the bUD_LOW_SPEED, and enables the USB device function.

When a USB bus reset, a USB bus hang or wake-up event is detected, or when the USB successfully processes data transmission or data reception, the USB protocol processor will set the corresponding interrupt flag and generate an interrupt request. The application program can query and analyze the interrupt flag register USB_INT_FG directly or in the USB interrupt service program, and process the interrupt flag register USB_INT_FG according to

UIF_BUS_RST and UIF_SUSPEND; and, if the UIF_TRANSFER is valid, it needs to continue to analyze the USB interrupt status register USB_INT_ST and process it according to the current endpoint number MASK_UIS_ENDP and the current transaction token PID identification MASK_UIS_TOKEN. If the synchronization trigger bit bUEP_R_TOG of the OUT transaction of each endpoint is set in advance, then whether the synchronization trigger bit of the currently received data packet matches the synchronization trigger bit of the endpoint can be determined by U_TOG_OK or bUIS_TOG_OK. If the data is synchronized, the data is valid; if the data is not synchronized, the data should be discarded. After each interrupt of USB transmission or reception, the synchronization trigger bit of the corresponding endpoint should be modified correctly to synchronize the data packet sent next time and detect whether the data packet received next time is synchronized; in addition, the corresponding synchronization trigger bit can be flipped automatically after successful transmission or reception by setting bUEP_AUTO_TOG.

The data to be sent by each endpoint is in its own buffer, and the length of the data to be sent is independently set in the UEPn_T_LEN; the data received by each endpoint is in the respective buffer, but the length of the received data is in the USB receiving length register USB_RX_LEN, which can be distinguished according to the current endpoint number when the USB receives the interrupt.

Table 16.3.1 List of USB device registers (those marked in grey are controlled by RB_UC_RESET_SIE reset)

Name	Address	Description	Reset value
UDEV_CTRL	D1h	USB device physical port control register	00xx 0000b
UEP1_CTRL	D2h	Endpoint1 control register	0000 0000b
UEP1_T_LEN	D3h	Endpoint1 transmit length register	0xxx xxxxb
UEP2_CTRL	D4h	Endpoint2 control register	0000 0000b
UEP2_T_LEN	D5h	Endpoint2 transmit length register	0000 0000b
UEP3_CTRL	D6h	Endpoint3 control register	0000 0000b
UEP3_T_LEN	D7h	Endpoint3 transmit length register	0xxx xxxxb
UEP0_CTRL	DCh	Endpoint0 control register	0000 0000b
UEP0_T_LEN	DDh	Endpoint0 transmit length register	0xxx xxxxb
UEP4_CTRL	DEh	Endpoint4 control register	0000 0000b
UEP4_T_LEN	DFh	Endpoint4 transmit length register	0xxx xxxxb
UEP4_1_MOD	EAh	Endpoint1/4 mode control register	0000 0000b
UEP2_3_MOD	EBh	Endpoint2/3 mode control register	0000 0000b
UEP0_DMA_H	EDh	Endpoint0/4 buffer start address high byte	0000 0xxxb
UEP0_DMA_L	ECh	Endpoint0/4 buffer start address low byte	xxxx xxxxb
UEP0_DMA	ECh	16-bit SFR consists of UEP0_DMA_L and UEP0_DMA_H	0xxxh
UEP1_DMA_H	EFh	Endpoint1 buffer start address high byte	0000 0xxxb
UEP1_DMA_L	EEh	Endpoint1 buffer start address low byte	xxxx xxxxb
UEP1_DMA	EEh	16-bit SFR consists of UEP1_DMA_L and UEP1_DMA_H	0xxxh
UEP2_DMA_H	E5h	Endpoint2 buffer start address high byte	0000 0xxxb
UEP2_DMA_L	E4h	Endpoint2 buffer start address low byte	xxxx xxxxb
UEP2_DMA	E4h	16-bit SFR consists of UEP2_DMA_L and UEP2_DMA_H	0xxxh
UEP3_DMA_H	E7h	Endpoint3 buffer start address high byte	0000 0xxxb
UEP3_DMA_L	E6h	Endpoint3 buffer start address low byte	xxxx xxxxb
UEP3_DMA	E6h	16-bit SFR consists of UEP3_DMA_L and UEP3_DMA_H	0xxxh

USB Device Physical Port Control Register (UDEV_CTRL), controlled by bUC_RESET_SIE reset:

Bit	Name	Access	Description	Reset value
7	bUD_PD_DIS	RW	USB UDP/UDM pin internal pull-down resistor disable 1: Disable internal pull-down resistor. 0: Enable internal pull-down resistor. This bit also can be used in GPIO mode to provide pull-down resistor.	0
6	Reserved	RO	Reserved	0
5	bUD_DP_PIN	RO	Current UDP pin status 0: Low level. 1: High level.	x
4	bUD_DM_PIN	RO	Current UDM pin status 0: Low level. 1: High level.	x
3	Reserved	RO	Reserved	0
2	bUD_LOW_SPEED	RW	USB device physical port low-speed mode enable bit 1: Low-speed (1.5Mbps) mode. 0: Full-speed (12Mbps) mode.	0
1	bUD_GP_BIT	RW	USB device mode general-purpose flag User-defined. Can be reset and set by software.	0
0	bUD_PORT_EN	RW	USB device physical port enable 1: Enable physical port. 0: Disable physical port.	0

Endpoint n Control Register (UEPn_CTRL):

Bit	Name	Access	Description	Reset value
7	bUEP_R_TOG	RW	Expected data toggle flag of USB endpoint n receiver (SETUP/OUT): 1: Expected DATA1. 0: Expected DATA0.	0
6	bUEP_T_TOG	RW	Prepared data toggle flag of USB endpoint n transmitter (IN): 1: Transmit DATA1. 0: Transmit DATA0.	0
5	Reserved	RO	Reserved	0
4	bUEP_AUTO_TOG	RW	Auto toggle enable 1: Auto toggle. 0: Manual toggle. Only supports single-receive or single-transmit mode of endpoint1/2/3, not supported when RX_EN and TX_EN of an endpoint are 1.	0
3	bUEP_R_RES1	RW	High bit of handshake response type for USB endpoint n receiving (SETUP/OUT).	0
2	bUEP_R_RES0	RW	Low bit of handshake response type for USB endpoint n receiving (SETUP/OUT).	0
1	bUEP_T_RES1	RW	High bit of handshake response type for USB endpoint n	0

			transmittal (IN).	
0	bUEP_T_RES0	RW	Low bit of handshake response type for USB endpoint n transmittal (IN).	0

The MASK_UEP_R_RES, consisting of bUEP_R_RES1 and bUEP_R_RES0, is used to control how the receiver of endpoint n responds to SETUP/OUT transactions: 00 indicates reply ACK or ready; 01 indicates timeout / no response and is used to implement real-time / synchronous transmission of non-endpoint 0; 10 indicates reply NAK or busy; 11 indicates reply STALL or error.

The MASK_UEP_T_RES consisting of bUEP_T_RES1 and bUEP_T_RES0 is used to control how the sender of endpoint n responds to IN transactions: 00 indicates reply DATA0/DATA1 or data ready and expects ACK;01 to indicate reply DATA0/DATA1 and expect no response, which is used to achieve real-time / synchronous transmission of non-endpoint 0; 10 indicates reply NAK or busy; 11 indicates reply STALL or error.

Endpoint n Transmit Length Register (UEPn_T_LEN):

Bit	Name	Access	Description	Reset value
[7:0]	bUEPn_T_LEN	RW	Set the number of data bytes that USB endpoint n is ready to transmit (n = 0/1/3/4).	xxh
	bUEP2_T_LEN		Set the number of data bytes that USB endpoint 2 is ready to transmit	00h

USB Endpoint1/4 Mode Control Register (UEP4_1_MOD):

Bit	Name	Access	Description	Reset value
7	bUEP1_RX_EN	RW	USB endpoint1 receive (OUT) enable: 1: Enable. 0: Disable.	0
6	bUEP1_TX_EN	RW	USB endpoint1 transmit (IN) enable: 1: Enable. 0: Disable.	0
5	Reserved	RO	Reserved	0
4	bUEP1_BUF_MOD	RW	Endpoint1 data buffer mode control	0
3	bUEP4_RX_EN	R0	USB endpoint4 receive (OUT) enable: 1: Enable. 0: Disable.	0
2	bUEP4_TX_EN	RW	USB endpoint4 transmit (IN) enable: 1: Enable. 0: Disable.	0
[1:0]	Reserved	RO	Reserved	00b

The data buffer mode of USB endpoints 0 and 4 is controlled by a combination of bUEP4_RX_EN and bUEP4_TX_EN, as shown in the following table.

Table 16.3.2 Buffer mode of endpoint0 and endpoint4

bUEP4_RX_EN	bUEP4_TX_EN	Structure description: arrange from low to high with UEP0_DMA as the starting address
0	0	Endpoint 0 single 64 byte transceiver common buffer (IN and OUT)
1	0	Endpoint 0 single 64 byte transceiver common buffer; endpoint 4 single 64

		byte receive buffer (OUT)
0	1	Endpoint 0 single 64 byte send and receive common buffer; endpoint 4 single 64 byte send buffer (IN)
1	1	Endpoint 0 single 64 byte send and receive common buffer; Endpoint 4 single 64 byte receive buffer (OUT); Endpoint 4 single 64 byte send buffer (IN). All 192 bytes are arranged as follows: UEP0_DMA+0 address: shared by end point 0 transceiver UEP0_DMA+64 address: received by endpoint 4 UEP0_DMA+128 address: transmitted by endpoint 4

USB Endpoint2/3 Mode Control Register (UEP2_3_MOD):

Bit	Name	Access	Description	Reset value
7	bUEP3_RX_EN	RW	USB endpoint3 receive (OUT) enable: 1: Enable. 0: Disable.	0
6	bUEP3_TX_EN	RW	USB endpoint3 transmit (IN) enable: 1: Enable. 0: Disable.	0
5	Reserved	RO	Reserved	0
4	bUEP3_BUF_MOD	RW	Endpoint3 buffer mode control	0
3	bUEP2_RX_EN	R0	USB endpoint2 receive (OUT) enable: 1: Enable. 0: Disable.	0
2	bUEP2_TX_EN	RW	USB endpoint2 transmit (IN) enable: 1: Enable. 0: Disable.	0
1	Reserved	RO	Reserved	0
0	bUEP2_BUF_MOD	RW	Endpoint2 buffer mode control	0

The data buffer modes of USB endpoints 1, 2, and 3 are controlled by the combination of bUEPn_RX_EN and bUEPn_TX_EN and bUEPn_BUF_MOD (nasty 1, 2, 3), respectively, as shown in the table below. In the double 64-byte buffer mode, the first 64-byte buffer is selected according to bUEP_*_TOG=0 when USB data is transmitted, and the latter 64-byte buffer is selected according to bUEP_*_TOG=1 to realize automatic switching.

Table 16.3.3 Buffer mode of endpoint n (n=1/2/3)

bUEPn_RX_EN	bUEPn_TX_EN	bUEPn_BUF_MOD	Structure description: arrange from low to high with UEPn_DMA as the starting address
0	0	x	Disable endpoint, and disable UEPn_DMA buffer
1	0	0	Single 64-byte receiving buffer (OUT)
1	0	1	Double 64-byte receiving buffer, selected by bUEP_R_TOG.
0	1	0	Single 64-byte transmitting buffer (IN)
0	1	1	Double 64-byte transmitting buffer, selected by bUEP_T_TOG.
1	1	0	Single 64-byte receiving buffer; Single 64-byte

			transmitting buffer
1	1	1	Double 64-byte receiving buffer, selected by bUEP_R_TOG; Double 64-byte transmitting buffer, selected by bUEP_T_TOG. All 256-byte as follow: UEPn_DMA+0 address: endpoint receiving when bUEP_R_TOG=0; UEPn_DMA+64 address: endpoint receiving when bUEP_R_TOG=1; UEPn_DMA+128 address: endpoint transmitting when bUEP_T_TOG=0; UEPn_DMA+192 address: endpoint transmitting when bUEP_T_TOG=1

USB Endpoint n Buffer Start Address (UEPn_DMA) (n=0/1/2/3):

Bit	Name	Access	Description	Reset value
[7:0]	UEPn_DMA_H	RW	Endpoint n buffer start address high byte, only the low 3 bits are valid, and the high 5 bits are fixed to 0.	0xh
[7:0]	UEPn_DMA_L	RW	Endpoint n buffer start address low byte	xxh

Note: Length of buffer to receive data > = min (length of most big data packet that may be received + 2 bytes, 64 bytes)

16.4 Host Register

In USB host mode, CH549 provides a set of bi-directional host endpoints, including a transmitting endpoint OUT and a receiving endpoint IN. The maximum length of the packet is 64 bytes, supporting control transmission, batch transmission, interrupt transmission and real-time/synchronous transmission.

Each USB transaction initiated by the host endpoint automatically sets the interrupt flag UIF_TRANSFER at the end of the processing. The application program can directly query, or query and analyze the interrupt flag register USB_INT_FG in the USB interrupt service program, and carry out corresponding processing according to each interrupt flag. Moreover, if the UIF_TRANSFER is valid, then it is necessary to continue to analyze the USB interrupt status register USB_INT_ST and carry out corresponding processing according to the reply PID identification MASK_UIS_H_RES of the current USB transmission transaction.

If the synchronization trigger bit bUH_R_TOG of the IN transaction of the host receiving endpoint is set in advance, then whether the synchronization trigger bit of the currently received data packet matches the synchronization trigger bit of the host receiving endpoint can be judged by U_TOG_OK or bUIS_TOG_OK. If the data is synchronized, the data is valid; if the data is not synchronized, the data should be discarded. After each interrupt of USB transmission or reception, the synchronization trigger bit of the corresponding host endpoint should be modified correctly to synchronize the data packet transmitted next time and detect whether the data packet received next time is synchronized; in addition, the corresponding synchronization trigger bit can be flipped automatically after successful transmission or reception by setting bUEP_AUTO_TOG.

The USB host token setting register UH_EP_PID is the multiplexing of the USB endpoint 2 control register in the USB device mode, which is used to set the terminal number of the target device to be operated and the token PID packet identification of the USB transmission transaction. The data corresponding to the SETUP token and the OUT

token are provided by the host transmitting endpoint, the data to be transmitted is in the UH_TX_DMA buffer zone, and the length of the data to be transmitted is set in the UH_TX_LEN; the data corresponding to the IN token is returned by the target device to the host receiving endpoint, the received data is stored in the UH_RX_DMA buffer zone, and the received data length is stored in the USB_RX_LEN.

Table 16.4.1 List of USB host registers (those marked in grey are controlled by bUC_RESET_SIE reset)

Name	Address	Description	Reset value
UHOST_CTRL	D1h	USB host physical port control register	00xx 0000b
UH_SETUP	D2h	USB host auxiliary setting register	0000 0000b
UH_RX_CTRL	D4h	USB host receive endpoint control register	0000 0000b
UH_EP_PID	D5h	USB host token setting register	0000 0000b
UH_TX_CTRL	D6h	USB host transmit endpoint control register	0000 0000b
UH_TX_LEN	D7h	USB host transmit length register	0xxx xxxxb
UH_EP_MOD	EBh	USB host endpoint mode control register	0000 0000b
UH_RX_DMA_H	E5h	USB host receive buffer start address high byte	0000 0xxxb
UH_RX_DMA_L	E4h	USB host receive buffer start address low byte	xxxx xxxxb
UH_RX_DMA	E4h	16-bit SFR consists of UH_RX_DMA_L and UH_RX_DMA_H	0xxxh
UH_TX_DMA_H	E7h	USB host transmit buffer start address high byte	0000 0xxxb
UH_TX_DMA_L	E6h	USB host transmit buffer start address low byte	xxxx xxxxb
UH_TX_DMA	E6h	16-bit SFR consists of UH_TX_DMA_L and UH_TX_DMA_H	0xxxh

USB Host Physical Port Control Register (UHOST_CTRL), controlled by bUC_RESET_SIE reset:

Bit	Name	Access	Description	Reset value
7	bUH_PD_DIS	RW	USB host endpoint UDP/UDM pin internal pull-down disable 1: Disable; 0: Enable. This bit can also be used in GPIO mode to provide pull-down resistors	0
6	Reserved	RO	Reserved	0
5	bUH_DP_PIN	RO	Current UDP pin status 0: Low level. 1: High level.	x
4	bUH_DM_PIN	RO	Current UDM pin status 0: Low level. 1: High level.	x
3	Reserved	RO	Reserved	0
2	bUH_LOW_SPEED	RW	USB host physical port low-speed mode enable bit 1: Low-speed (1.5Mbps) mode. 0: Full-speed (12Mbps) mode.	0
1	bUH_BUS_RESET	RW	USB host port bus reset control bit 1: Force host port output USB bus reset; 0: 0 end output.	0

0	bUH_PORT_EN	RW	USB host port enable 1: Enable host port; 0: Disable host port. This bit is cleared automatically when the USB device is disconnected	0

USB Host Auxiliary Setting Register (UH_SETUP):

Bit	Name	Access	Description	Reset value
7	bUH_PRE_PID_EN	RW	Low-speed preamble PRE PID enable 1: Enable USB host to communicate with low-speed USB devices through external HUB; 0: Disable the low-speed preamble. There can be no HUB between the USB host and the low-speed USB device.	0
6	bUH_SOF_EN	RW	Auto generate SOF packet enable 1: SOF package is generated automatically by USB host. 0: It is not generated automatically, but it can be generated manually.	0
[5:0]	Reserved	RO	Reserved	00h

USB Host Receive Endpoint Control Register (UH_RX_CTRL):

Bit	Name	Access	Description	Reset value
7	bUH_R_TOG	RW	Synchronization triggers expected by the USB host receiver (processing IN transactions) 0: Expected DATA0; 1: Expected DATA1.	0
[6:5]	Reserved	RO	Reserved	00b
4	bUH_R_AUTO_TOG	RW	Auto flip the bUH_R_TOG enable control bit 1: bUH_R_TOG flag is automatically flipped after the USB host has successfully received it. 0: It does not flip automatically, but you can switch 0 manually.	0
3	Reserved	RO	Reserved	0
2	bUH_R_RES	RW	Response control bits of the USB host receiver to IN transactions 1: ACK or be ready; 0: No response, for real-time / synchronous transmission with non-endpoint 0 of the target device.	0
[1:0]	Reserved	RO	Reserved	00b

USB Host Token Setting Register (UH_EP_PID):

Bit	Name	Access	Description	Reset value
[7:4]	MASK_UH_TOKE	RW	Set the token PID package identity for this USB	0000b

	N		transport transaction	
[3:0]	MASK_UH_ENDP	RW	Set the endpoint number of the target device to be operated this time	0000b

USB Host Transmit Endpoint Control Register (UH_TX_CTRL):

Bit	Name	Access	Description	Reset value
7	Reserved	RO	Reserved	0
6	bUH_T_TOG	RW	Synchronous trigger bits prepared by the USB host sender (processing SETUP/OUT transactions) 0: Transmit DATA0; 1: Transmit DATA1.	0
5	Reserved	RO	Reserved	0
4	bUH_T_AUTO_TOG	RW	Auto flip the bUH_T_TOG enable control bit 1: Auto flip the bUH_T_TOG flag after the USB host has successfully transmitted it; 0: Does not flip automatically, but can be switched manually	0
[3:1]	Reserved	RO	Reserved	000b
0	bUH_T_RES	RW	Response Control bit of USB Host transmitter to SETUP/OUT transaction 0: Expect to answer ACK or ready; 1: Expected no response, for real-time / synchronous transmission with non-endpoint 0 of the target device.	0

USB Host Transmit Length Register (UH_TX_LEN):

Bit	Name	Access	Description	Reset value
[7:0]	UH_TX_LEN	RW	Set the number of bytes of data that the sending endpoint of the USB host is ready to send	xxh

USB Host Endpoint Mode Control Register (UH_EP_MOD):

Bit	Name	Access	Description	Reset value
7	Reserved	RO	Reserved	0
6	bUH_EP_TX_EN	RW	0: Disable USB host to transmit data from endpoint; 1: Enable USB host to transmit data from endpoint (SETUP/OUT).	0
5	Reserved	RO	Reserved	0
4	bUH_EP_TBUF_MOD	RW	USB host transmit endpoint data buffer mode control bit	0
3	bUH_EP_RX_EN	RO	0: Disable USB host receiver endpoint to receive data (IN) 1: Enable USB host receiver endpoint to receive data (IN).	0
[2:1]	Reserved	RO	Reserved	00b
0	bUH_EP_RBUF_MOD	RW	USB host receives endpoint data buffer mode control bit	0

The data buffer mode of the USB host sending endpoint is controlled by the combination of bUH_EP_TX_EN and bUH_EP_TBUF_MOD, see the following table.

Table 16.4.2 Host send buffer mode

bUH_EP_TX_EN	bUH_EP_TBUF_MOD	Structure description: UH_TX_DMA as the starting address
0	x	Endpoint disabled, no UH_TX_DMA buffer used
1	0	Single 64-byte transmit buffer (SETUP/OUT)
1	1	Double 64-byte send buffer, selected by bUH_T_TOG: Select the first 64-byte buffer when bUH_T_TOG=0; Select the last 64-byte buffer when bUH_T_TOG=1.

The combination of bUH_EP_RX_EN and bUH_EP_RBUF_MOD controls the USB host to receive the endpoint data buffer mode, as shown in the following table.

Table 16.4.3 Host receive buffer mode

bUH_EP_RX_EN	bUH_EP_RBUF_MOD	Structure description: UH_RX_DMA as the starting address
0	x	Endpoint disabled, no UH_RX_DMA buffer used
1	0	Single 64-byte receive buffer (IN)
1	1	Double 64-byte send buffer, selected by bUH_R_TOG: Select the first 64-byte buffer when bUH_R_TOG=0; Select the last 64-byte buffer when bUH_R_TOG=1.

USB Host Receive Buffer Start Address (UH_RX_DMA):

Bit	Name	Access	Description	Reset value
[7:0]	UH_RX_DMA_H	RW	The USB host receives high bytes of the starting address of the buffer, which is valid only for the lower 3 bits and is fixed at 0 for the high 5 bits.	0xh
[7:0]	UH_RX_DMA_L	RW	USB host receives buffer starting address low byte	xxh

USB Host Transmit Buffer Start Address (UH_TX_DMA):

Bit	Name	Access	Description	Reset value
[7:0]	UH_TX_DMA_H	RW	The starting address of the USB host transmitting buffer is high bytes, valid only for the lower 3 bits, and fixed at 0 for the high 5 bits.	0xh
[7:0]	UH_TX_DMA_L	RW	USB host transmit buffer start address low byte	xxh

17. Parameters

17.1 Absolute Maximum Ratings

(Critical or exceeding the absolute maximum will likely cause the chip to operate improperly or even be damaged.)

Name	Parameter description		Min.	Max.	Unit
TA	Ambient temperature during operation	Fsys<40MHz	-40	85	℃
		For custom chips Fsys=48MHz	-20	70	℃
TAROM	Ambient temperature for Flash-ROM/EEPROM erase operations (recommended)		-20	85	℃

TS	Ambient temperature for storage	-55	125	℃
VDD	Supply voltage (VDD is connected to power, GND to ground)	-0.4	7.0	V
V33	Internal USB supply voltage	-0.4	VDD+0.4	V
VIO	Voltage on input/output pins	-0.4	VDD+0.4	V
VIOU	Voltage on UDP/UDM pin	-0.4	V33+0.4	V
VIOHV	Voltage on P5.5/HVOD pin	-0.4	13	V

17.2 Electrical Characteristics (5V)

(Test conditions: TA=25℃, VDD=5V, Fsys=12MHz)

Name	Parameter description		Min.	Typ.	Max.	Unit
VDD5	VDD supply voltage	V33 is only connected to an external capacitor	3.7	5	6.5	V
V33	Internal LDO output voltage (Automatically shorted to VDD during sleep)	TA=-15~65℃	3.23	3.3	3.37	V
		TA=-40~85℃	3.2	3.3	3.4	V
ICC24M5	Total supply current when Fsys=24MHz			4.4		mA
ICC12M5	Total supply current when Fsys=12MHz			3.0		mA
ICC750K5	Total supply current when Fsys=750KHz			1.6		mA
ISLP5	Total supply current after standby/normal sleep			1.1	1.5	mA
ISLP5L	Total supply current after power off/deep sleep bLDO_3V3_OFF=1, LDO disabled			4	20	uA
IADC5	ADC operating current			200	800	uA
ICMP5	CMP operating current			100	500	uA
ITKEY5	Touch-key capacitor charging current		35	50	70	uA
VIL5	Input low level voltage		0		1.2	V
VIH5	Input high level voltage		2.4		VDD	V
VOL5	Output low level voltage (I_{IL}=15mA)				0.4	V
VOH5	Output high level voltage (I_{OH}=6mA)		VDD-0.4			V
VOH5U	DP/UDM high level output voltage (I_{OH}=8mA)		V33-0.4			V
VHVOD	Voltage on P5.5/HVOD pin (not output / high impedance)		0		12.6	V
IIN	The input current without pull-up resistor		-5	0	5	uA
IDN5	The input current with pull-down resistor		-35	-70	-140	uA
IUP5	The input current with pull-up resistor		35	70	140	uA
IUP5X	The input current with pull-up resistor from low to high		250	400	600	uA
Rsw5	On-resistance of analogue switches for modules such as ADCs		500	700	1350	Ω
Vpot	Threshold voltage for power-on reset		2.3	4.0	4.6	V

17.3 Electrical Characteristics (3.3V)

(Test conditions: TA=25℃, VDD=V33=3.3V, Fsys=12MHz)

Name	Parameter description		Min.	Typ.	Max.	Unit
VDD3	VDD supply voltage	V33 is shorted to VDD, with USB enabled	3.0	3.3	3.6	V
		V33 is shorted to VDD, with USB disabled	2.7	3.3	3.6	V
ICC24M3	Total supply current when Fsys=24MHz			4.4		mA
ICC12M3	Total supply current when Fsys=12MHz			3.0		mA
ICC750K3	Total supply current when Fsys=750KHz			1.6		mA
ISLP3	Total supply current after standby/normal sleep			1.1	1.5	mA
ISLP3L	Total supply current after power off/deep sleep bLDO_3V3_OFF=1, LDO disabled			3	16	uA
IADC3	ADC operating current			180	700	uA
ICMP3	CMP operating current			70	300	uA
ITKEY3	Touch-key capacitor charging current		35	50	70	uA
VIL3	Input low level voltage		0		0.8	V
VIH3	Input high level voltage		1.9		VDD	V
VOL3	Output low level voltage (I_{IL}=10mA)				0.4	V
VOH3	Output high level voltage (I_{OH}=4mA)		VDD-0.4			V
VOH3U	DP/UDM high level output voltage (I_{OH}=8mA)		V33-0.4			V
VHVOD	Voltage on P5.5/HVOD pin (not output / high impedance)		0		12.6	V
IIN	The input current without pull-up resistor		-5	0	5	uA
IDN3	The input current with pull-down resistor		-15	-30	-60	uA
IUP3	The input current with pull-up resistor		15	30	60	uA
IUP3X	The input current with pull-up resistor from low to high		100	170	250	uA
Rsw3	On-resistance of analogue switches for modules such as ADCs		600	1000	2500	Ω
Vpot	Threshold voltage for power-on reset		2.3	2.7	3.0	V

17.4 Timing Parameters

(Test conditions: TA=25℃, VDD=5V or VDD=V33=3.3V, Fsys=12MHz)

Name	Parameter description		Min.	Typ.	Max.	Unit
Fxt	External crystal frequency or XI input clock frequency		6	24	24	MHz
Fosc	Internal clock frequency after calibration when VDD>=3V	TA=-15~65℃	23.52	24	24.48	MHz
		TA=-40~85℃	23.38	24	24.72	MHz
Fosc3	Internal clock frequency after calibration when VDD<3V		23.1	24	24.9	MHz
Fpll	PLL frequency after internal frequency doubling		24	96	96	MHz

Fusb4x	USB sampling clock frequency, with USB host function enabled	47.98	48	48.02	MHz
	USB sampling clock frequency, with USB device function enabled	47.04	48	48.96	MHz
Fsys	System clock frequency (VDD>=3V)	0.1	12	40	MHz
	System clock frequency (VDD<3V)	0.1	12	24	MHz
Tpor	Power on reset delay	8	11	15	mS
Trst	RST External input valid reset signal width	70			nS
Trdl	Thermal reset delay	20	30	50	uS
Twdc	Formula for calculating watchdog overflow period/timing period	131072 * (0x100 - WDOG_COUNT) / Fsys			
Tusp	Detect USB auto hang time in USB host mode	2	3	4	mS
	Detect USB auto hang time in USB device mode	4	5	6	mS
Twaksb	Time to wake up from standby/normal sleep	0.5	0.8	5	uS
Twakdp	Time to wake up from power down/deep sleep	120	200	1000	uS

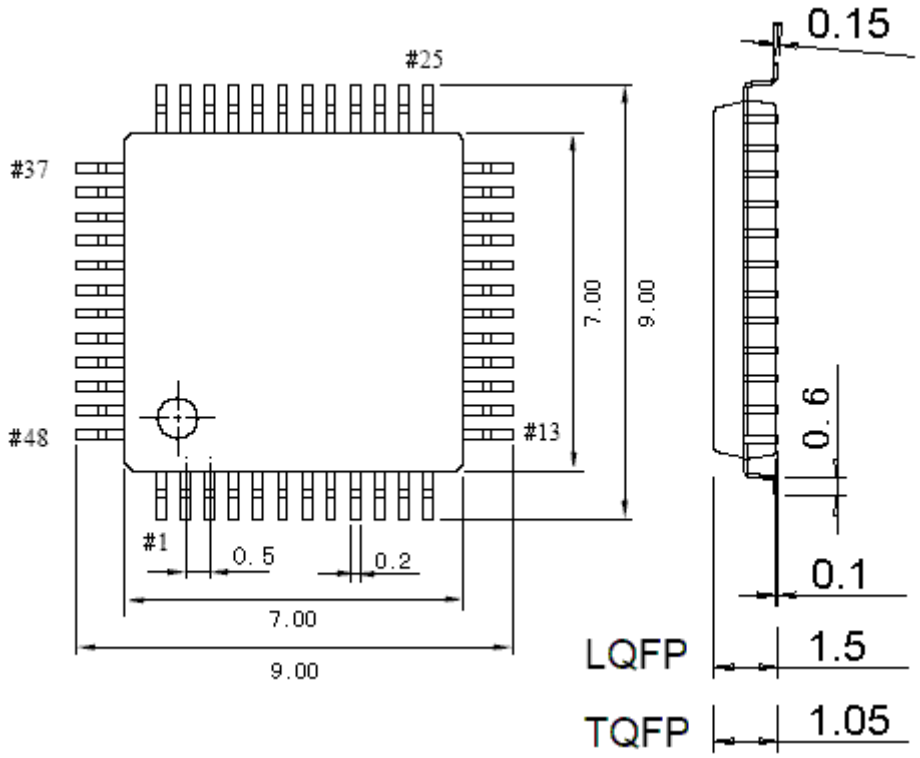
17.5 Other Parameters

(Test conditions: TA=25℃, VDD=4.5V~5.5V or VDD=V33=3.0V~3.6V)

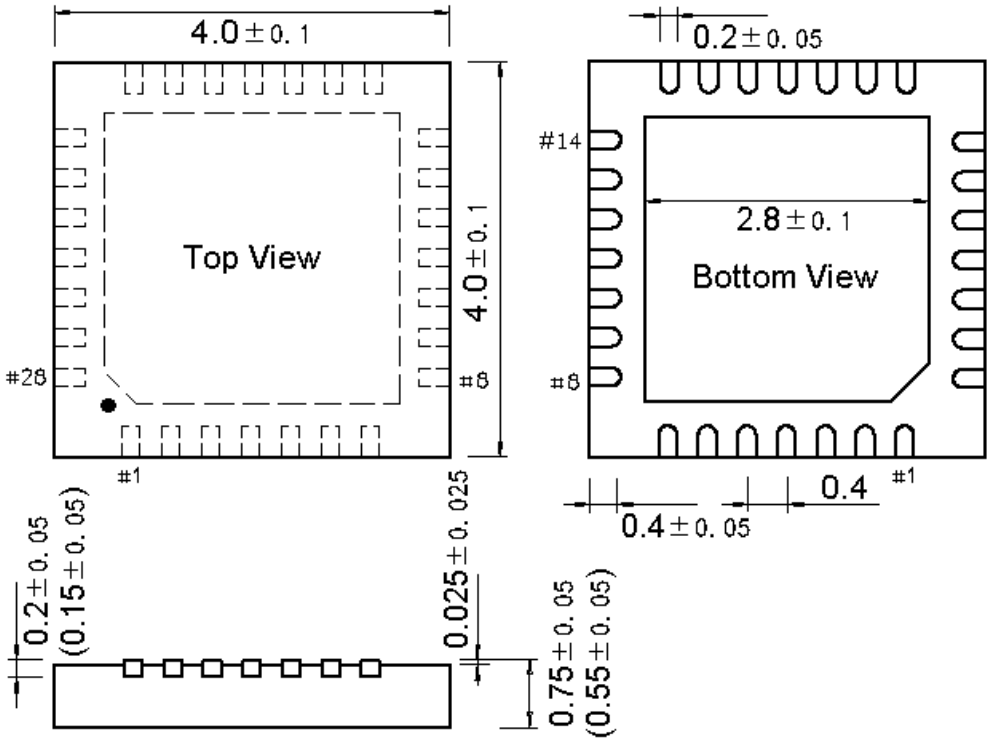
Name	Parameter description	Min.	Typ.	Max.	Unit
RTS	Measurement range of TS	-40		90	℃
ATSC	Measurement error of TS after software calibration		±9		℃
CTSV	Sensitivity of TS (voltage/temperature coefficient)	4	5	6	mV/℃
TERPG	Single erase/write operation time of Flash-ROM/EEPROM	2	5	8	mS
NEPCE	Erase/write cycle endurance of Flash-ROM/EEPROM	10K	Sampling value 100K		times
TDR	Data retention capability of Flash-ROM/EEPROM	10			years
VESD	ESD voltage tolerance on I/O input or output pins	4K	Sampling value 8K		V

18. Package Information

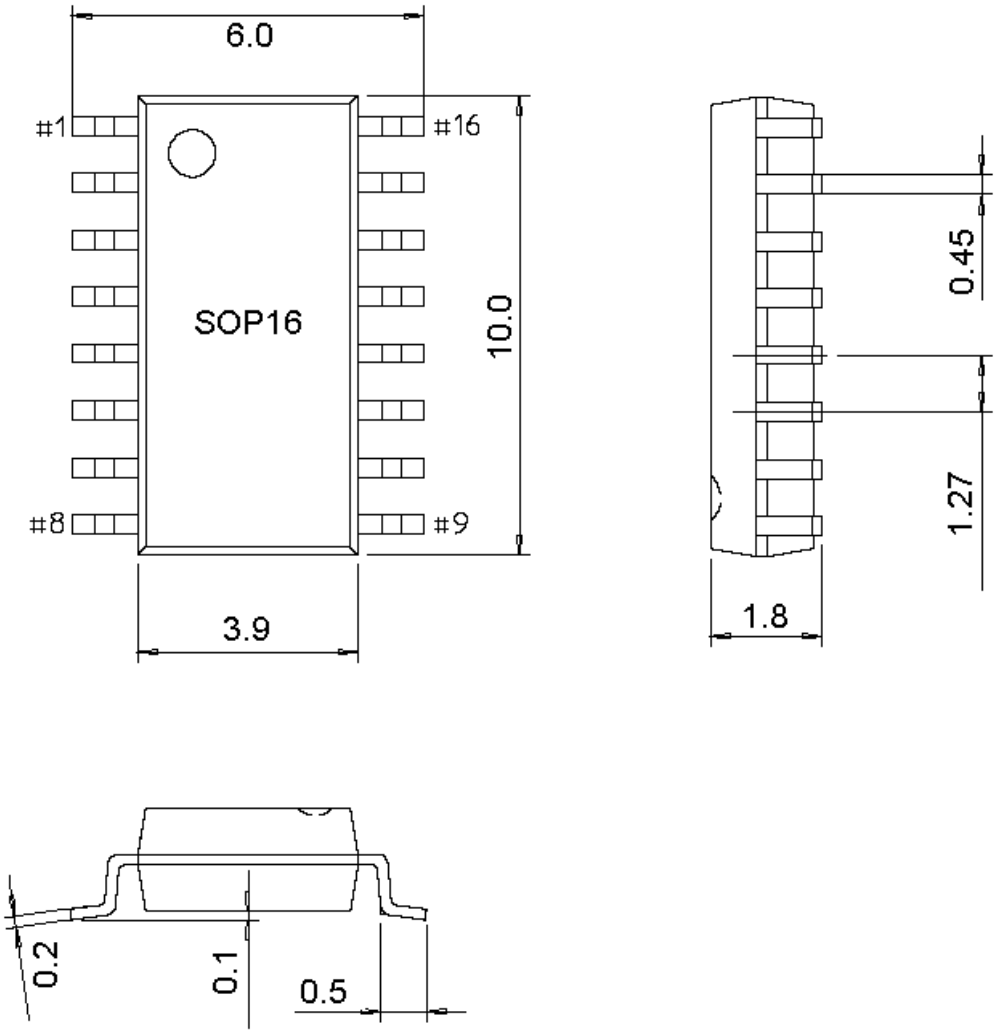
18.1 LQFP48-7*7



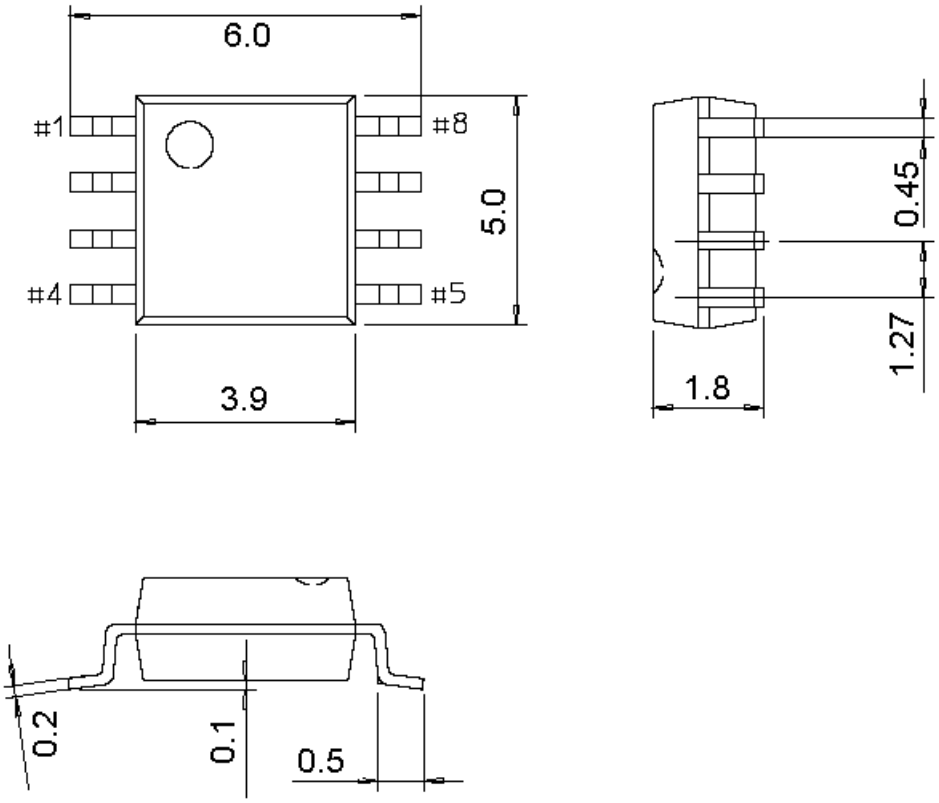
18.2 QFN28-4*4



18.3 SOP16-150mil



18.4 SOP8-150mil



19. Revision History

Version	Date	Description
V0.99	2017.09.27	First edition release
V1.0	2018.03.07	Official edition release
V1.1	2018.11.13	Modify A_INV description, delete routine file name, modify VDD3, add INTX
V1.2	2019.05.29	The register is renamed POWER_CFG. It is recommended to turn off the global interrupt during sleep, indicating that V33 will be automatically short to VDD during sleep, adding package size.
V1.3	2019.12.20	Modify clerical errors 15.4 (5), correcting clerical errors 16.4 UH_TX_DMA
V1.4	2020.06.26	Modify section 16.3, fine-tune some parameters of section 17.2 and section 17.3
V1.5	2020.11.12	Add CH548N package form
V1.6	2021.10.15	Limit the main frequency to no more than 48MHz, remind USB that there is no series resistance outside the pin.
V1.7	2022.01.28	Bit clear expression optimization: direct bit writing 0 clearing or register corresponding bit writing 1 clearing 0
V1.8	2023.05.26	Fine-tune the parameters such as 17-knot current, keep the 48MHz main frequency for new product design, and suggest that MASK_ULLDO_VOL should be adjusted during deep sleep under 3.3V power supply.