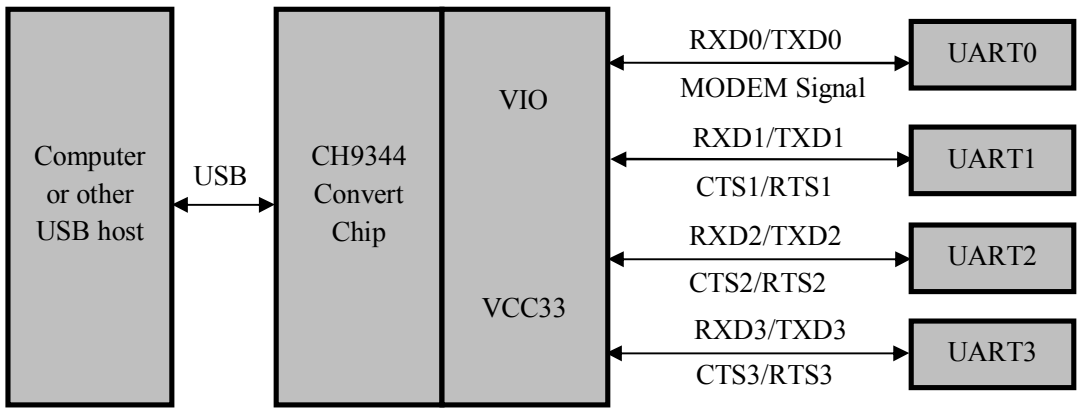
USB to Quad UARTs Chip CH9344

Datasheet
Version: V1C
http://wch.cn

1. Introduction

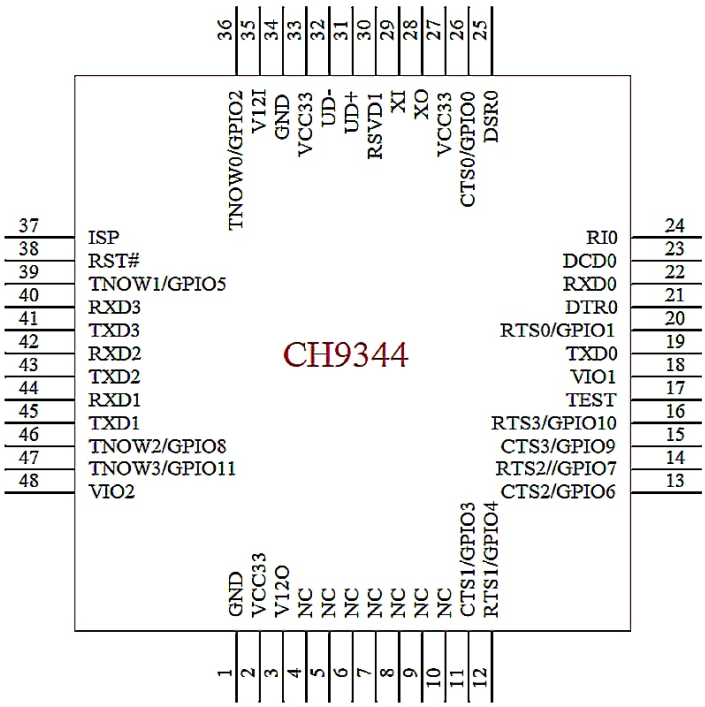
CH9344 is a USB to Quad UART Bridge Controller, which provides 4-channel full duplex UART interfaces UART0/1/2/3, to expand UART interface for computer or upgrade common serial devices to USB bus directly.



2. Features

- Operating voltage: 3.3V.
- High-speed USB 2.0 interface, peripheral components only need crystal and capacitor.
- Compatible with 16C550 UART with enhanced.
- Supports 5, 6, 7 or 8 data bits and 1 or 2 stop bits.
- Supports odd, even, none, blank0, mark1 and other parity.
- Supports RTS and CTS hardware automatic flow control.
- Supports half-duplex, supports RS485 switching in sending status, this function is enabled by default.
- Provides 12 GPIOs, which can be arbitrarily input and output.
- Supports programmable communication baud rate, supports 115200bps and up to 12Mbps communication baud rate.
- UART 0/1/2 and some I/Os are independently powered and support 3.3V, 2.5V or 1.8V power supply voltage. UART 3 supports 3.3V power supply.
- UART driver support: Windows XP/Vista/Win7/Win8/Win10/Win11/Win Server/Linux, etc.
- Provides LQFP-48 lead-free package, compatible with RoHS.

3. Packages



Package	Width Of Plastic	Pitch Of Pin		Instruction Of Package	Ordering Information
LQFP-48	7×7 mm	0.5mm	19.7mil	Standard LQFP48-pin patch	CH9344L

4. Pin Out

Pin No.	Pin Name	Pin Type	Pin Description
1, 34	GND	POWER	Ground: public ground, 0V reference point.
2, 27, 33	VCC33	POWER	Input 3.3V power supply voltage, requires an external 0.1uF capacitor.
18	VIO1	POWER	I/O power supply voltage input, requires an external decoupling capacitor, supply I/O power for 11-26 pins.
48	VIO2	POWER	I/O power supply voltage input, requires an external decoupling capacitor. supply I/O power for 42-48 pins.
3	V12O	POWER	Core power supply 1.2V output, requires an external 3.3uF capacitor.
35	V12I	POWER	Core power supply 1.2V input, requires an external 0.1uF capacitor.
11	CTS1/GPIO3	IN/OUT	MODEM input signal of UART1, clear to send. General GPIO3, used for IO input and output.
12	RTS1/GPIO4	IN/OUT	MODEM output signal of UART1, request to send. General GPIO4, used for IO input and output.
13	CTS2/GPIO6	IN/OUT	MODEM input signal of UART2, clear to send. General GPIO6, used for IO input and output.
14	RTS2/GPIO7	IN/OUT	MODEM output signal of UART2, request to send. General GPIO7, used or IO input and output.
15	CTS3/GPIO9	IN/OUT	MODEM input signal of UART3, clear to send. General GPIO9, used for IO input and output.

16	RTS3/GPIO10	IN/OUT	MODEM output signal of UART3, request to send. General GPIO10, used for IO input and output.
17	TEST	OUT	Test pin, default to be suspended.
19	TXD0	OUT	Serial data output of UART0.
20	RTS0/GPIO1	IN/OUT	MODEM output signal of UART0, request to send. General GPIO1, used for IO input and output.
21	DTR0	OUT	MODEM output signal of UART0, data terminal ready.
22	RXD0	IN	Serial data input of UART0.
23	DCD0	IN	MODEM input signal of UART0, data carrier detect.
24	RI0	IN	MODEM input signal of UART0, ring indicator.
25	DSR0	IN	MODEM input signal of UART0, data set ready.
26	CTS0/GPIO0	IN/OUT	MODEM input signal of UART0, clear to send. General GPIO0, used for IO input and output
28	XO	OUT	Reverse output of crystal oscillator.
29	XI	IN	Input of crystal oscillator.
30	RSVD1	IN	Reserved, requires a 12KΩ resistor to GND and a 20pF capacitor in parallel.
31	UD+	USB signal	Connect to USB D+ Signal directly.
32	UD-	USB signal	Connect to USB D- Signal directly.
36	TNOW0/GPIO2	IN/OUT	485 transmit and receive enable pin of UART0. General GPIO2, used for IO input and output.
37	ISP	IN	Firmware upgrade configuration pin, active low, built-in pull-up resistor.
38	RST#	IN	External reset input pin, active low, built-in pull-up resistor.
39	TNOW1/GPIO5	IN/OUT	485 transmit and receive enable pin of UART1. General GPIO5, used for IO input and output.
40	RXD3	IN	Serial data input of UART3.
41	TXD3	OUT	Serial data output of UART3.
42	RXD2	IN	Serial data input of UART2.
43	TXD2	OUT	Serial output of UART2.
44	RXD1	IN	Serial data input of UART1.
45	TXD1	OUT	Serial data output of UART1.
46	TNOW2/GPIO8	IN/OUT	485 transmit and receive enable pin of UART2. General GPIO8,used for IO input and output.
47	TNOW3/GPIO11	IN/OUT	485 transmit and receive enable pin of UART3. General GPIO11, used for IO input and output.
4, 5, 6, 7, 8, 9, 10	NC	NONE	No connection, must be suspended.

Note: The MODEM signal pin and TNOW signal pin function are enabled by default when the chip is powered on. Turn off the GPIO pin function.

4.1 VIO Description

In order to be compatible with the power system of external devices, CH9344 provides two sets of power pins. The specific distribution is as follows:

Name	Range Of Power	Pin No. Power Supply Output
VIO1	Supports 1.8V/2.5V/3.3V independent power supply	11-26
VIO2	Supports 1.8V/2.5V/3.3V independent power supply	42-48

5. Function Description

5.1 General Description

CH9344 has an integrated power-on reset circuit. When chip is working normally, an external 30MHz clock signal is required to provide to the XI pin.

The clock signal is generated by the built-in inverter of CH9344 through crystal frequency stabilization oscillation. The peripheral circuit needs to place a 30MHz crystal between the XI and XO pins, and connect the XI and XO pins to the ground connect with a 20pF oscillation capacitor.

CH9344 has integrated all peripheral circuits required for USB bus, including embedded USB2.0 controller and USB-PHY, series matching resistance of USB signal line, 1.5K pull-up resistor required for Device, etc. The UD+ and UD- pins can be directly connected to PC or other USB host. If a fuse resistor or inductor or ESD protection device is connected in series for chip safety, the AC and DC equivalent series resistance should be within 5Ω. CH9344 and USB products can directly use the 3.3V power supply which is outputted by VBUS on the USB bus after LDO stabilization. If the USB products supply standing power in another manner, CH9344 should also use the standing power supply, to avoid the I/O current backflow between the chip and USB power supply.

5.2 UART Description

CH9344 provides 4 sets of full-duplex UART interfaces UART0/1/2/3. UART0 supports MODEM signals: RTS, DTR, DCD, RI, DSR, CTS. UART1/2/3 support MODEM signal: RTS, CTS.

Serial data includes 1 low-level start bit, 5, 6, 7 or 8 data bits, 1 or 2 high-level stop bits, and supports odd/even/mark/blank parity. The UART interface supports common communication baud rates: 1200, 2400, 4800, 9600, 19.2K, 38.4K, 57.6K, 115.2K, 230.4K, 250K, 460.8K, 500K, 921.6K, 1M, 2M, 3M, 4M, 6M, 12M etc. The baud rate error of the UART interface sending a signal is less than 0.2%, and the allowable baud rate error of the UART interface receiving signal is not more than 2%.

CH9344 supports the 485 signal automatic receiving and sending enable pin, and this function is enabled by default. The corresponding pins of UART0/1/2/3 are TNOW0, TNOW1, TNOW2 and TNOW3.

CH9344 supports 12 general GPIO pins, which can be used as input and output. The pins are multiplexed with the MODEM signal pins of UART0/1/2/3 and the TNOW pins.

6. Parameters

6.1 Absolute Maximum Ratings

(Critical state or exceeding maximum can cause chip to not work or even be damaged)

Name	Parameter Description		Min.	Max.	Unit
TA	Operating ambient temperature	VCC33=3.3V	-40	85	℃
TS	Storage ambient temperature		-55	125	℃
VCC33	Supply voltage (VCC33 connects to power, GND to ground)		-0.4	4.2	V
VIO	UART I/O supply voltage (VIO1 and VIO2 connect to power, GND to ground)		-0.4	4.2	V
VUART	Voltage of serial and other pins		-0.4	VIO+0.4	V
VESD	HBM ESD withstand voltage of USB or I/O Pin		2		KV

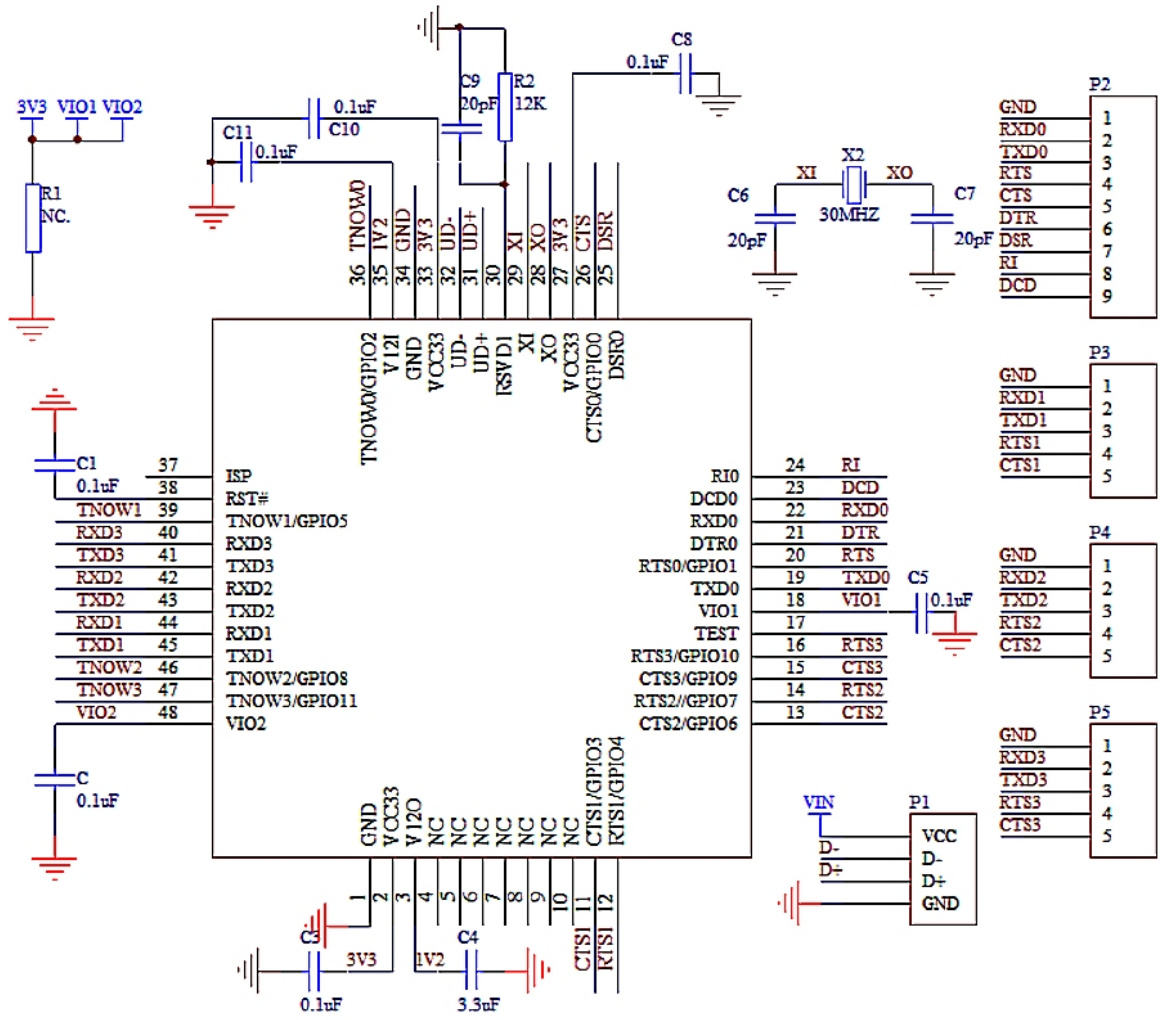
6.2 Electrical Parameters

(Test Conditions: TA=25℃, VCC33=VIO1=VIO2=3.3V)

Name	Parameter Description	Min.	Typ.	Max.	Unit
VCC33	Supply voltage	3.0	3.3	3.6	V
VIO	UART I/O supply voltage (VIO1 and VIO2)	1.7	3.3	3.6	V
ICC	Operating supply current	30	55	70	mA
ISLP	Operating supply current (USB suspended)	500	770	1000	uA
VIL	Input low voltage (VCC33=VIO1=VIO2=3.3V)	-0.4	-	0.7	V
VIH	Input high voltage (VCC33=VIO1=VIO2=3.3V)	2.0	-	VIO+0.4	V
VOL	Output low voltage (6mA draw current)	-	-	0.4	V
VOH	Output high voltage (5mA output current)	VIO-0.4	-	-	V
IUP	Input current of input with built-in pull-up resistor	25	45	80	uA
IDN	Input current of input with built-in pull-down resistor	-25	-45	-80	uA

7. Application

7.1 USB to Quad-TTL UART Interfaces



In the image above, the CH9344 realizes the USB to quad-TTL UART interfaces. UART0 supports the 9-wire MODEM signal. UART 1-3 only support RTS and CTS signals to achieve flow control.

P1 is the USB port. The USB bus includes a pair of 5V power lines and a pair of data signal lines. Usually, the +5V power line is red, the ground line is black, the D+ signal line is green and the D- signal line is white. The power supply current provided by the USB bus can reach 500mA, and the VBUS pin detects the USB power supply status here.

The power supply scheme is that the VCC33 pin connects to a 3.3V power supply. Each VCC33 pin is close to and connected with a 0.1μF decoupling capacitor. The V12O pin is connected with an external 3.3μF capacitor and to the V12I pin. V12I pin is connected with an external 0.1μF decoupling capacitor. VIO1 provides peripheral pin power for pins 11-26. VIO2 provides peripheral pin power for pins 42-48. VIO1 and VIO2 support 3.3V, 2.5V, and 1.8V power supply voltage, and the pins need to be connected with an external 0.1μF capacitor.

RSVD1 pin needs to connect with a 12K resistor to ground, and the pin also needs to connect with a 20pF capacitor in parallel to ground.

The main purpose of resistor R1 is to prevent the UART device connected to CH9344 sinks current to CH9344 through the signal pin, causing it to work abnormally. A 100Ω resistor can be connected in parallel between VCC33 and GND, and the specific resistance value needs to be adjusted according to the drive capability of the external UART interface pin.

Crystal X1, capacitors C6 and C7 are used in the clock oscillation circuit of CH9344. The frequency of X1 is 30MHz±0.4‰. C6 and C7 are monolithic or high-frequency ceramic capacitors with a capacity of about 20pF.

P2-P5 is the output of quad-TTL UART interfaces, which can be connected with external MAX3245/SP3243 to realize the conversion of TTL to RS232 signal.

When designing the PCB, pay attention to: the decoupling capacitor should be as close as possible to the connected pins of CH9344, including VCC33, VIO1, VIO2, V12O and V12I power input and output pins. The USB D+ and D-signal lines are close to parallel wiring, and providing ground wire or copper on both sides to reduce signal interference from the outside.