Differential 2-Channel 2:1, Quad-Pole Double-Throw Super-Speed Analog Switch, CH482D/X

Differential 3-Channel 2:1, 6-Pole Double-Throw Super-Speed Analog Switch, CH483M/X

Differential 2-Channel 4:1, Quad-Pole Quad-Throw Super-Speed Analog Switch, CH484M

Differential 2-Channel switch, Quad-Pole Double-Throw Super-Speed Analog Switch, CH481D

Differential 2-Channel 4:1, Quad-Pole Quad-Throw High-Speed Analog Switch, CH486F

Datasheet
Version: 1C
http://wch.cn

1. Overview

CH482D, CH483M, CH483X, CH484M, CH481D and CH486F are differential high speed signal bidirectional analog switches based on RF technology with high bandwidth and low ON resistance.

CH482D includes 2 channels of differential super-speed signal 2:1 analog switch, QPDT, which can be used for 1 of 2 switch of the USB 3.0 Super Speed, PCIe Gen1/2, SATA/SAS 1.5G/3G/6G, Display Port and other 2-channel differential signals.

The functions of CH482X are similar to functions of CH482D with higher bandwidth, which can be used for 1 of 2 switch of USB 3.1 Gen2 (Super Speed+), PCIe Gen1/2/3, SATA/SAS 3G/6G, Display Port and other 2-channel differential signals.

CH484M includes 2 channels of differential super-speed signal 4:1 analog switch, QPQT, which can be used for one-of-four switch of the USB 3.0 Super Speed, PCIe Gen1/2, SATA/SAS 1.5G/3G, Display Port and other 2-channel differential signals.

CH481D includes 2 channels of differential super-speed signal matrix exchange analog switch, which can be used for pass-through or crossover of the USB 3.0 Super Speed, PCIe Gen1/2, SATA/SAS 1.5G/3G/6G, Display Port and other 2-channel differential signals. For information about matrix switches or medium/low-frequency signal cross switches with more channels, please refer to CH449 datasheet.

CH486F includes 2 channels of differential high-speed signal 4:1 analog switch, QPQT, which can be used for one-of-four switch of the USB 2.0 High Speed, SATA/SAS 1.5G and other 2-channel differential signals. For DPOT 8-channel multiplexer (8:1 MUX), please refer to CH448.

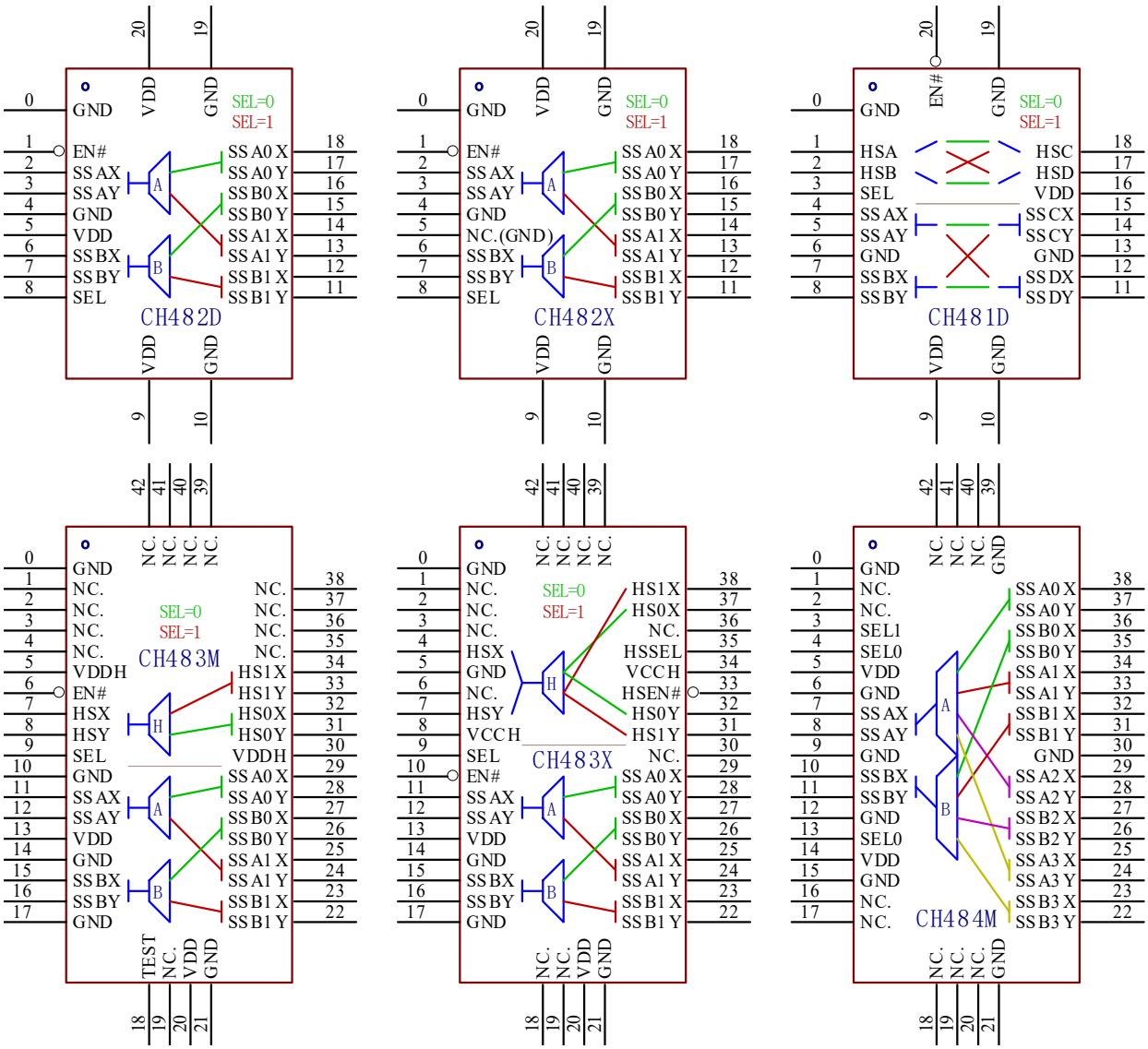
CH483M and CH483X include all modules of CH482D (SS super speed channel for short), and also include the 1-channel differential high speed signal 2:1 analog switch (HS high speed channel for short), QPDT+DPDT, which can be used for 1 of 2 switch of USB 3.0 Super Speed & USB 2.0 High Speed, PCIe Gen1/2 & Refclk, Display Port and other 3-channel differential signals.

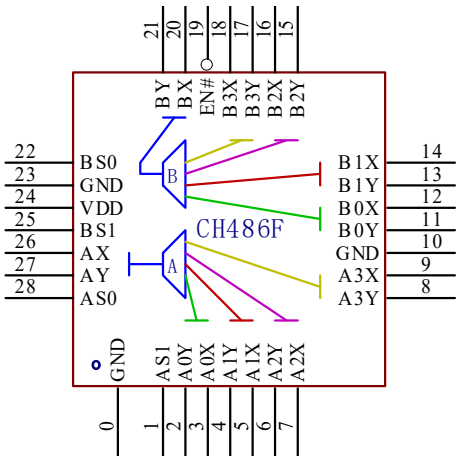
2. Features

- High bandwidth, SS super speed channel supports 6Gbps differential signal, and super speed USB signal.

- CH482X super speed channel supports 10Gbps differential signal, and USB 3.2 Gen2 signal.
- HS high speed channel supports 1.5G (4:1) or 2.5Gbps (2:1) differential signal, and full-amplitude voltage analog signal.
- HS high speed channel supports video signal, low speed, full speed and high speed USB signal.
- Low ON resistance. The typical value of Ron is about 4Ω.
- Low crosstalk, high isolation degree.
- Provide a global enable pin, and the multi-channel analog switch realizes unified enable and unified switching.
- SS super speed channel ESD supports 2KV HBM, other channels and control pins ESD support 4KV HBM.
- Rated 3.3V supply voltage, low static power dissipation.
- Provide QFN20-2.5X4.5, QFN42-3.5X9, QFN28 and other packages, compatible with RoHS.

3. Package





Package	Body size	Lead pitch		Description	Part No.
QFN20-2.5X4.5	2.5*4.5mm	0.50mm	19.7mil	Quad (Rectangular) no-lead 20-pin	CH482D
QFN20-2.5X4.5	2.5*4.5mm	0.50mm	19.7mil	Quad (Rectangular) no-lead 20-pin	CH482X
QFN42-3.5X9	3.5*9mm	0.50mm	19.7mil	Quad (Rectangular) no-lead 42-pin	CH483M
QFN42-3.5X9	3.5*9mm	0.50mm	19.7mil	Quad (Rectangular) no-lead 42-pin	CH483X
QFN42X-3.5X9	3.5*9mm	0.50mm	19.7mil	Quad (Rectangular) no-lead 42-pin	CH484M
QFN20-2.5X4.5	2.5*4.5mm	0.50mm	19.7mil	Quad (Rectangular) no-lead 20-pin	CH481D
QFN28	4*4mm	0.40mm	15.7mil	Quad no-lead 28-pin	CH486F

Note: For devices in QFN package, the EPAD is marked as Pin 0#, which is unnecessary but recommended to connect.

CH483X can only be used for compatible applications, and needs to be reserved. For new designs, please select CH483M or CH482D preferentially.

4. Pin definitions

4.1. CH482D and CH482X

Pin No.	Pin Name	Pin Type	Description
9, 20	VDD	Power	Positive power, 3.3V rated voltage, need to be connected with an external decoupling capacitor
4, 10, 19, 0	GND	Power	Ground, digital signal reference ground
5	VDD	Power	CH482D: Optional positive power, 3.3V rated voltage
	NC.	NC.	CH482X: No electric signal connection, it is recommended to connect to GND or VDD
1	EN#	Digital input	Global enable input, active low. Disconnected and power off when at high level
8	SEL	Digital input	2:1 analog switch selection input: High level: select 1# terminal (SS*1*);

			Low level: select 0# terminal (SS*0*)
2, 3, 6, 7	SSAX, SSAY, SSBX, SSBY	Analog signal	Common terminal of one-of-two analog switch
18, 17, 16, 15	SSA0X, SSA0Y, SSB0X, SSB0Y	Analog signal	Analog switch 0#, selected when SEL pin inputs low level
14, 13, 12, 11	SSA1X, SSA1Y, SSB1X, SSB1Y	Analog signal	Analog switch 1#, selected when SEL pin inputs high level

4.2. CH483M and CH483X

CH483M Pin No.	CH483X Pin No.	Pin Name	Pin Type	Description
13, 20	13, 20	VDD	Power	SS positive power, 3.3V rated voltage
	30	NC.	NC.	No electric signal connection, it is recommended to connect to GND or VDD
30, 5		VDDH	Power	HS positive power, 3.3V rated voltage
	8, 34	VCCH	Power	HS positive power, 5V rated voltage
10, 14, 17, 21, 0	5, 14, 17, 21, 0	GND	Power	Ground, digital signal reference ground
18	None	TEST	Analog signal	Reserved. If SS works at 2.5V, it is recommended to be shorted to VDD to improve performance.
6		EN#	Digital input @VDD domain	Global enable input, active low. Disconnected and power off when at high level.
	10	EN#	Digital input @VDD domain	SS global enable input, active low. Disconnected and power off when at high level.
	33	HSEN#	Digital input @VCCH domain	HS global enable input, active low.
9		SEL	Digital input @VDD domain	Global one-of-two analog switch input selection: High level: select 1# terminal (*S*1*); Low level: select 0# terminal (*S*0*)
	9	SEL	Digital input @VDD domain	SS one-of-two analog switch input selection: High level: select 1# terminal (SS*1*); Low level: select 0# terminal (SS*0*)
	35	HSSEL	Digital input @VCCH domain	HS one-of-two analog switch input selection: High level: select 1# terminal (HS1*); Low level: select 0# terminal (HS0*)
11, 12, 15, 16	11, 12, 15, 16	SSAX, SSAY, SSBX, SSBY	Analog signal	SS common terminal of one-of-two analog switch
29, 28, 27, 26	29, 28, 27, 26	SSA0X, SSA0Y, SSB0X, SSB0Y	Analog signal	SS analog switch 0# selected when SEL pin inputs low level

25, 24, 23, 22	25, 24, 23, 22	SSA1X, SSA1Y, SSB1X, SSB1Y	Analog signal	SS analog switch 1# selected when SEL pin inputs high level
7, 8	4, 7	HSX, HSY	Analog signal	HS common terminal of one-of-two analog switch
32, 31	37, 32	HS0X, HS0Y	Analog signal	HS analog switch 0# selected when HSSEL pin inputs low level
34, 33	38, 31	HS1X, HS1Y	Analog signal	HS analog switch1# selected when HSSEL pin inputs high level
1, 2, 3, 4, 19, 35, 36, 37, 38, 39, 40, 41, 42	1, 2, 3, 6, 18, 19, 36, 39, 40, 41, 42	NC.	NC.	No electric signal connection, it is recommended to be suspended

4.3. CH484M

Pin No.	Pin Name	Pin Type	Description
5, 14	VDD	Power	Positive power supply, 3.3V rated voltage, needs to be connected with an external decoupling capacitor
6, 9, 12, 15, 21, 30, 39, 0	GND	Power	Ground, digital signal reference ground
3	SEL1	Digital input	One-of-four analog switch selection input SEL1/0: 00: Select 0# (SS*0*). 01: Select 1# (SS*1*). 10: Select 2# (SS*2*). 11: Select 3# (SS*3*). Pin 4 and Pin 13 need to be used as SEL0 together after being shorted.
4, 13	SEL0		
7, 8, 10, 11	SSAX, SSAY, SSBX, SSBY	Analog signal	Common terminal of one-of-four analog switch
38, 37, 36, 35	SSA0X, SSA0Y, SSB0X, SSB0Y	Analog signal	Analog switch 0#, selected when SEL1/0 pin inputs 00
34, 33, 32, 31	SSA1X, SSA1Y, SSB1X, SSB1Y	Analog signal	Analog switch 1#, selected when SEL1/0 pin inputs 01
29, 28, 27, 26	SSA2X, SSA2Y, SSB2X, SSB2Y	Analog signal	Analog switch 2#, selected when SEL1/0 pin inputs 10
25, 24, 23, 22	SSA3X, SSA3Y, SSB3X, SSB3Y	Analog signal	Analog switch 3#, selected when SEL1/0 pin inputs 11
1, 2, 16, 17, 18, 19, 20, 40, 41, 42	NC.	NC.	No electric signal connection, it is recommended to be suspended

4.4. CH481D

Pin No.	Pin Name	Pin Type	Description
9, 16	VDD	Power	Positive power supply, 3.3V rated voltage, need to be connected with an external decoupling capacitor
6, 10, 13, 19, 0	GND	Power	Ground, digital signal reference ground

20	EN#	Digital input	Global enable input, active low. Disconnected and power off when at high level.
3	SEL	Digital input	Mode input of matrix analog switch: Low level: select pass-through mode (A is connected to C, B is connected to D). High level: select exchange mode (A is connected to D, B is connected to C).
4, 5	SSAX, SSAY	Analog signal	Port A of SS
7, 8	SSBX, SSBY	Analog signal	Port B of SS
15, 14	SSCX, SSCY	Analog signal	Port C of SS
12, 11	SSDX, SSDY	Analog signal	Port D of SS
1	HSA	Analog signal	Port A of HS
2	HSB	Analog signal	Port B of HS
18	HSC	Analog signal	Port C of HS
17	HSD	Analog signal	Port D of HS

4.5. CH486F

Pin No.	Pin Name	Pin Type	Pin description
24	VDD	Power	Positive power supply, 3.3V rated voltage, needs to be connected with an external decoupling capacitor
10, 23, 0	GND	Power	Ground, digital signal reference ground
19	EN#	Digital input	Global enable input, active low.
1, 28	AS1, AS0	Digital input	Channel A one-of-four analog switch selection input: 00: Select 0# (A0*). 01: Select 1# (A1*). 10: Select 2# (A2*). 11: Select 3# (A3*).
26, 27	AX, AY	Analog signal	Common terminal of channel A one-of-four analog switch
3, 2	A0X, A0Y	Analog signal	Analog switch 0#, selected when AS1/0 pin inputs 00
5, 4	A1X, A1Y	Analog signal	Analog switch 1#, selected when AS1/0 pin inputs 01
7, 6	A2X, A2Y	Analog signal	Analog switch 2#, selected when AS1/0 pin inputs 10
9, 8	A3X, A3Y	Analog signal	Analog switch 3#, selected when AS1/0 pin inputs 11
25, 22	BS1, BS0	Digital input	Channel B one-of-four analog switch selection input: 00: Select 0# (B0*). 01: Select 1# (B1*). 10: Select 2# (B2*). 11: Select 3# (B3*).
20, 21	BX, BY	Analog signal	Common terminal of channel B one-of-four analog switch
12, 11	B0X, B0Y	Analog signal	Analog switch 0#, selected when BS1/0 pin inputs 00

14, 13	B1X, B1Y	Analog signal	Analog switch 1#, selected when BS1/0 pin inputs 01
16, 15	B2X, B2Y	Analog signal	Analog switch 2#, selected when BS1/0 pin inputs 10
18, 17	B3X, B3Y	Analog signal	Analog switch 3#, selected when BS1/0 pin inputs 11

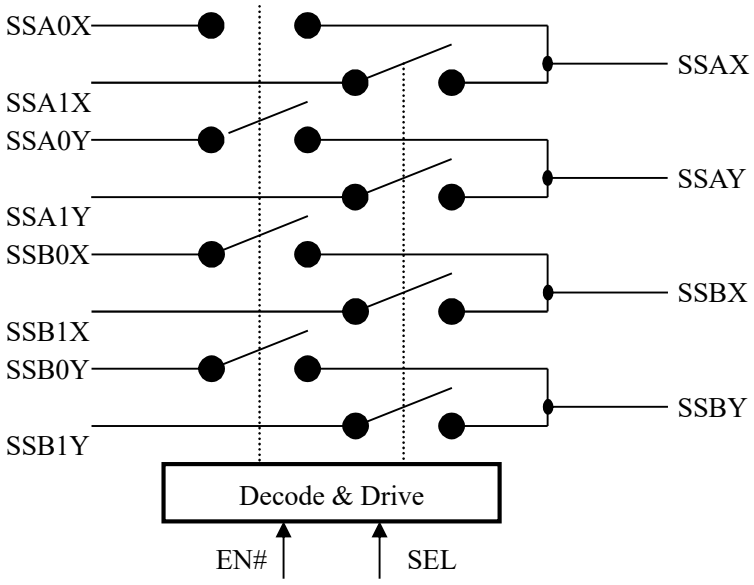
5. Functional specification

5.1. CH482D and CH482X

CH482D is a QPDT broadband super speed bidirectional analog switch, which contains 2 differential channels of 2:1 MUX analog switch (4 channels 2:1 in total), which can be used for one-of-two switch of differential signals not more than 1.7V voltage and 6Gbps.

CH482X is a QPDT broadband super speed bidirectional analog switch, which contains 2 differential channels of 2:1 MUX analog switch (4 channels 2:1 in total), which can be used for one-of-two switch of differential signals not more than 1.7V voltage and 10Gbps. It supports USB 3.1/3.2 Gen2.

SSAX and SSAY constitute the super speed differential channel SSA. SSBX and SSBY constitute the super speed differential channel SSB. The differential signals X and Y can be set to +/- (p/n) or the vice versa according to PCB design optimization requirements. Channel SSA and SSB can be set to TX/RX or vice versa according to PCB design optimization requirements.



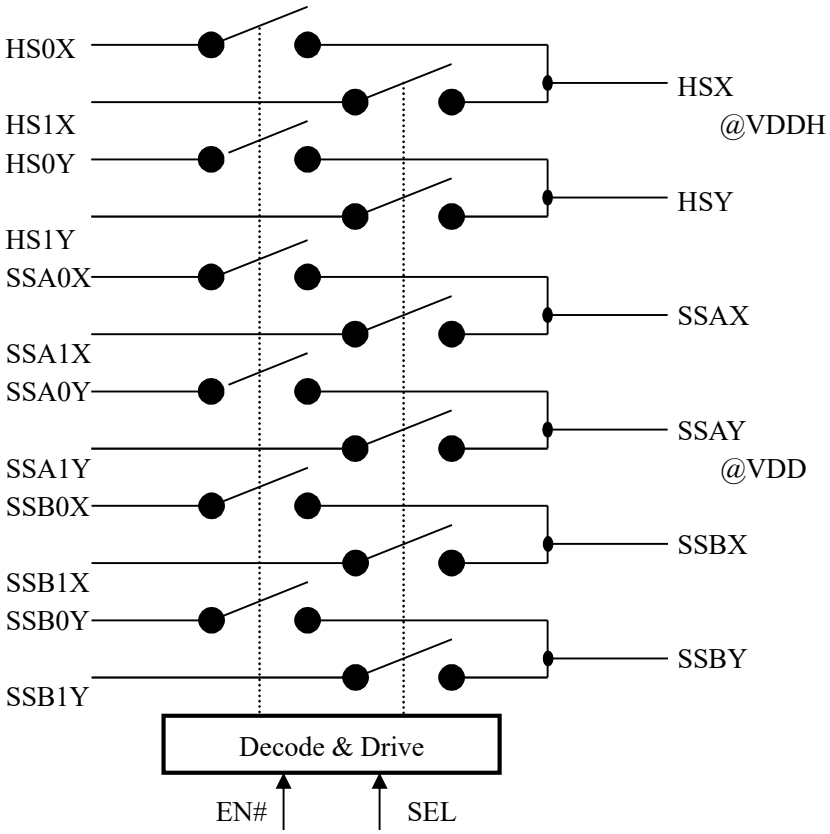
CH482D/X is uniformly enabled by the control of EN# pin, and uniformly switched by SEL pin select. The following table is its control table.

EN#	SEL	SSAX	SSAY	SSBX	SSBY
0	0	Select SSA0X	Select SSA0Y	Select SSB0X	Select SSB0Y
0	1	Select SSA1X	Select SSA1Y	Select SSB1X	Select SSB1Y
1	X	All off	All off	All off	All off

5.2. CH483M

CH483M is a QPDT broadband super speed bidirectional + DPDT broadband high speed bidirectional analog switch chip, which contains 3 differential channels 2:1 MUX analog switch (one-of-two 6 channels in total), which can be used for one-of-two switch of "USB super speed + USB high speed" and other differential signals.

HSX and HSY constitute high speed differential channel HS, supporting VDDH voltage full amplitude and 2.5Gbps signal. SS is the same as that of CH482D.



CH483M is uniformly enabled by the control of EN# pin, and uniformly switched by SEL pin select. The following table is its control table.

EN#	SEL	SSAX	SSAY	SSBX	SSBY	HSX	HSY
0	0	Select SSA0X	Select SSA0Y	Select SSB0X	Select SSB0Y	Select HS0X	Select HS0Y
0	1	Select SSA1X	Select SSA1Y	Select SSB1X	Select SSB1Y	Select HS1X	Select HS1Y
1	X	All off	All off	All off	All off	All off	All off

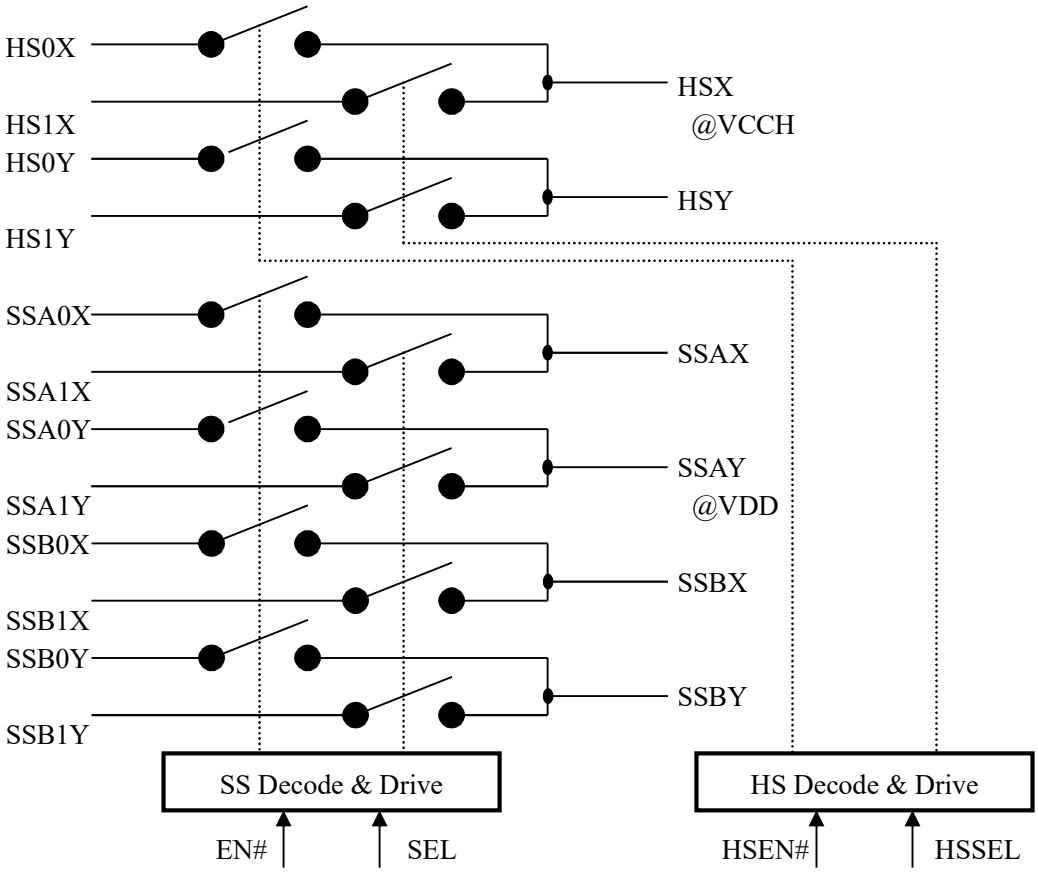
If CH483M SS is required to support 2.5V supply voltage, its TEST pins can be shorted to VDD.

5.3. CH483X

CH483X is a QPDT broadband super speed bidirectional + DPDT broadband high speed bidirectional analog switch, which contains 3 differential channels of 2:1 MUX analog switch (6 channels 2:1 in total), which can be used for one-of-two switch of "USB super speed + USB high speed" and other differential signals.

HSX and HSY constitute high speed differential channel HS, supporting VCCH voltage full amplitude and 500Mbps signal. SS is the same as CH482D.

Compared with CH483M, CH483X has two main differences: first, the HS and SS are completely independent, and each uses the independent control signals. Second, the power supply VCCH of HS channel is rated at 5V. In this case, HS channel supports 5V full-amplitude signal and the control signal supports 5V or 3.3V.



SS of CH483X is enabled by the control of EN# pin, and switched by SEL pin select. The following table is its control table.

EN#	SEL	SSAX	SSAY	SSBX	SSBY
0	0	Select SSA0X	Select SSA0Y	Select SSB0X	Select SSB0Y
0	1	Select SSA1X	Select SSA1Y	Select SSB1X	Select SSB1Y
1	X	All off	All off	All off	All off

HS of CH483X is enabled by the control of HSEN# pin, and switched by HSSEL pin select. The following table is its control table.

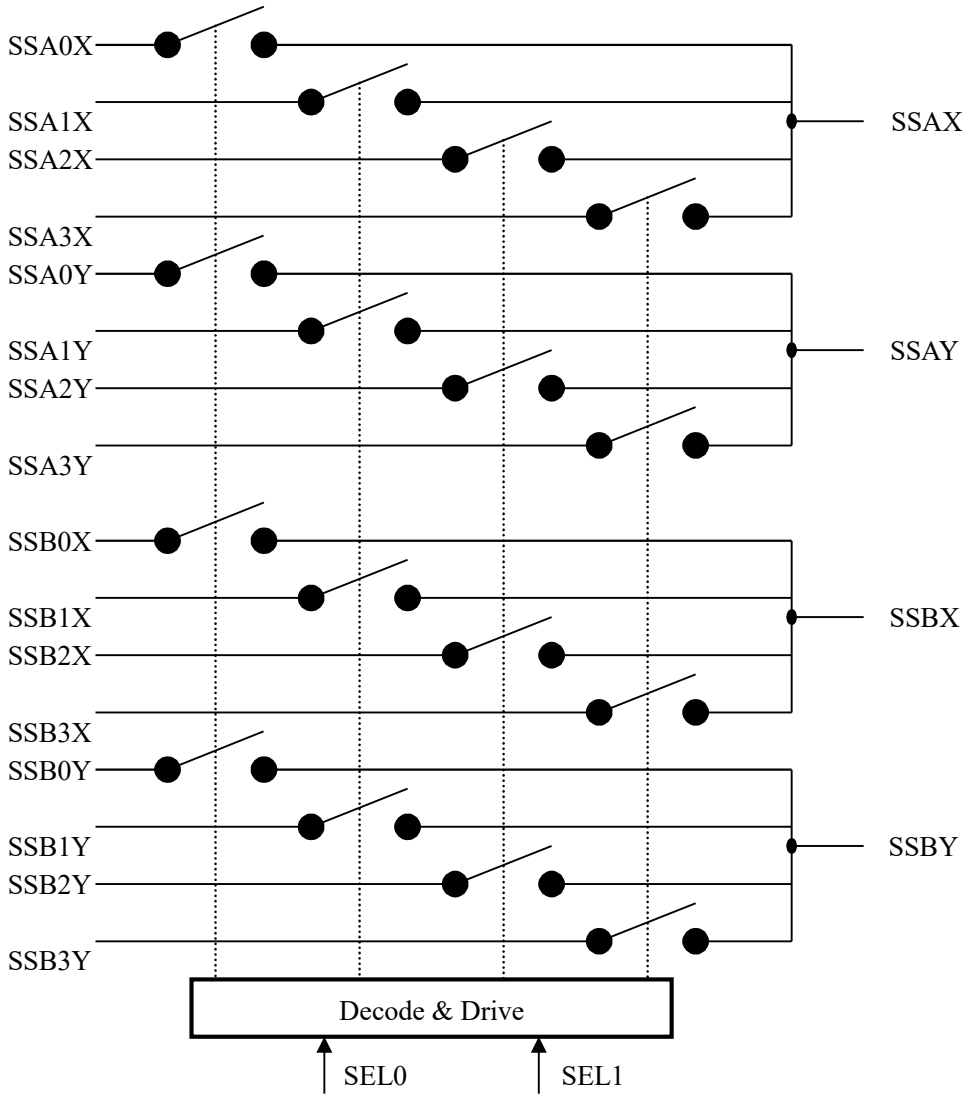
HSEN#	HSSEL	HSX	HSY
0	0	Select HS0X	Select HS0Y
0	1	Select HS1X	Select HS1Y
1	X	All off	All off

5.4. CH484M

CH484M is a QPQT broadband super speed bidirectional analog switch chip, which contains 2 differential

channels of 4:1 MUX analog switch (4 channels 4:1 in total), which can be used for one-of-four switch of differential signals not more than 1.7V voltage and 5Gbps.

SSAX and SSAY constitute the super speed differential channel SSA. SSBX and SSBY constitute the super speed differential channel SSB. The differential signals X and Y can be set to +/- (p/n) or the vice versa according to PCB design optimization requirements. Channel SSA and SSB can be set to TX/RX or vice versa according to PCB design optimization requirements.



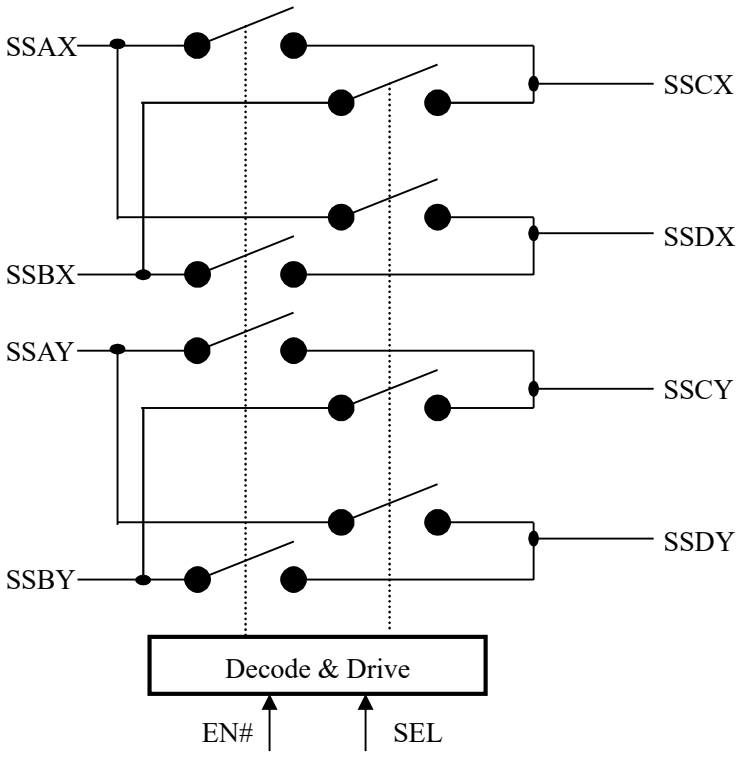
CH484M channels are always enabled, with SEL1 and SEL0 pins selecting the switch of channels. The following table is its control table.

SEL1	SEL0	SSAX	SSAY	SSBX	SSBY
0	0	Select SSA0X	Select SSA0Y	Select SSB0X	Select SSB0Y
0	1	Select SSA1X	Select SSA1Y	Select SSB1X	Select SSB1Y
1	0	Select SSA2X	Select SSA2Y	Select SSB2X	Select SSB2Y
1	1	Select SSA3X	Select SSA3Y	Select SSB3X	Select SSB3Y

5.5. CH481D

CH481D is a 2*2 matrix exchange broadband super speed analog switch chip, which contains 2 differential channels of 2:2 MUX analog switch (2-channel 2:2 Exchange Switch in total), which can be used for the physical layer routing of differential signals not more than 1.7V voltage and 6Gbps.

SSAX and SSAY constitute SSA ports of super speed differential channels. SSBX and SSBY constitute the SSB ports of the super speed differential channels, while SSCX and SSCY constitute the SSC ports of the super speed differential channels. SSDX and SSDY constitute the SSDs port of the super speed differential channels. The differential signals X and Y can be set to +/- (p/n) or the vice versa according to PCB design optimization requirements. Ports SSA, SSB, SSC and SSD can be set to TX/RX or vice versa according to PCB design optimization requirements.



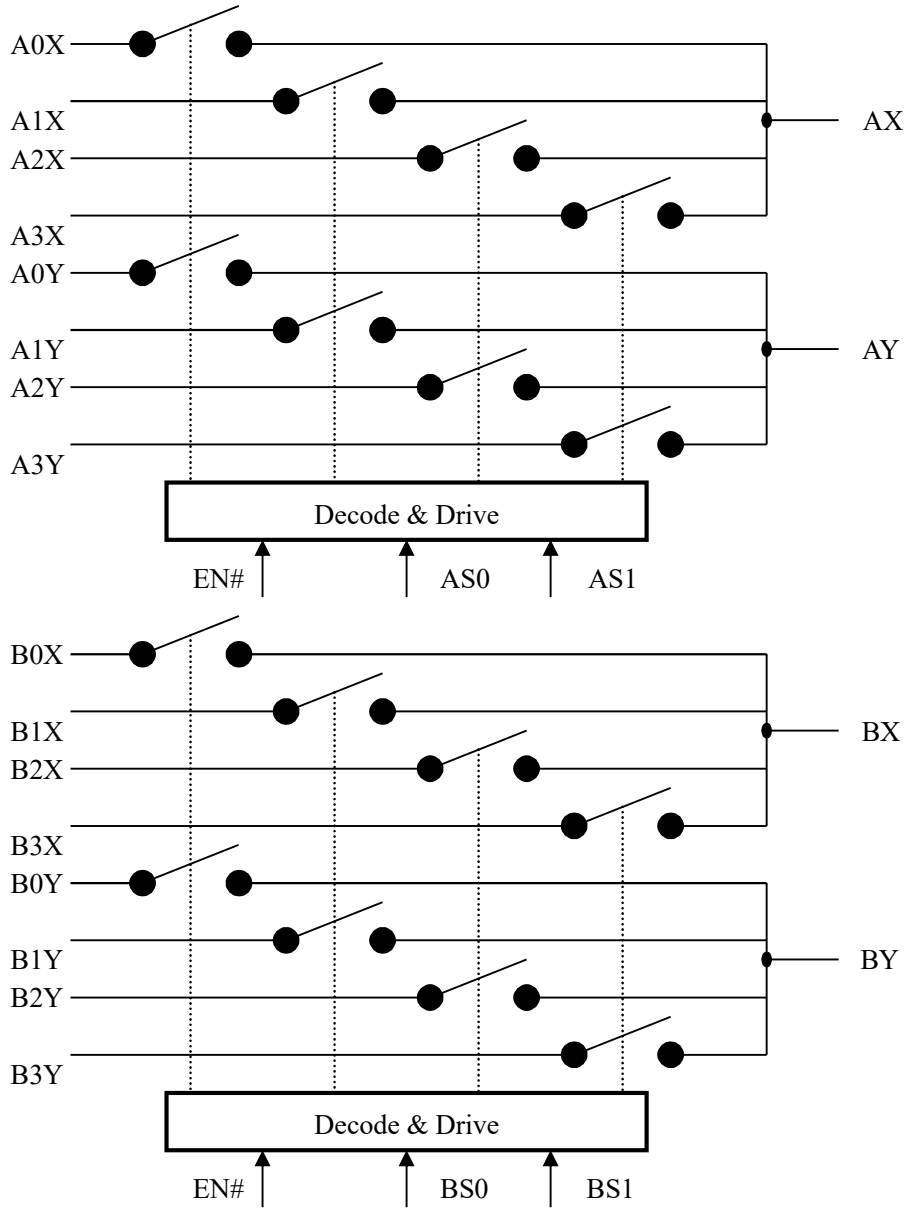
CH481D is uniformly enabled by the control of EN# pin, and switched by SEL pin select. The following table is its control table.

EN#	SEL	SSAX	SSAY	SSBX	SSBY	Description
0	0	Select SSCX	Select SSCY	Select SSDX	Select SSDY	A=C, B=D
0	1	Select SSCX	Select SSDY	Select SSDY	Select SSCY	A=D, B=C
1	X	All off	All off	All off	All off	

5.6. CH486F

CH486F is a QPQT broadband high speed bidirectional analog switch chip, which contains 2 differential channels of 4:1 MUX analog switch (4 channels 4:1 in total), which can be used for one-of-four switch of differential signals not more than 1.5Gbps.

AX and AY constitute the high speed differential channel A. BX and BY constitute the high speed differential channel B. The 2 differential channels are completely independently controlled. The differential signals X and Y can be set to +/- (p/n) or the vice versa according to PCB design optimization requirements. Channel A and B can be set to RX/TX or vice versa according to PCB design optimization requirements.



CH486F is uniformly enabled by the control of EN# pin. The switch of channel A is selected by AS1 and AS0 pins and the switch of channel B is selected by BS1 and BS0 pins. The following table is its control table.

EN#	AS1	AS0	AX	AY
0	0	0	Select A0X	Select A0Y
0	0	1	Select A1X	Select A1Y
0	1	0	Select A2X	Select A2Y
0	1	1	Select A3X	Select A3Y
1	X	X	All off	All off

EN#	BS1	BS0	BX	BY
0	0	0	Select B0X	Select B0Y
0	0	1	Select B1X	Select B1Y
0	1	0	Select B2X	Select B2Y
0	1	1	Select B3X	Select B3Y
1	X	X	All off	All off

6. Parameters

6.1. Absolute maximum ratings

Stresses at or above the absolute maximum ratings listed in the table below may cause permanent damage to the device.

Symbol	Parameter description	Min.	Max.	Unit
TA	Operating ambient temperature	-40	85	℃
TS	Storage ambient temperature	-55	150	℃
VCCH	VCCH supply voltage (VCCH connects to power, GND to ground)	-0.5	6.0	V
VDD	VDD and VDDH supply voltage (VDD/VDDH connects to power, GND to ground)	-0.4	3.8	V
VIOHX	Voltage on CH483X-HS digital or analog inputs/output pins	-0.5	VCCH+0.5	V
VIOHC	Voltage on digital input pins	-0.4	3.8	V
VIOHS	Voltage on HS analog switch input/output pins	-0.4	VDD+0.3	V
VIOSS	Voltage on SS analog switch input/output pins	-0.4	VDD	V
Isw	Continuous through current of analog switch	0	10	mA
Iall	Total continuous through current of all analog switches	0	100	mA

6.2. Electrical characteristics of CH482/3/4/1 super-speed channels

Test conditions: TA=25℃, VDD=3.3V

Symbol	Parameter description	Min.	Typ.	Max.	Unit
VDDS	VDD supply voltage (CH483M supports 2.5V power supply)	3.0/2.5	3.3	3.5	V
ICCS	Static supply current, EN#=GND, SEL=VDD or GND		80	500	uA
ICCSD	Power off supply current, EN#=VDD, SEL=VDD or GND		1	10	uA
VILS	Low level input voltage on digital pins	0		0.9	V
VIHS	High level input voltage on digital pins	1.9		VDD	V
ILEAKS	Input leakage current on digital pins		0.2	8	uA
IOFFS	Leakage current @1.7V of analog switch in off state		±2	±50	uA
VCMS	Recommended voltage range of analog signal	0		1.5	V
VCMXS	Allowable voltage range of analog signal	-0.2		1.7	V
RONS0	Analog switch ON resistance, 0V analog signal voltage		3.5	5	Ω
RONS1	Analog switch ON resistance, 1.5V analog signal voltage		9	13	Ω
RONS0X	CH482X/CH484M ON resistance, 0V signal voltage		5	7	Ω
RONS1X	CH482X/CH484M ON resistance, 1.5V signal voltage		13	17	Ω

6.3. Electrical characteristics of CH483M/6 high-speed channels

Test conditions: TA=25℃, VDDH=VCCH=VDD=3.3V)

Symbol	Parameter description	Min.	Typ.	Max.	Unit
VDDH	Supply voltage of CH486 HS	3.0	3.3	3.5	V

ICCH	Static supply current, HSEN#/HSSEL=VDD or GND, EN#/SEL/AS/BS=VDD or GND of CH486		1	10	uA
ICCXH	Static supply current, *EN#/*SEL/AS/BS=2.3V			500	uA
VILH	Low level input voltage on digital pins	0		0.9	V
VIHH	High level input voltage on digital pins	1.9		VDDH	V
ILEAKH	Input leakage current on digital pins		0.2	8	uA
IOFFH	Leakage current of analog switch in off state		±0.02	±2	uA
VCMH	Recommended voltage range of analog signal	0		VDDH	V
VCMXH	Allowable voltage range of analog signal	-0.2		VDDH+0.2	V
RONH0	Analog switch ON resistance, 0V analog signal voltage		3.5	5	Ω
RONH2	Analog switch ON resistance, 2.5V analog signal voltage		9	14	Ω
RONH3	Analog switch on resistance, analog signal voltage is VDDH		7.5	11	Ω

Notes: If the analog signal is lower than 2.5V, the CH48X can also support 2.5V power supply, but the high frequency characteristics are slightly worse and the ON resistance is higher.

6.4. Electrical characteristics at 5V of CH483X high-speed channels

Test conditions: TA=25℃, VCCH=5V

Symbol	Parameter description	Min.	Typ.	Max.	Unit
VCCH	Supply voltage of CH483X high speed channel HS	4.2	5.0	5.5	V
ICCH5	Static supply current, HSEN#/HSSEL=VDD or GND		0.1	10	uA
ICCXH5	Static supply current, HSEN#/HSSEL=3.4V		1	5	mA
VILH5	Low level input voltage on digital pins	0		1.0	V
VIHH5	High level input voltage on digital pins	2.0		VCCH	V
ILEAKH5	Input leakage current on digital pins		0.1	10	uA
IOFFH5	Leakage current of analog switch in off state		±0.01	±1	uA
VCMH5	Recommended voltage range of analog signal	0		VCCH	V
VCMXH5	Allowable voltage range of analog signal	-0.3		VCCH+0.3	V
RONH50	Analog switch ON resistance, 0V analog signal voltage		3.7	6	Ω
RONH53	Analog switch ON resistance, 3.3V analog signal voltage		9	14	Ω
RONH55	Analog switch ON resistance, analog signal voltage is VCCH		6	9	Ω

Notes: The CH483X high speed channel also supports 3.3V power supply, but the ON resistance is increased by about 60%. Refer to Section 6.3 for other characteristics.

6.5. Timing parameters of CH482/3/4/1 super-speed channels

Test conditions: TA=25℃, VDD=3.3V, VCM=0V

Symbol	Parameter description		Min.	Typ.	Max.	Unit
CIN	Digital input pin capacitance, F=1MHz			3	7	pF
DILS	CH482D/CH483 Differential insertion loss	0.1GHz		-0.33		dB
		2.5GHz		-0.6		dB
		4GHz		-1.2		dB
DOIS	Differential off-isolation	0.1GHz		-65		dB
		2.5GHz		-29		dB
		4GHz		-24		dB
DRLS	Differential return loss	0.1GHz		-29		dB
		2.5GHz		-16		dB
		4GHz		-11		dB
NECS	Near end crosstalk	0.1GHz		-70		dB
		2.5GHz		-48		dB
		4GHz		-32		dB
BWS3	CH482D/CH483 analog switch -3dB signal bandwidth		5	7		GHz
BWS2X	CH482X analog switch -3dB signal bandwidth		7	10		GHz
BWS4	CH484M analog switch -3dB signal bandwidth		3	4		GHz
BWS1	CH481D analog switch -3dB signal bandwidth		5	6.5		GHz
TONS	Analog switch on delay, RL=50Ω			1	20	uS
TSWS	Analog switch switching delay, RL=50Ω			9	80	nS
TOFFS	Analog switch off delay, RL=50Ω			6	25	nS

6.6. Timing parameters of CH483/6 high-speed channels

Test conditions: TA=25℃, VDDH/VDD=3.3V, VCM=0V

Symbol	Parameter description			Min.	Typ.	Max.	Unit
CIN	Digital input pin capacitance, F=1MHz				3	8	pF
DILH	Differential insertion loss	CH483M-HS	100MHz		-0.3		dB
			1GHz		-1.0		dB
		CH486F	100MHz		-0.32		dB
			1GHz		-1.7		dB
DOIH	Differential off-isolation	CH483M-HS	100MHz		-47		dB
			1GHz		-26		dB
		CH486F	100MHz		-47		dB
			1GHz		-25		dB
DRLH	Differential return loss	CH483M-HS	100MHz		-26		dB
			1GHz		-9.4		dB
		CH486F	100MHz		-24		dB
			1GHz		-7		dB

NECH	Near end crosstalk	CH483M-HS	100MHz		-84		dB
			1GHz		-35		dB
		CH486F	100MHz		-88		dB
			1GHz		-47		dB
BWH	Analog switch -3dB signal bandwidth	CH483M-HS		2.0	2.5		GHz
		CH486F		1.3	1.6		GHz
		CH483X-HS		0.35	0.5		GHz
TONH	Analog switch on delay, RL=50Ω				15	40	nS
TSWH	Analog switch switching delay, RL=50Ω				15	40	nS
TOFFH	Analog switch off delay, RL=50Ω				7	25	nS

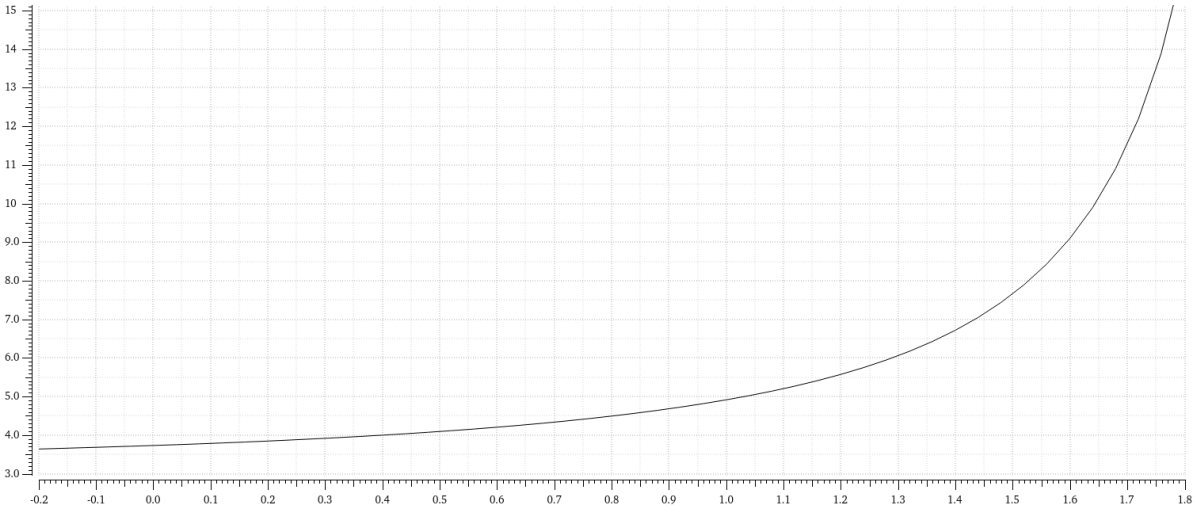
6.7. Other characteristics

Test conditions: TA=25℃

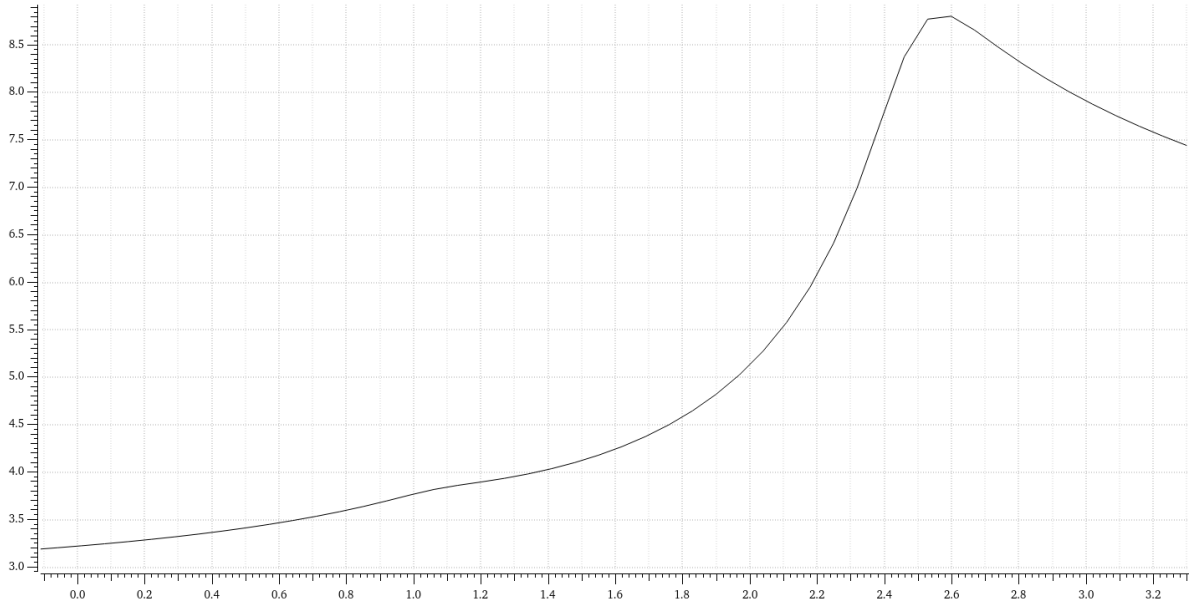
Symbol	Parameter description	Min.	Typ.	Max.	Unit
VESDSS	HBM ESD withstand voltage of SS	2	3		KV
VESDSSX	HBM ESD withstand voltage of CH482X/CH484M SS	1.6	2.5		KV
VESDHS	HBM ESD withstand voltage of HS	4	6		KV
VESDC	HBM ESD withstand voltage of digital pin	4	6		KV

6.8. Characteristic diagram (For reference only. Test condition: TA=25℃)

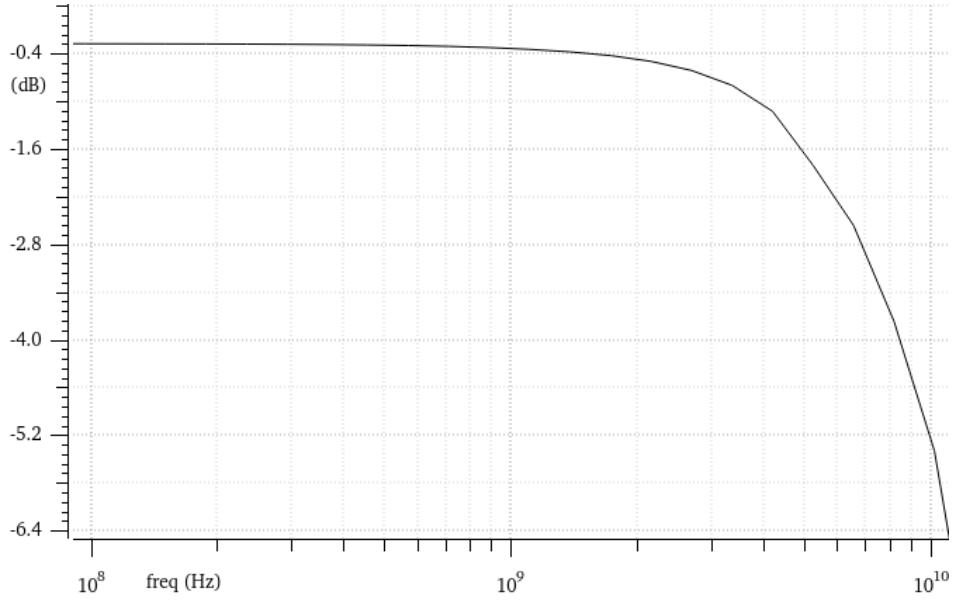
6.8.1 Correlation between analog switch ON resistance (RON) and analog signal voltage (VCOM) of CH482D/CH483/CH481D SS



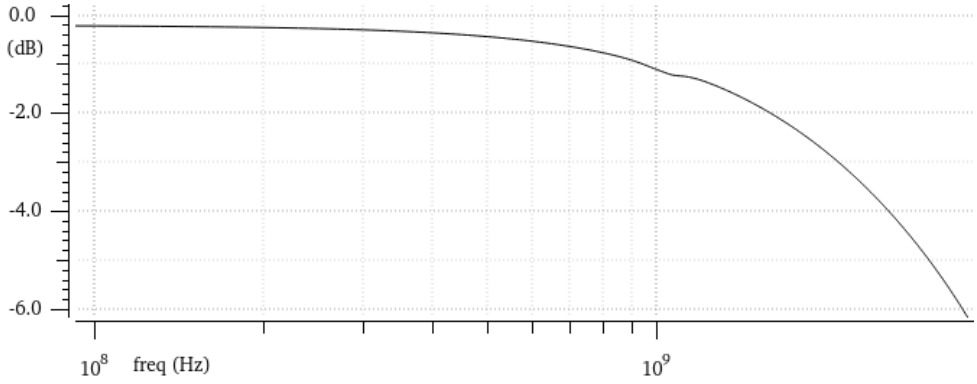
6.8.2 Correlation between analog switch ON resistance (RON) and analog signal voltage (VCOM) of HS



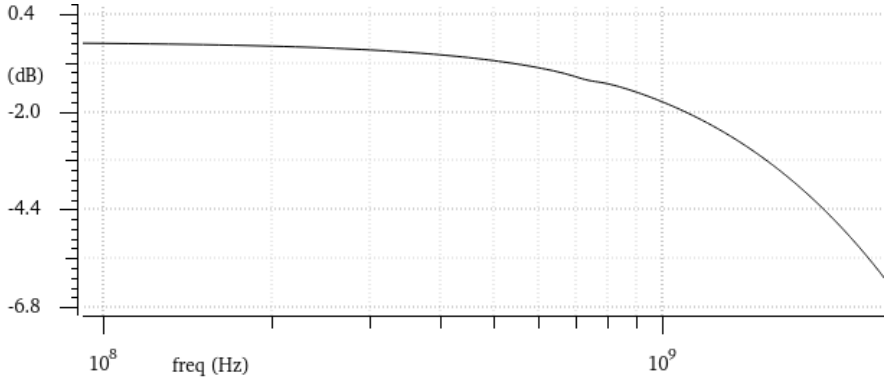
6.8.3 DILS high-frequency characteristics of CH482D/CH483/CH481D SS



6.8.4 DILH high-frequency characteristics of CH483M HS



6.8.5 DILH high frequency characteristics of CH486F HS



7. Applications

7.1. Super-speed/high-speed USB signal switch

The CH48X is a multiplexer/demultiplexer switch of multi-channel differential signals.

CH483M and CH483X can be used for 2:1 synchronous switch of USB 3.0 super speed signals and USB 2.0 high speed signals.

CH482D can be used for 2:1 synchronous switch of USB 3.0 Super-speed signals.

CH482X supports 10Gbps signals, with a slightly lower ESD performance. It is recommended to add an external high-frequency ESD protection device with small parasitic capacitance. The CH482X can be used for 2:1 switch of USB 3.1 and 3.2 Gen2 SuperSpeed+ signals.

CH484M can be used for 4:1 switch of USB 3.0 SuperSpeed signals.

Generally recommended analog ports: SSA corresponds to TX, SSB to RX, X to + or p, Y to - or n.

CH486F can be used for 4:1 MUX/DEMUX of USB 2.0 High Speed signals.

PSB design has a great influence on signal quality, transfer distance and compatibility, so it is recommended to refer to mature design. In PCB design, special attention must be paid to the wiring of the high frequency signals (impedance matching, differential pair matching, channel to channel matching, crosstalk and isolation, trace width, trace distance, ground plane, EMI, etc.). The function and connection of pins should be adjusted and optimized according to the convenience of PCB wiring. In addition, the power decoupling capacitor should be placed close to the power pins.

7.2. Other differential or non-differential signal switch

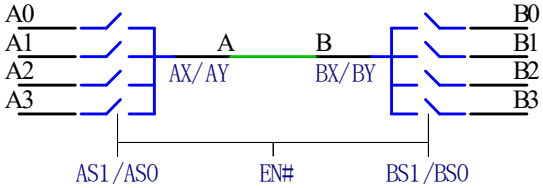
CH482D/X, CH483M/X and CH484M can be used for the switch of PCIe Gen1/2, SATA/SAS 1.5G/3G, Display Port and other differential signals. CH483M/X also supports synchronous switching of auxiliary differential signals PCIe Refclk.

CH482D/X and CH483M/X can also be used for SATA/SAS 6G, etc. CH482X can also be used for PCIe Gen3, etc.

All CH48X series can be used for the switch of non-differential signals and video signals.

7.3. CH486F differential pairing/routing

Refer to the figure below. Short AX/AY of CH486F to BX/BY respectively, select A*X/A*Y port via AS1/0, B*X/B*Y port via BS1/0, so as to implement repairing/rerouting of the signals between port A* and port B*.



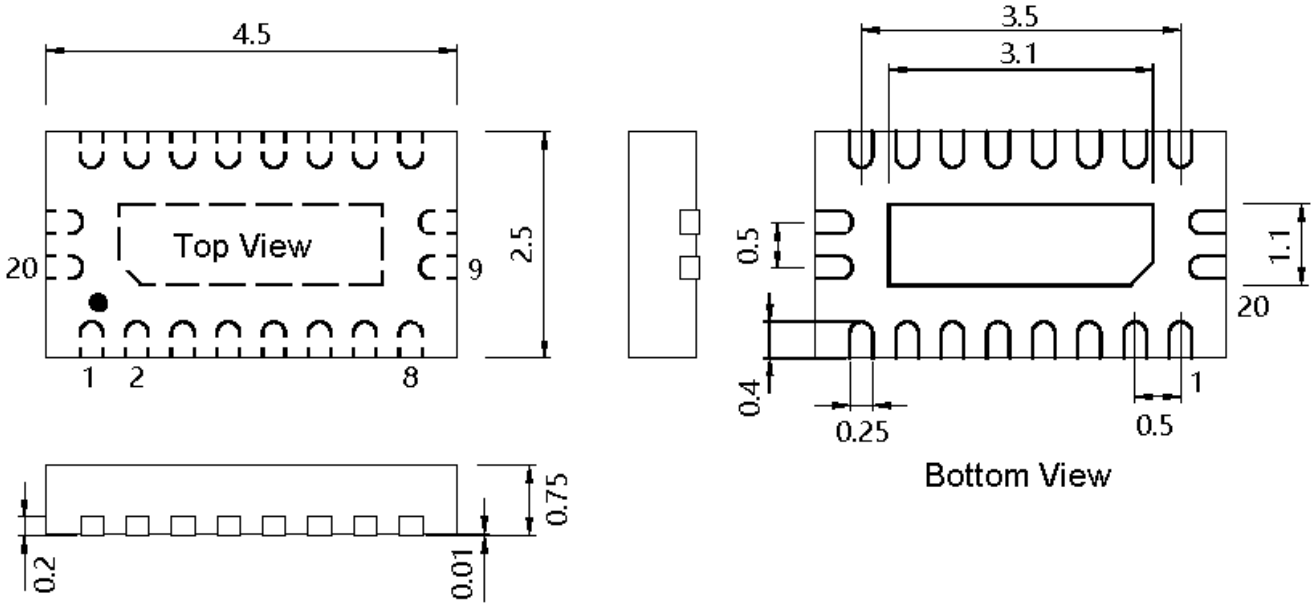
7.4. Cross/exchange between signal pairs

CH481D provides pass-through or exchange of the two-in-two-out signals, which can be used for the controllable exchange of 2 differential channels.

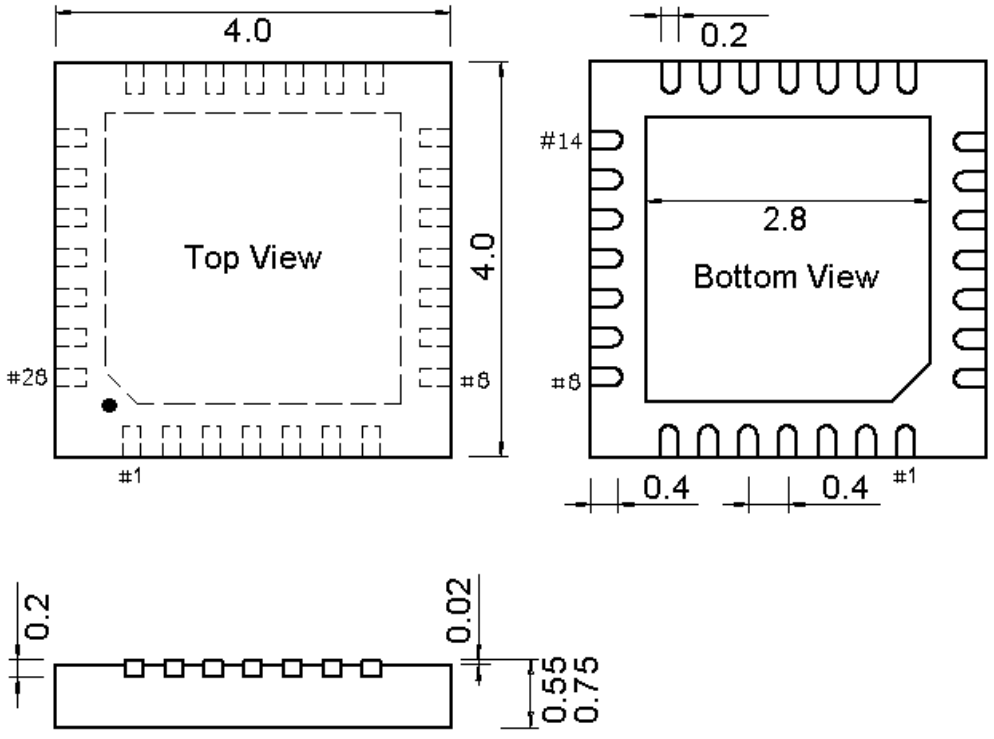
8. Package information

Note: All dimensions are in millimeters. The pin center spacing is a nominal value, and the error of other dimensions is not greater than ±0.2mm.

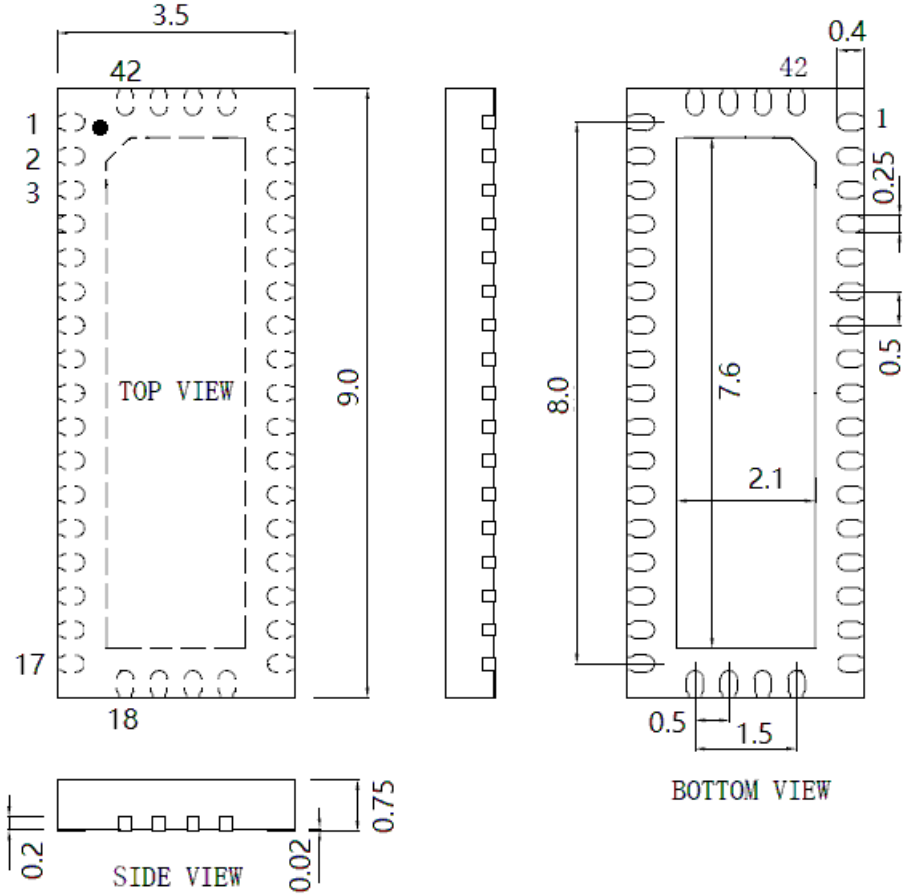
8.1. QFN20-2.5X4.5



8.2. QFN28-4X4



8.3. QFN42-3.5X9 (CH483M/X)



8.4. QFN42X-3.5X9 (CH484M)