CH182 Ethernet PHY Transceiver

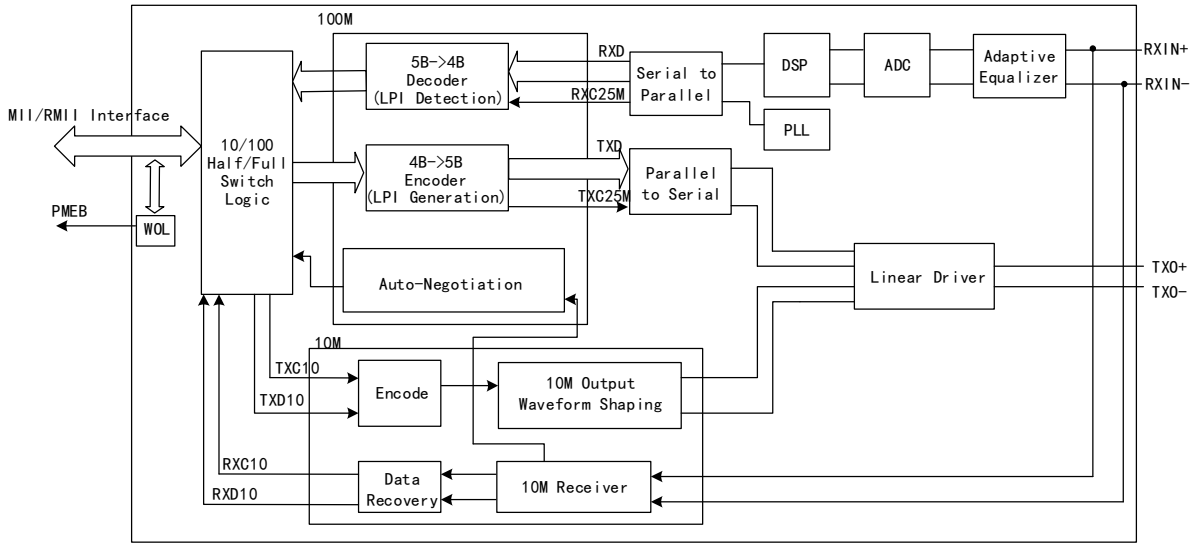
V1.6

https://wch-ic.com

1. Overview

CH182 is an industrial grade 10/100M Ethernet PHY transceiver with Auto-MDIX support. CH182 internally includes Physical Coding Sublayer (PCS), Physical Media Access Layer (PMA), Twisted Pair Physical Medium Dependent (TP-PMD), 10BASE-TX encoder/decoder, Twisted Pair Media Attachment Unit (TPMAU), MII and RMII interfaces, and other modules required for Ethernet Transceiver functions.

The following figure shows the block diagram of CH182.



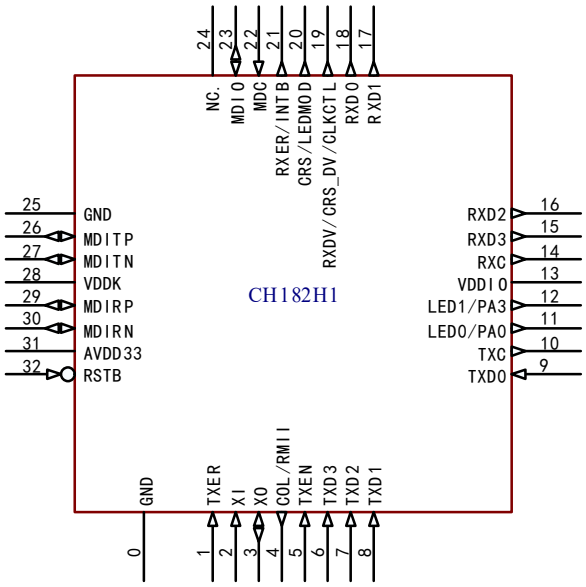
2. Feature

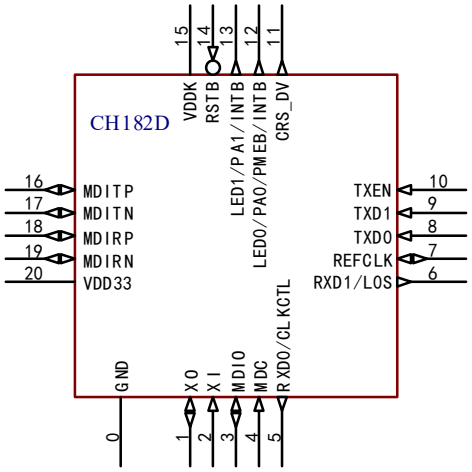
- Low-power Ethernet physical layer transceiver PHYceiver implemented based on DSP algorithm.
- Support downtime mode.
- Support Auto-MDIX switching TX/RX and automatic identification of positive and negative signal lines.
- Support 10BASE-T and 100BASE-TX and auto-negotiation.
- Support both MII and RMII interface modes.
- Support full-duplex and half-duplex operation.
- Support UTP CAT5 and CAT6 twisted pair cable, support 120m transmission distance.
- Built-in LDO buck, single 3.3V power supply.
- Independent I/O interface power supply, supporting 3.3V, 2.5V or 1.8V to adapt to processors or MCUs with different voltages.
- Built-in 50Ω impedance matching resistor, built-in capacitor required for 25MHz crystal oscillator, and streamlined peripheral circuitry.
- Optional support for external 50MHz clock input.
- Support WOL network wake-up.
- Support interrupt function.
- Support 2 types of network status LEDs.
- The CH182D chip has a built-in unique Ethernet MAC address that does not need to be purchased or assigned

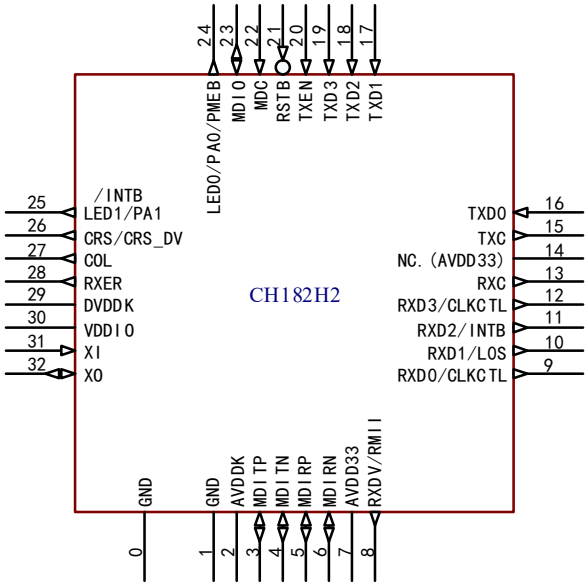
separately.

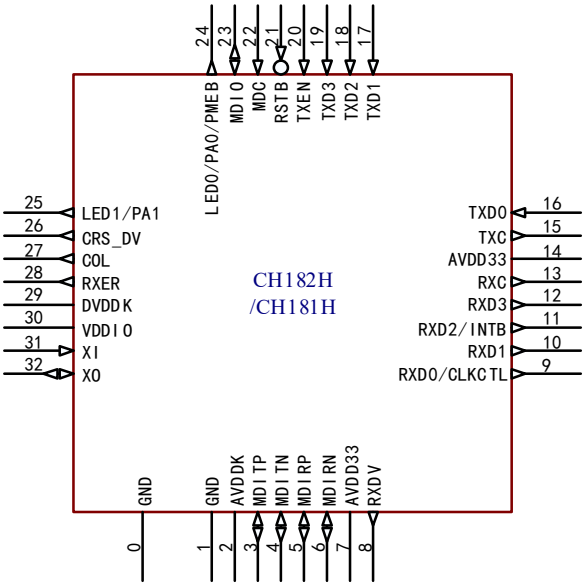
- Available in QFN32X5, QFN32 and QFN20 packages.

3. Pinouts









Package Form	Body Size	Pin Pitch		Package Description	Order Model
QFN32	4.0*4.0mm	0.40mm	15.7mil	Quad Flat No-lead Package	CH182H1
QFN20	3.0*3.0mm	0.40mm	15.7mil	Quad Flat No-lead Package	CH182D
QFN32X5	5.0*5.0mm	0.50mm	19.7mil	Quad Flat No-lead Package	CH182H2
QFN32X5	5.0*5.0mm	0.50mm	19.7mil	Quad Flat No-lead Package	CH182H
QFN32X5	5.0*5.0mm	0.50mm	19.7mil	Quad Flat No-lead Package	CH181H

Note: 1. CH182H2 is an upgraded version of CH182H and is pin compatible.

2. New design available CH182D/CH182H1/CH182H2, it is recommended to prefer small size CH182D or CH182H1.

3. Customized pins CH182H3, CH182H6, CH182H7, CH182H8, CH182F2, CH182F7, CH182F8, are only available in bulk quantity, please refer to the "CH182DS3" for pin arrangement and pin definition.

4. Pin Definitions

Table 4-1 CH182H1 pin definitions

<table>
<tr><th>Pin No.
182H1</th><th>Pin name</th><th>Type</th><th>Pin description</th></tr>
<tr><td>0</td><td>GND</td><td>P</td><td>Common ground.</td></tr>
<tr><td>1</td><td>TXER</td><td>I, PD</td><td>Transmit error indication.</td></tr>
<tr><td>2</td><td>XI</td><td>I</td><td>Crystal oscillator input, requires an external 25MHz crystal end, and external 25MHz or 50MHz clock input is optional.
RMII is connected to GND in slave mode, and TXC/REFCLKI is connected to 50MHz clock.</td></tr>
<tr><td>3</td><td>XO</td><td>I/O</td><td>The inverted output of crystal oscillator needs to be externally connected to the other end of 25MHz crystal.
Or when XI is connected to GND, XO is used to input external 25MHz or 50MHz clock.</td></tr>
<tr><td>4</td><td>COL/RMII</td><td>LI,
O, PD</td><td>Collision monitoring (COL):
COL outputs a high level when a collision is detected.

RMII mode selection (RMII):
During power-on reset,
By default, the internal pull-down resistor is set low =MII interface mode;
Optional external 4.7KΩ pull-up resistor set high =RMII interface mode.</td></tr>
<tr><td>5</td><td>TXEN</td><td>I</td><td>Transmit enable (TXEN).</td></tr>
<tr><td>6</td><td>TXD3</td><td>I</td><td rowspan="4">Transmit data bit TXD[3:0]:
Driven by MAC, it provides parallel transmission data to PHY.
When TXEN is enabled:
In MII mode, TXD[3:0] data is valid;
In RMII mode, TXD[1:0] data is valid.</td></tr>
<tr><td>7</td><td>TXD2</td><td>I</td></tr>
<tr><td>8</td><td>TXD1</td><td>I</td></tr>
<tr><td>9</td><td>TXD0</td><td>I</td></tr>
<tr><td>10</td><td>TXC
/REFCLKI</td><td>I/O</td><td>MII mode transmit clock (TXC):
In MII mode, this pin provides a reference clock for TXD[3:0] and TXEN signals. TXC is 25MHz and 2.5MHz in 100Mbps and 10Mbps modes, respectively.

RMII mode 50MHz clock input (REFCLKI):
In RMII mode, this mode is used for 50MHz clock input.</td></tr>
<tr><td>11</td><td>LED0/PA0</td><td>LI, O
PD</td><td>LED0:
Traditional LED function selection, the default LED_SEL is 01:
<table>
<tr><th>LED_SEL</th><th>00</th><th>01</th><th>10</th><th>11</th></tr>
<tr><td>LED0</td><td>ACT_{ALL}</td><td>$LINK_{ALL}$
/ACT_{ALL}</td><td>$LINK_{10}$
/ACT_{ALL}</td><td>$LINK_{10}$
/ACT_{10}</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Pin No.
182H1</th><th>Pin name</th><th>Type</th><th>Pin description</th></tr>
<tr><td></td><td></td><td></td><td>PHY address[0](PA0):
Latch the value of PHY address [0] at power-on,
Default set low by internal pull-down resistor = 0;
Optional external 4.7KΩ pull-up resistor set high = 1.</td></tr>
<tr><td>12</td><td>LED1/PA3</td><td>LI, O
PD</td><td>LED1：
Traditional LED function selection, the default LED_SEL is 01:
<table><tr><th>LED_SEL</th><th>00</th><th>01</th><th>10</th><th>11</th></tr><tr><td>LED1</td><td>$LINK_{100}$</td><td>$LINK_{100}$</td><td>$LINK_{100}$</td><td>$LINK_{100}$
/ACT_{100}</td></tr></table>
PHY address[3](PA3):
Latch the value of PHY address [3] at power-on,
By default, the internal pull-down resistor is set low = 0;
Optional external 4.7KΩ pull-up resistor is set high = 1.</td></tr>
<tr><td>13</td><td>VDDIO</td><td>P</td><td>The power input of I/O interface is externally connected with 0.1uF capacitance to ground.</td></tr>
<tr><td>14</td><td>RXC
/REFCLKO</td><td>O</td><td>Output receive clock (RXC):
This pin provides a continuous working clock for RXD[3:0] and RXDV signals.
RXC is 25MHz and 2.5MHz in 100Mbps and 10Mbps modes, respectively.

RMII mode 50MHz clock output (REFCLKO):
In RMII mode, 50MHz clock output.</td></tr>
<tr><td>15</td><td>RXD3</td><td>O</td><td rowspan="4">Received data bits RXD[3:0]:
Driven by PHY, it provides parallel received data to MAC.</td></tr>
<tr><td>16</td><td>RXD2</td><td>O</td></tr>
<tr><td>17</td><td>RXD1</td><td>O</td></tr>
<tr><td>18</td><td>RXD0</td><td>O</td></tr>
<tr><td>19</td><td>RXDV
/CRS_DV
/CLKCTL</td><td>LI,
O,PD</td><td>Received data valid (RXDV):
In MII mode, when RXD[3:0] receives data, this pin outputs a high level; Is pulled low when receiving is completed; Effective on the rising edge of RXC.

Carrier detection/reception data valid (CRS_DV):
In RMII mode, if the receiving medium is not idle, it outputs a high level.

Clock direction selection (CLKCTL):
In RMII mode, it is used to configure the direction of the reference clock according to the latched value of this pin during power-on:
The internal pull-down resistor is set low =RXC output clock;</td></tr>
</table>

Pin No. 182H1	Pin name	Type	Pin description
			Optional external 4.7KΩ pull-up resistor = TXC input clock.
20	CRS /LEDMOD	LI, O, PD	Carrier monitoring (CRS): In MII mode, the pin outputs a high signal indicating that it is transmitting or receiving, and outputs a low signal indicating that it is in an idle state. In RMII mode, this pin outputs a low level. LED mode selection (LEDMOD): During the power-on reset, The latched value of this pin is used to determine the value of LED_SEL[1], refer to the relevant description of the LED pin.
21	RXER /INTB	LI, O/OD	Receiving error indication (RXER). INTB: interrupt output, open-drain output. *Note: The function of this pin is determined by Page 1 Register 28.*
22	MDC	I, PU	Clock input of SMI management interface (MDC): This pin inputs a serial clock synchronized with MDIO, and has a built-in pull-up resistor to prevent the pin from floating.
23	MDIO	I/O, PU	Data input and output of SMI management interface (MDIO): This pin is used to input or output bidirectional serial data of management information.
24	NC.	NC.	Pin reserved, not connected internally.
25	GND	P	Optional common ground, connection is recommended.
26	MDITP	I/O	Differential output in 10BASE-T/100BASE-TX MDI mode; Differential input in 10BASE-T/100BASE-TX MDIX mode.
27	MDITN	I/O	
28	VDDK	P	The external 1uF capacitor to ground should be placed close to the chip.
29	MDIRP	I/O	Differential input in 10BASE-T/100BASE-TX MDI mode; Differential output in 10BASE-T/100BASE-TX MDIX mode.
30	MDIRN	I/O	
31	AVDD33	P	For 3.3V main power input, it is recommended to put 0.1uF parallel 10uF capacitor to ground close to the chip, or a single 1uF～4.7uF capacitor.
32	RSTB	I, PU	Reset input, active low.

Note: I = Input; O = Output; I/O = Input/Output; P = Power supply;
OD = Open-drain output; PD = Power-on reset internal pull-low; PU = Power-on reset internal pull-high;
LI = Pin status detected during power-up and latching input for functional configuration;
NC = Reserved pins.

Table 4-2 CH182H2/CH182D pin definitions

Pin No.		Pin name	Type	Pin description
182D	182H2			
0	0	GND	P	Common ground.
-	1	GND	P	Optional common ground, connection is recommended.
-	2	AVDDK	P	The external 1uF capacitor to ground is placed close to the chip.
15	-	VDDK	P	The external 1uF capacitor to ground is placed close to the chip.
16	3	MDITP	I/O	Differential output in 10BASE-T/100BASE-TX MDI mode; Differential input in 10BASE-T/100BASE-TX MDIX mode.
17	4	MDITN	I/O	
18	5	MDIRP	I/O	Differential input in 10BASE-T/100BASE-TX MDI mode; Differential output in 10BASE-T/100BASE-TX MDIX mode.
19	6	MDIRN	I/O	
-	7	AVDD33	P	3.3V main power supply input, it is recommended to place 0.1uF parallel 10uF capacitor to ground close to the chip, or a single 1uF~4.7uF capacitor.
20	-	VDD33	P	It is suggested that the 0.1uF parallel 10uF capacitor to ground should be placed close to the chip, or a single 1UF ~ 4.7UF capacitor.
-	8	RXDV /RMII	LI, O,PD	Received data valid (RXDV): In MII mode, when RXD[3:0] receives data, this pin outputs a high level; Is pulled low when receiving is completed; Effective on the rising edge of RXC. During power-on reset By default, the internal pull-down resistor is set low =MII interface mode. Optional external 4.7KΩ pull-up resistor set high =RMII interface mode.
5	9	RXD0 /CLKCTL	LI, O,PD	Receive data bit [0](RXD0). Clock direction selection (CLKCTL): In RMII mode, it is used to configure the direction of the reference clock according to the latched value of this pin during power-on: By default, the internal pull-down resistor is set low =TXC output clock; Optional external 4.7KΩ pull-up resistor set high =TXC input clock.
6	10	RXD1 /LOS	O,PD	Receive data bit [1](RXD1). LED0 function selection (LOS): By default, the pull-down resistor sets the low level =LED0 function internally; Optional external 4.7KΩ pull-up resistor set high =WOL function.

Pin No.		Pin name	Type	Pin description
182D	182H2			
-	11	RXD2 /INTB	LI, O/OD, PD	Receive data bit [2] (RXD2) INTB: In RMII mode, interrupt output and open-drain output.
-	12	RXD3 /CLKCTL	LI, O,PD	Receive data bit [3] (RXD3) Clock direction selection (CLKCTL): In RMII mode, it is used for configuration according to the latch value of this pin during power-on. Direction of reference clock: By default, the internal pull-down resistor is set low =TXC output clock; Optional external 4.7KΩ pull-up resistor set high =TXC input clock.
-	13	RXC	O,PD	Output receive clock (RXC): This pin provides a continuous working clock for RXD[3:0] and RXDV signals. RXC is 25MHz and 2.5MHz in 100Mbps and 10Mbps modes, respectively.
-	14	NC. (AVDD33)	NC. (P)	Pin reserved, not connected internally. In order to be compatible with the pins of CH182H, the external can also be connected to a 3.3V power supply.
-	15	TXC /REFCLK	I/O, PD	MII mode transmit clock (TXC): In MII mode, this pin provides a reference clock for TXD[3:0] and TXEN signals. TXC is 25MHz and 2.5MHz in 100Mbps and 10Mbps modes, respectively. 50MHz reference clock (REFCLK): In RMII mode, 50MHz clock input or output. The direction is determined by the RXD0/CLKCTL pin or page 7 register 16.
8	16	TXD0	I,PD	Transmit data bit TXD [3:0]: Driven by MAC, it provides parallel transmission data to PHY. When TXEN is enabled: In MII mode, TXD[3:0] data is valid; In RMII mode, TXD[1:0] data is valid.
9	17	TXD1	I,PD	
-	18	TXD2	I,PD	
-	19	TXD3	I,PD	
10	20	TXEN	I,PD	Transmit enable (TXEN).
14	21	RSTB	I,PU	Reset input, active low.
4	22	MDC	I,PU	Clock input of SMI management interface (MDC): This pin inputs a serial clock synchronized with MDIO, built-in pull-up resistor prevents pin from floating.
3	23	MDIO	I/O,	Data input and output of SMI management interface (MDIO):

<table>
<tr><th colspan="2">Pin No.</th><th rowspan="2">Pin name</th><th rowspan="2">Type</th><th rowspan="2">Pin description</th></tr>
<tr><th>182D</th><th>182H2</th></tr>
<tr><td></td><td></td><td></td><td>PU</td><td>This pin is used to input or output bidirectional serial data of management information.</td></tr>
<tr><td>-</td><td>24</td><td>LED0
/PA0
/PMEB</td><td>LI,
O/OD,
PU</td><td>LED0:
Traditional LED function selection, the default LED_SEL is 11:
<table><tr><td>LED_SEL</td><td>00</td><td>01</td><td>10</td><td>11</td></tr><tr><td>LED0</td><td>ACT_{ALL}</td><td>$LINK_{ALL}$
/ACT_{ALL}</td><td>$LINK_{10}$
/ACT_{ALL}</td><td>$LINK_{10}$
/ACT_{10}</td></tr></table>
PHY address[0] (PA0):
Latch the value of PHY address [0] at power-on,
By default, the internal pull-up resistor is set to high level = 1;
Optional external pull-down resistor is set low =0.

Power management event output (PMEB):
WOL power management event output, active low.
If a magic packet or wake-up frame is received, a low level is output.
Note: The function of this pin is determined by Page 1 Register 28.</td></tr>
<tr><td>13</td><td>25</td><td>LED1
/PA1
/INTB</td><td>LI,
O/OD,
PD</td><td>LED1:
Traditional LED function selection, the default LED_SEL is 11:
<table><tr><td>LED_SEL</td><td>00</td><td>01</td><td>10</td><td>11</td></tr><tr><td>LED1</td><td>$LINK_{100}$</td><td>$LINK_{100}$</td><td>$LINK_{100}$</td><td>$LINK_{100}$
/ACT_{100}</td></tr></table>
PHY address[1] (PA1):
Latch the value of PHY address [1] at power-on,
By default, the internal pull-down resistor sets the low level = 0;
Optional external 4.7KΩ pull-up resistor is set high =1.

INTB: interrupt output, open-drain output.
Note: The function of this pin is determined by Page 1 Register 28.</td></tr>
<tr><td>-</td><td>26</td><td>CRS
/CRS_DV</td><td>O,PD</td><td>Carrier detection (CRS):
In MII mode, the pin outputs a high-level signal indicating that it is transmitting or receiving, and a low-level signal indicating that it is in an idle state.

Carrier detection/reception data is valid. (CRS_DV):
In RMII mode, if the receiving medium is not idle, it outputs a high level.</td></tr>
</table>

<table>
<tr><th colspan="2">Pin No.</th><th rowspan="2">Pin name</th><th rowspan="2">Type</th><th rowspan="2">Pin description</th></tr>
<tr><th>182D</th><th>182H2</th></tr>
<tr><td>-</td><td>27</td><td>COL</td><td>O,PD</td><td>Collision monitoring (COL): When a collision is detected, COL outputs a high level.</td></tr>
<tr><td>-</td><td>28</td><td>RXER</td><td>O,PD</td><td>Receive error indication (RXER).</td></tr>
<tr><td>-</td><td>29</td><td>DVDDK</td><td>P</td><td>An external capacitor of 0.1 UF (0.1UF ~ 1UF) is placed close to the chip.</td></tr>
<tr><td>-</td><td>30</td><td>VDDIO</td><td>P</td><td>The power input of I/O interface is externally connected with 0.1uF capacitance to ground.</td></tr>
<tr><td>2</td><td>31</td><td>XI</td><td>I</td><td>Crystal oscillator input requires an external 25MHz crystal end, and external 25MHz or 50MHz clock input is optional.</td></tr>
<tr><td>1</td><td>32</td><td>XO</td><td>I/O</td><td>The inverted output of crystal oscillator needs to be externally connected to the other end of 25MHz crystal.
Or when XI is connected to GND, XO is used to input external 25MHz or 50MHz clock.</td></tr>
<tr><td>12</td><td>-</td><td>LED0/PA0
/PMEB
/INTB</td><td>LI,
O/OD,
PU</td><td>LED0:
Traditional LED function selection, the default LED_SEL is 11:
<table>
<tr><td>LED_SEL</td><td>00</td><td>01</td><td>10</td><td>11</td></tr>
<tr><td>LED0</td><td>ACT_{ALL}</td><td>$LINK_{ALL}$ /ACT_{ALL}</td><td>$LINK_{10}$ /ACT_{ALL}</td><td>$LINK_{10}$ /ACT_{10}</td></tr>
</table>
PHY address[0] (PA0):
Latch the value of PHY address [0] at power-on,
By default, the internal pull-up resistor is set to high level = 1;
Optional external pull-down resistor is set low =0.

Power management event output (PMEB):
WOL power management event output, active low.
If a magic packet or wake-up frame is received, a low level is output.

INTB: interrupt output, open-drain output.
Note: The function of this pin is determined by Page 1 Register 28.</td></tr>
<tr><td>7</td><td>-</td><td>REFCLK</td><td>I/O,
PD</td><td>50MHz reference clock (REFCLK):
In RMII mode, this pin is used to output or input the 50MHz reference clock REFCLK. The direction is determined by the RXD0/CLKCTL pin or page 7 register 16.</td></tr>
<tr><td>11</td><td>-</td><td>CRS_DV</td><td>O, PD</td><td>Carrier detection/reception data is valid. (CRS_DV):
If the receiving medium is not in an idle state, a high level is output.</td></tr>
</table>

Note: I = Input; O = Output; I/O = Input/Output; P = Power supply;
OD = Open-drain output; PD = Power-on reset internal pull-low; PU = Power-on reset internal pull-high;
LI = Pin status detected during power-up and latching input for functional configuration;

NC = Reserved pins.

Table 4-3 CH182H/CH181H pin definitions

Pin No.		Pin name	Type	Pin description
CH181H	CH182H			
0	0	GND	P	Common ground.
1	1	GND	P	Optional common ground, connection is recommended.
2	2	AVDDK	P	The external 1uF capacitor to ground is placed close to the chip.
3	3	MDITP	I/O	Differential output in 10BASE-T/100BASE-TX MDI mode; Differential input in 10BASE-T/100BASE-TX MDIX mode.
4	4	MDITN	I/O	
5	5	MDIRP	I/O	Differential input in 10BASE-T/100BASE-TX MDI mode; Differential output in 10BASE-T/100BASE-TX MDIX mode.
6	6	MDIRN	I/O	
7	7	AVDD33	P	3.3V main power supply input, it is recommended to place 0.1uF parallel 10uF capacitor to ground close to the chip, or a single 1uF～4.7uF capacitor.
8	8	RXDV	LI, O,PD	Receive data valid (RXDV). When RXD[3:0] receives data, this pin outputs a high level; Is pulled low when receiving is completed; Effective on the rising edge of RXC. During power-on reset, PHY detects the MAC interface mode configured on this pin: By default, the internal pull-down resistor set low =MII interface mode; Optional external 4.7KΩ pull-up resistor set high =RMII interface mode.
9	9	RXD0 /CLKCTL	LI, O,PD	Receive data bit [0] (RXD0). Clock direction selection (CLKCTL): In RMII mode, it is used to configure the direction of the reference clock according to the latched value of this pin during power-on: By default, the internal pull-down resistor set low =TXC output clock; Optional external 4.7KΩ pull-up resistor set high =TXC input clock.
10	10	RXD1	O,PD	Receive data bit [1] (RXD1).
11	11	RXD2 /INTB	LI, O,PD	Receive data bit [2] (RXD2). INTB: In RMII mode, interrupt output and open-drain output.
12	12	RXD3	O,PD	Receive data bit [3] (RXD3).
13	13	RXC	O,PD	Output receive clock (RXC). This pin provides a continuous working clock for RXD[3:0] and RXDV signals. RXC is 25MHz and 2.5MHz in 100Mbps and

<table>
<tr><th colspan="2">Pin No.</th><th rowspan="2">Pin name</th><th rowspan="2">Type</th><th rowspan="2">Pin description</th></tr>
<tr><th>CH181H</th><th>CH182H</th></tr>
<tr><td></td><td></td><td></td><td></td><td>10Mbps modes, respectively.</td></tr>
<tr><td>14</td><td>14</td><td>AVDD33</td><td>P</td><td>Optional 3.3V power input.</td></tr>
<tr><td>15</td><td>15</td><td>TXC
/REFCLK</td><td>I/O,
PD</td><td>MII mode outputs the transmission clock, and RMI mode outputs or inputs the reference clock. In MII mode, this pin provides a reference clock for TXD[3:0] and TXEN signals. TXC is 25MHz and 2.5MHz in 100Mbps and 10Mbps modes, respectively.

In RMII mode, this pin is used to output or input the 50MHz reference clock REFCLK. The direction is determined by the RXD0/CLKCTL pin or page 7 register 16.</td></tr>
<tr><td>16</td><td>16</td><td>TXD0</td><td>I,PD</td><td rowspan="4">Tansit TXD[3:0].
Driven by MAC, it provides parallel transmission data to PHY.
When TXEN is enabled, TXD[0:3] data is valid.</td></tr>
<tr><td>17</td><td>17</td><td>TXD1</td><td>I,PD</td></tr>
<tr><td>18</td><td>18</td><td>TXD2</td><td>I,PD</td></tr>
<tr><td>19</td><td>19</td><td>TXD3</td><td>I,PD</td></tr>
<tr><td>20</td><td>20</td><td>TXEN</td><td>I,PD</td><td>Transmit enable (TXEN).</td></tr>
<tr><td>21</td><td>21</td><td>RSTB</td><td>I,PU</td><td>Reset input, active low.</td></tr>
<tr><td>22</td><td>22</td><td>MDC</td><td>I,PU</td><td>Clock input of SMI management interface (MDC).
This pin inputs a serial clock synchronized with MDIO and has a built-in pull-up resistor to prevent the pin from floating.</td></tr>
<tr><td>23</td><td>23</td><td>MDIO</td><td>I/O,
PU</td><td>Data input and output of SMI management interface (MDIO).
This pin is used to input or output bidirectional serial data of management information.</td></tr>
<tr><td>24</td><td>24</td><td>LED0
/PA0
/PMEB</td><td>LI,
O/O
D,PU</td><td>Address of SMI management interface of PHY and custom LED settings.
The default LED pin is LED function:
The PHY address is selected by PA1 and PA0: 00000 ~ 00011, and the default value is 01;
Traditional LED function selection, the default LED_SEL is 11:</td></tr>
<tr><td>25</td><td>25</td><td>LED1
/PA1</td><td>LI,
O,PD</td><td>
<table>
<tr><th>LED_SEL</th><th>00</th><th>01</th><th>10</th><th>11</th></tr>
<tr><td>LED0</td><td>ACT_{ALL}</td><td>$LINK_{ALL}$
/ACT_{ALL}</td><td>$LINK_{10}$
/ACT_{ALL}</td><td>$LINK_{10}$
/ACT_{10}</td></tr>
<tr><td>LED1</td><td>$LINK_{100}$</td><td>$LINK_{100}$</td><td>$LINK_{100}$</td><td>$LINK_{100}$
/ACT_{100}</td></tr>
<tr><td>LED2</td><td>Reserved</td><td>Reserved</td><td>Reserved</td><td>Reserved</td></tr>
</table>
Note: CH181HLED flicker judgment signal is an Ethernet carrier signal.

Power management event output (PMEB):
WOL power management event output, active low.</td></tr>
</table>

Pin No.		Pin name	Type	Pin description
CH181H	CH182H			
				If a magic packet or wake-up frame is received, a low level is output.
26	26	CRS_DV	O,PD	Carrier detection/reception data valid. (CRS_DV). If the receiving medium is not in an idle state, a high level is output.
27	27	COL	O,PD	Collision monitoring (COL): When a collision is detected, COL outputs a high level.
28	28	RXER	O,PD	Receive error indication (RXER).
29	29	DVDDK	P	An external capacitor of 0.1 UF (0.1 UF ~ 1 UF) is placed close to the chip.
30	30	VDDIO	P	The power input of I/O interface is externally connected with 0.1uF capacitance to ground.
31	31	XI	I	Crystal oscillator input requires an external 25MHz crystal end or an external 25MHz clock input.
32	32	XO	I/O	The inverted output of crystal oscillator needs to be externally connected to the other end of 25MHz crystal. Or when XI is connected to GND, XO is used to input external 25MHz or 50MHz clock.

Note: I = Input; O = Output; I/O = Input/Output; P = Power supply;
OD = Open-drain output; PD = Power-on reset internal pull-low; PU = Power-on reset internal pull-high;
LI = Pin status detected during power-up and latching input for functional configuration;
NC = Reserved pins.

5. Register Description

Table 5-1 PHY register description

Register name (BASE)	Address	Default value
Control Register	0x00	3100h
Status Register	0x01	7849h
PHY Identifier	0x02/0x03	7371h/2XXXh
Auto-Negotiation Advertisement	0x04	01e1h
Auto-Negotiation Link Partner Ability	0x05	0001h
Auto-Negotiation Expansion	0x06	0044h
PAGE_SEL	0x1F	0000h
Register Name (PAGE 7) (Applicable to chips other than CH181H and CH182H)	Address	Default value
INTERRUPT_MASK	0x13	0030h
Register name (PAGE 18) (For CH182D chips only)	Address	Default value
MAC_PHY_ADDR0	0x1A	X
MAC_PHY_ADDR1	0x1B	X
MAC_PHY_ADDR2	0x1C	X

Note: 1. The default abbreviated form of the above register descriptions is as follows:

Reset Value: 1 = bit set to logic 1; *Access Type: RO = read-only;*

0 = bit set to logic 0; *RW = read/write;*

X = no default value; *RC = read clear.*

h = hexadecimal; *SC = self-clear.*

2. Other extended registers include interface timing, vendor-defined characteristics, etc., and usually do not need to be modified. For details, please refer to the CH182DS2 manual.

5.1 Register 0 Control Register

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th><th>Access</th><th>Default value</th></tr>
<tr><td>15</td><td>Reset</td><td>Software reset, automatically cleared after the reset is completed.</td><td>RW, SC</td><td>0</td></tr>
<tr><td>14</td><td>Loopback</td><td>Set the data path from sending to receiving.
1 = Enable Loopback; 0 = Normal operation.</td><td>RW</td><td>0</td></tr>
<tr><td>13</td><td>Speed Selection</td><td>Set the network speed.。
1 = 100Mbps； 0 = 10Mbps。
After auto-negotiation is completed, this bit reflects the speed status.
1 = 100BASE-T； 0 = 10BASE-T。
Note: The default value of some packages is determined according to the pin latch value.<table><tr><th>Package</th><th>Pin</th></tr><tr><td>CH182H8</td><td>LED1</td></tr><tr><td>CH182F8</td><td>LED0</td></tr><tr><td>CH182H3</td><td>LED1</td></tr><tr><td>CH182H7</td><td>{COL/CRS,RXD1,RXD0}</td></tr><tr><td>CH182F7</td><td>{CRS_DV,RXD1,RXD0}</td></tr></table></td><td>RW</td><td>1</td></tr>
<tr><td>12</td><td>Auto-Negotiation Enable</td><td>Auto-negotiation function
1 = Enable auto-negotiation, bit 13 and bit 8 will be ignored;
0 = Disable auto-negotiation, and bits 13 and 8 will determine the link speed and data transmission mode.
Note: The default value of some packages is determined according to the pin latch value.<table><tr><th>Package</th><th>Pin</th></tr><tr><td>CH182H8</td><td>LED0</td></tr><tr><td>CH182F8</td><td>LED0</td></tr><tr><td>CH182H3</td><td>RXD0</td></tr><tr><td>CH182H6</td><td>RXD0</td></tr><tr><td>CH182H7</td><td>{COL/CRS,RXD1,RXD0}</td></tr><tr><td>CH182F7</td><td>{CRS_DV,RXD1,RXD0}</td></tr></table></td><td>RW</td><td>1</td></tr>
<tr><td>11</td><td>Power Down</td><td>1= Turn off the power supply; 0= Normal operation.</td><td>RW</td><td>0</td></tr>
<tr><td>10</td><td>Isolate</td><td>1 = The MII/RMII interface is isolated from PHY, and PHY can still respond to MDC/MDIO;
0 = Normal operation.
Note: The initial power-on value of this bit is determined according to the corresponding pin latch value, and the soft reset will return to the default value.</td><td>RW</td><td>0</td></tr>
</table>

		Package / *Pin* *CH182H8* / *RXER* *CH182H3* / *RXER* *CH182H7* / *{COL/CRS,RXD1,RXD0}* *CH182F7* / *{CRS_DV,RXD1,RXD0}*		
9	Restart Auto-Negotiation	Restart auto negotiation. 1 = Restart auto negotiation; 0 = Normal operation.	RW, SC	0
8	Duplex Mode	Duplex mode. 1 = Full-duplex; 0 = Half-duplex. *Note: The default value of some packages is determined according to the pin latch value.* *Package* / *Pin* *CH182H8* / *RXD0* *CH182H7* / *{COL/CRS,RXD1,RXD0}* *CH182F7* / *{CRS_DV,RXD1,RXD0}*	RW	1
7	Collision Test	Collision test. 1 = Enable; 0 = Normal operation. When set to 1, COL signal will be generated within a period of time after TXEN is sent, and COL signal will also disappear after TXEN cancels sending for a period of time.	RW	0
6:0	Reserved	Reserved	RO	0

5.2 Register 1 Status Register

Bit	Name	Description	Access	Default value
15	100BASE-T4	1 = Support enabling 100BASE-T4; 0 = Not support 100BASE-T4.	RO	0
14	100BASE-TX Full Duplex	1 = Support enabling 100BASE-TX full-duplex; 0 = Not support 100BASE-TX full-duplex.	RO	1
13	100BASE-TX Half Duplex	1 = Support enabling 100BASE-TX half-duplex; 0 = Not support 100BASE-TX half-duplex.	RO	1
12	10BASE-T Full Duplex	1 = Support enabling 10BASE-T full-duplex; 0 = Not support 10BASE-T full-duplex.	RO	1
11	10BASE-T Half Duplex	1 = Support enabling 10BASE-T half-duplex; 0 = Not support 10BASE-T half-duplex.	RO	1
10	100BASE-T2 Full Duplex	1 = Support enabling 100BASE-T2 full-duplex; 0 = Not support 100BASE-T2 full-duplex.	RO	0
9	100BASE-T2 Half Duplex	1 = Support enabling 100BASE-T2 half-duplex; 0 = Not support 100BASE-T2 half-duplex.	RO	0
8	Extend Status	1 = Register 15 extension base register status information; 0 = Register 15 has no extended base register status	RO	0

		information.		
7	Reserved	Reserved	RO	0
6	MF Preamble Suppression	Management frames with preamble suppression are allowed to be received.	RO	1
5	Auto-Negotiation Complete	1 = The self-negotiation process is completed; 0 = The self-negotiation process was not completed.	RO	0
4	Remote Fault	1 = Remote error condition detected (Read clear); 0 = No remote error conditions were detected.	RO	0
3	Auto-Negotiation Ability	1 = PHY can perform self-negotiation; 0 = PHY cannot perform self-negotiation.	RO	1
2	Link Status	1 = A valid link has been established. 0 = No valid link has been established.	RO	0
1	Jabber Detect	1 = Jabber condition detected; 0 = Jabber condition not detected.	RO	0
0	Extended Capability	1= Extended register function; 0= No extended register function.	RO	1

5.3 Register 2 PHY Identifier Register 1

Bit	Name	Description	Access	Default value
15:0	OUI_MSB	The 6th to 21st organization unique identifiers assigned to OUI.	RO	7371h

5.4 Register 3 PHY Identifier Register 2

Bit	Name	Description	Access	Default value
15:10	OUI_LSB	The 0 to 5 organization unique identifiers assigned to the OUI.	RO	24h
9:4	VNDR_MDL	Identification code, the default value is used to distinguish between model and package.	RO	XXh
3:0	MDL_REV	Version number.	RO	Xh

5.5 Register 4 Auto-Negotiation Advertisement Register

Bit	Name	Description	Access	Default value
15	Next Page	Next page byte. 0= Transmit main function data page; 1= Send protocol rule data page.	RW	0
14	Acknowledge	1= Confirm the receipt of the peer-to-peer auto-negotiation function register; 0= No acknowledgement signal is received.	RO	0
13	Remote Fault	1= Notify the remote error detection function; 0= Notify the remote error detection function.	RW	0

<table>
<tr><td>12</td><td>Reserved</td><td>Reserved</td><td>RO</td><td>0</td></tr>
<tr><td>11</td><td>Asymmetric PAUSE</td><td>1= Support asymmetric suspension of notification;
0= Asymmetric pausing is not supported.</td><td>RW</td><td>0</td></tr>
<tr><td>10</td><td>Pause</td><td>1= Supports symmetric suspension of notification;
0= Symmetric pause is not supported.</td><td>RW</td><td>0</td></tr>
<tr><td>9</td><td>100BASE-T4</td><td>1 = PHY support 100BAES-T4;
0 = PHY does not support 100BASE-T4.</td><td>RO</td><td>0</td></tr>
<tr><td>8</td><td>100BASE-TX Full Duplex</td><td>1 = PHY support 100BASE-TX full-duplex;
0 = PHY does not support 100BASE-TX full-duplex.
Note: The default value of some packages is determined according to the pin latch value.<table><tr><th>Package</th><th>Pin</th></tr><tr><td>CH182H8</td><td>LED1</td></tr><tr><td>CH182F8</td><td>LED0</td></tr><tr><td>CH182H3</td><td>LED1</td></tr><tr><td>CH182H7</td><td>{COL/CRS,RXD1,RXD0}</td></tr><tr><td>CH182F7</td><td>{CRS_DV,RXD1,RXD0}</td></tr></table></td><td>RW</td><td>1</td></tr>
<tr><td>7</td><td>100BASE-TX</td><td>1 = PHY support 100BASE-TX;
0 = PHY does not support 100BASE-TX.
Note: The default value of some packages is determined according to the pin latch value.<table><tr><th>Package</th><th>Pin</th></tr><tr><td>CH182H8</td><td>LED1</td></tr><tr><td>CH182F8</td><td>LED0</td></tr><tr><td>CH182H3</td><td>LED1</td></tr><tr><td>CH182H7</td><td>{COL/CRS,RXD1,RXD0}</td></tr><tr><td>CH182F7</td><td>{CRS_DV,RXD1,RXD0}</td></tr></table></td><td>RW</td><td>1</td></tr>
<tr><td>6</td><td>10BASE-T Full Duplex</td><td>1 = PHY support 10BASE-T full-duplex;
0 = PHY does not support 10BASE-T full-duplex.
Note: The initial power-on value of this bit is determined according to the corresponding pin latch value, and the soft reset will return to the default value.<table><tr><th>Package</th><th>Pin</th></tr><tr><td>CH182H7</td><td>{COL/CRS,RXD1,RXD0}</td></tr><tr><td>CH182F7</td><td>{CRS_DV,RXD1,RXD0}</td></tr></table></td><td>RW</td><td>1</td></tr>
<tr><td>5</td><td>10BASE-T</td><td>1 = PHY support 10BASE-T;
0 = PHY does not support 10BASE-T.
Note: The default value of some packages is determined according to the pin latch value.<table><tr><th>Package</th><th>Pin</th></tr><tr><td>CH182H7</td><td>{COL/CRS,RXD1,RXD0}</td></tr><tr><td>CH182F7</td><td>{CRS_DV,RXD1,RXD0}</td></tr></table></td><td>RW</td><td>1</td></tr>
</table>

4:0	Selector Field	PHY supports binary code selector. At present, only CSMA/CD00001 is special, and no other protocols support it.	RO	00001

5.6 Register 5 Auto-Negotiation Link Partner Ability Register

This register receives the message function of the peer during auto-negotiation. If the next page function is supported, the content changes after a successful self-negotiation.

Bit	Name	Description	Access	Default value
15	Next Page	Next page byte. 1= Transmit a specific protocol data page; 0= Transmit main function data page. *Note: CH181H does not realize this function.*	RO	0
14	Acknowledge	1= The peer acknowledges the receipt of the local auto-negotiation function register; 0= Receipt not acknowledged.	RO	0
13	Remote Fault	1= The peer indicates a remote error; 0= The peer did not specify a remote error.	RO	0
12	Reserved	Reserved	RO	0
11	Asymmetric Pause	1 = Support asymmetric flow control; 0 = Asymmetric flow control is not supported. This bit reflects the function of the peer when auto-negotiation is enabled.	RO	0
10	Pause	1= Support flow control; 0= Flow control is not supported. This bit reflects the function of the peer when auto-negotiation is enabled.	RO	0
9	100BASE-T4	1 = The peer supports 100BASE-T4; 0 = The peer does not support 100BASE-T4.	RO	0
8	100BASE-TX Full Duplex	1 = The peer supports 100BASE-TX full-duplex; 0 = The peer does not support 100BASE-TX full-duplex.	RO	0
7	100BASE-TX	1 = The peer supports 100BASE-TX; 0 = The peer does not support 100BASE-TX.	RO	0
6	10BASE-T Full Duplex	1 = The peer supports 10BASE-T full-duplex; 0 = the peer supports 10BASE-T full-duplex.	RO	0
5	10BASE-T	1 = The peer supports 10base-t; 0 = The peer does not support 10base-t.	RO	0
4:0	Selector Field	At present, only CSMA/CD00001 is special for the binary coded node selector at the opposite end, and it does not support other protocols.	RO	0001b

5.7 Register 6 Auto-Negotiation Expansion Register

Bit	Name	Description	Access	Default value
15:7	Reserved	Reserved	RO	0h
6	NPLA	Indicate that storage location of the next page sent by the opposite end.	RO	0
5	NPSL	Indicates whether the next page of the peer is stored in register 8.	RO	0
4	Parallel Detection Fault	1= A fault was detected by the parallel detection function; 0= No fault was detected by the parallel detection function.	RC	0
3	Link Partner Next Page Able	1 = Support the next page; 0 = The next page is not supported. *Note: CH181H does not realize this function.*	RO	0
2	Local Next Page Able	1= The local device can transmit the next page; 0= The local device cannot transmit the next page.	RO	1
1	Page Received	1= A new page has been received; 0= No new page received.	RC	0
0	Link Partner Auto-Negotiation Able	If auto-negotiation is enabled: 1= The peer has auto-negotiation function; 0= The peer has no auto-negotiation function.	RO	0

5.8 Register 31 Page Selection Register PAGE_SEL

Bit	Name	Description	Access	Default value
15:8	Reserved	Reserved	RO	0
7:0	PAGE_SEL	Select a page address. 00000000~11111111.	RW	0

5.9 Page 7 Register 19 Interrupt, WOL Enable and LED Function Register INTERRUPT_MASK (Applicable to chips other than CH181H, CH182H)

Bit	Name	Description	Access	Default value
15	WOLDONE_EN	Enable WOL to complete the interrupt. 1= Enable WOL completion interrupt; 0= Disable WOL completion interrupt.	RW	0
14	INT_SPDCHG	Enable speed change interrupt. 1 = Enable speed changes interrupt; 0 = Enable speed changes interrupt. *Note: When this bit is set to 0, the link change interrupt event is only masked at the INTB pin, and bit 14 of page*	RW	0

<table>
<tr><td></td><td></td><td>0 register always reflects the speed change interrupt behavior.</td><td></td><td></td></tr>
<tr><td>13</td><td>INT_LINKCHG</td><td>Enable link change interrupt.
1 = Enable link changes interrupt;
0 = Disable link changes interrupt.
Note: When this bit is set to 0, the link change interrupt event is only masked at the INTB pin, and bit 11 of page 0 register always reflects the speed change interrupt behavior.</td><td>RW</td><td>0</td></tr>
<tr><td>12</td><td>INT_DUPCHG</td><td>Enable duplex change interrupt.
1 = Enable duplex changes interrupt;
0 = Disable duplex changes interrupt
Note: When this bit is set to 0, the link change interrupt event is only masked at the INTB pin, and bit 13 of page 0 register always reflects the speed change interrupt behavior.</td><td>RW</td><td>0</td></tr>
<tr><td>11</td><td>INT_ANERR</td><td>Enable self-negotiation error interrupt.
1 = Enable self-negotiation error interrupt;
0 = Disable self-negotiation error interrupt
Note: When this bit is set to 0, the link change interrupt event is only masked at the INTB pin, and bit 15 of page 0 register always reflects the self-negotiation error interrupt behavior.</td><td>RW</td><td>0</td></tr>
<tr><td>10</td><td>RG_LED0_WOL
_SEL</td><td>LED, Wake-On-LAN function selection
1 = Enable Wake-On-LAN function;
0 = Enable LED function.
Note: The default value of some packages is determined according to the pin latch value.
<table>
<tr><th>Package</th><th>Pin</th></tr>
<tr><td>CH182D</td><td>RXD1</td></tr>
<tr><td>CH182F2</td><td>RXD1</td></tr>
<tr><td>CH182H2</td><td>RXD1</td></tr>
<tr><td>CH182H1</td><td>CRS</td></tr>
</table></td><td>RW</td><td>0</td></tr>
<tr><td>9</td><td>INTERRUPT_LE
VEL</td><td>1 = Active high;
0 = Active low.</td><td>RW</td><td>0</td></tr>
<tr><td>8</td><td>INT_TEST</td><td>1 = The port continuously outputs an interrupt valid signal.
0 = The port continuously outputs an interrupt invalid signal.</td><td>RW</td><td>0</td></tr>
<tr><td>7:6</td><td>Reserved</td><td>Reserved</td><td>RW</td><td>0</td></tr>
<tr><td>5:4</td><td>LED_SEL[1:0]</td><td>Traditional LED function selection.
<table>
<tr><th>LED_
SEL</th><th>00</th><th>01</th><th>10</th><th>11</th></tr>
<tr><td>LED0</td><td>ACT_{AL}</td><td>$LINK_A$</td><td>$LINK_1$</td><td>$LINK_{10}$/</td></tr>
</table></td><td>RW</td><td>11b</td></tr>
</table>

<table>
<tr><td></td><td></td><td>
<table>
<tr><td></td><td>L</td><td>LL/ACT$_{ALL}$</td><td>0/ACT$_{ALL}$</td><td>ACT$_{10}$</td></tr>
<tr><td>LED1</td><td>LINK$_{100}$</td><td>LINK$_{100}$</td><td>LINK$_{100}$</td><td>LINK$_{100}$/ACT$_{100}$</td></tr>
<tr><td>LED2</td><td>Reserved</td><td>Reserved</td><td>Reserved</td><td>Reserved</td></tr>
</table>
Note 1: CH181HLED flicker judgment signal is an Ethernet carrier signal.
Note 2: The value of this LED_SEL[1] will change its default value because it is compatible with the latch values of different types of PHY pins. Where for CH182H1, the default value is 0.
Note 3: Only for CH182F8, when LED_SEL[1:0] is set to 11, the function of LED0 is LINK100/ACT100. As shown in the following table:
<table>
<tr><th>LED_SEL</th><th>00</th><th>01</th><th>10</th><th>11</th></tr>
<tr><td>LED0</td><td>ACT$_{ALL}$</td><td>LINK$_{ALL}$/ACT$_{ALL}$</td><td>LINK$_{10}$/ACT$_{ALL}$</td><td>LINK$_{100}$/ACT$_{100}$</td></tr>
</table>
</td><td></td><td></td></tr>
<tr><td>3</td><td>CUSTOMIZED_LED</td><td>Enable custom LED
1 = Enable custom LED function;
0 = Disable custom LED function.</td><td>RW</td><td>0</td></tr>
<tr><td>2</td><td>INT_ANC</td><td>Enable self-negotiation completion interrupt.
1 = Enable self-negotiation completion interrupt;
0 = Disable self-negotiation completion interrupt.</td><td>RW</td><td>0</td></tr>
<tr><td>1</td><td>INT_FHF</td><td>Enable BadSSD count half-full interrupt
1 = Enable BadSSD count to be half full to interrupt;
0 = Disable BadSSD count to be half full to interrupt。</td><td>RW</td><td>0</td></tr>
<tr><td>0</td><td>INT_RHF</td><td>Enable receive error count half-full interrupt
1 = Enable receive error count half-full interrupt;
0 = Disable receive error count half-full interrupt。</td><td>RW</td><td>0</td></tr>
</table>

5.10 Page 18 Register 26~Register 28 (For CH182D chips only)

Bit	Name	Description	Access	Default value
0x1A	MAC_PHY_ADDR0	Preset unique MAC address 0 (low order).	R0	X
0x1B	MAC_PHY_ADDR1	Preset unique MAC address 1.	R0	X
0x1C	MAC_PHY_ADDR2	Preset unique MAC address 0 (high order).	R0	X

6. Function Description

6.1 MII and Management Interface

6.1.1 Data Transfer

The Media Independent Interface MII provides a standard interface between the PHY and MAC layers. the MII operates at 25MHz or 2.5MHz frequency and supports 100Mbps and 10Mbps transmit and receive functions respectively.

Transmit:
MAC sends TXEN signal according to the transmit clock signal TXC provided by PHY and transfers the data into 4-bit parallel through TXD[3:0] to PHY. during TXEN enable, PHY will sample TXD[3:0] by TXC.
Receive:
PHY provides receive clock signal RXC, sends out RXDV signal, and converts the received data into 4-bit parallel via RXD[3:0] to MAC. crs_DV and COL signals are used for collision detection and processing. mac samples RXD[3:0] according to RXC.

6.1.2 Serial Management Interface SMI

MAC layer devices can use the MDC/MDIO management interface to control and configure PHY devices, and can control several different PHY chips by configuring the PHY address. The frame structure transmitted on the MDC/MDIO management interface is shown in the following table.

Table 6-1 Management frame format table

	Management frame fields							
	Preamble	Start	Operation	PHYAD	REGAD	TA	Data	Idle
Read	1…1	01	10	AAAAA	RRRRR	Z0	DDDDDDDDDDDDDDDD	Z
Write	1…1	01	01	AAAAA	RRRRR	10	DDDDDDDDDDDDDDDD	Z

Table 6-2 Serial management frame description table

Name	Description
Preamble	MAC transmits 32 consecutive 1s and 32 MDC clock signals on MDIO for PHY synchronization.
Start	The start character of the frame is defined as 01.
Operation	Operation code. Read: 10; Write: 01.
PHYAD	PHY address, 5 bits wide.
REGAD	Register address, 5 bits wide.
TA	The 2-bit steering character is used to avoid conflict during read operation. For read operation, during the 2-bit time of TA, the MAC controller keeps MDIO in high resistance state, while the PHY device keeps 1-bit high resistance state first and outputs 0 signal at the 2nd bit. During write operation, the MAC controller drives MDIO to output a 10 signal during this 2-bit time of TA, while the PHY maintains a high resistance state.
Data	16-bit data field.

Idle	The signal is in a high resistance state, and the pull-up resistor of PHY ensures that the MDIO line is at a pull-up high level.

Figure 6-1 Read cycle diagram

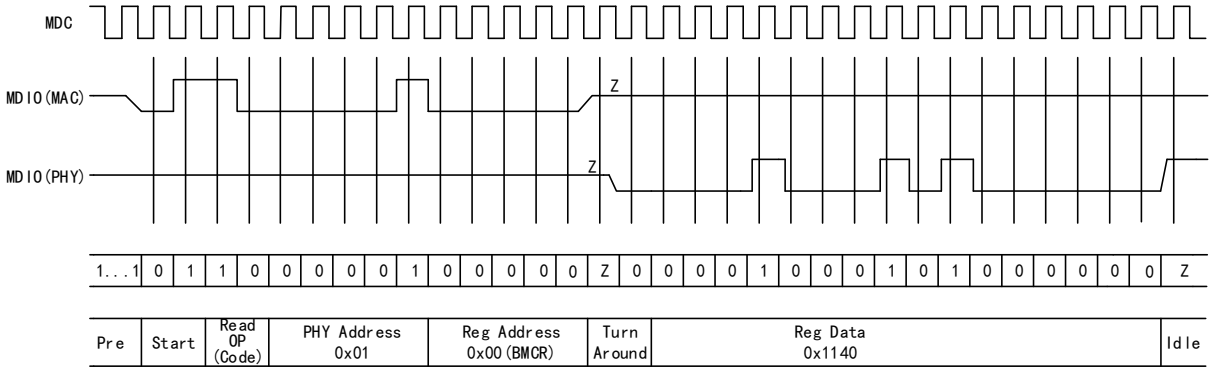
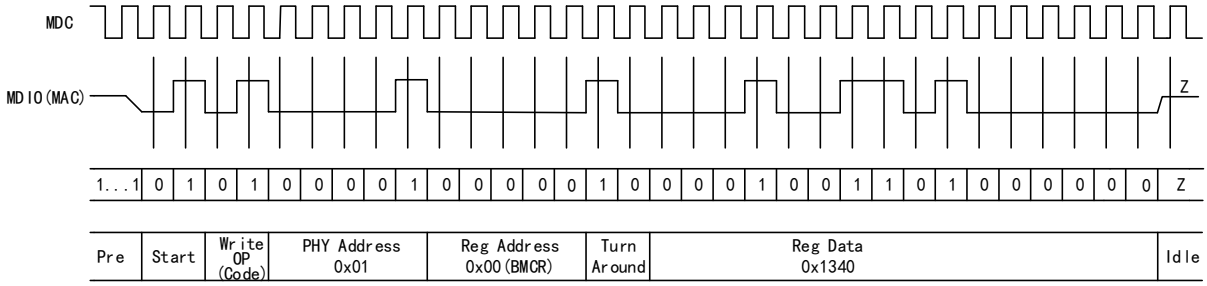


Figure 6-2 Write cycle diagram



6.2 Interrupt

When a corresponding state change is detected, PHY will output the interrupt pin INTB to a low level to generate an interrupt event. When the MAC receives the state change, it can access the interrupt source through MDC/MDIO interface.

Once the MAC reads the interrupt source through MDC/MDIO, the interrupt pin INTB will end low.

6.3 Auto-negotiation and Parallel Detection

CH182 supports IEEE802.3u protocol and is compatible with other Ethernet Transceiver supporting auto-negotiation. CH182 can automatically detect the network connection and determine the highest possible speed and duplex configuration between two devices. If the peer does not support auto-negotiation, CH182 will enter parallel detection mode and enable half-duplex mode. CH182 will send the fast link pulse FLP by default and wait for the peer response. If the FLP is received, the automatic negotiation process will continue. If normal link pulse NLP is received or a 100Mbps IDLE signal is received, CH182 will negotiate to 10Mbps half-duplex mode or 100Mbps half-duplex mode through parallel detection.

6.4 LED Function

6.4.1 LED and PHY Address

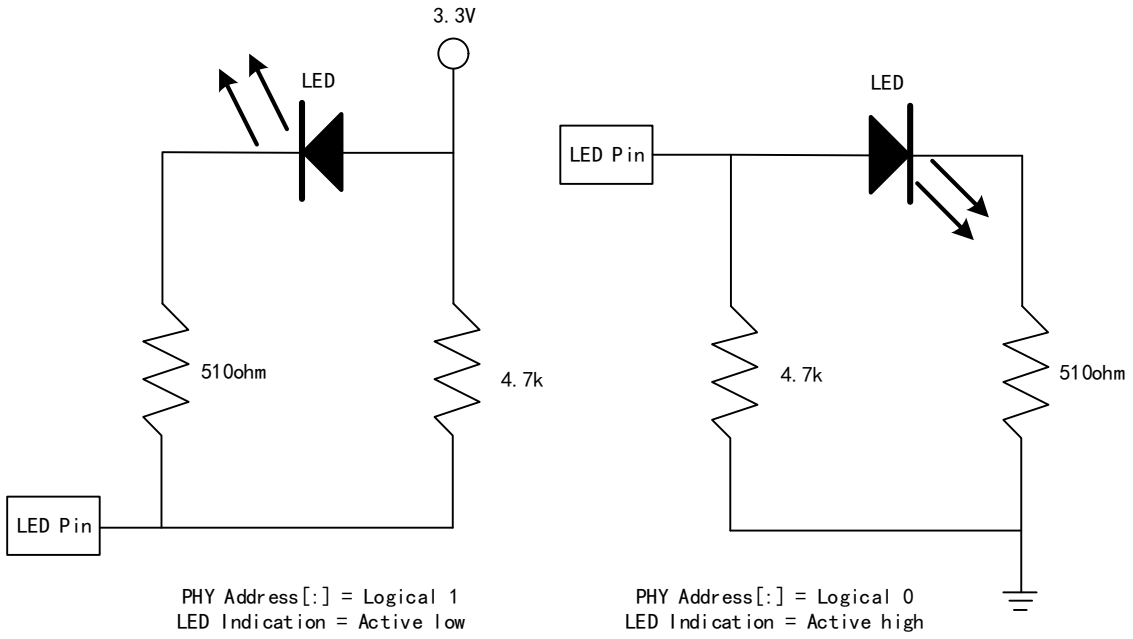
For CH182 and CH181 series chips, because some functions of PHY are related to the power-on latch state of LED

pins, the external combination of PHY function and LED usage must be considered to avoid conflicts. Specifically: When the default pull-up or pull-down state of the pin is used, the input level of the LED pin should be consistent with its default pull-up and pull-down level during power-on, and the 4.7KΩ resistor shown in Figure 6-3 below is not needed at this time.

When it is necessary to change the default pull-up or pull-down state of the pin, the input level of the LED pin should be opposite to its default pull-up and pull-down level during power-on. At this time, the 4.7KΩ resistor in Figure 6-3 below is used to change the level and cannot be omitted.

Taking CH182H2 chip as an example, when the default pull-up and pull-down state of LED pin is to be changed, the 4.7KΩ resistor cannot be omitted. As shown in Figure 6-3 below, if the PA1 pin of CH182H2 chip is externally connected with a pull-up resistor, the LED1 drive output is active at low level (left figure); If the PA0 pin is externally connected with a pull-down resistor, the LED0 drive output is active high (right figure). The PHY address configuration pin cannot be directly connected to GND or power supply, and must be pulled up or down by a 4.7K Ω resistor (3.9KΩ~5.6KΩ). If LED indication is not needed, the LED and its current limiting resistor (330Ω ~ 820Ω) can be removed.

Figure 6-3 Configuration diagram of LED and PHY address of CH182H2 chip



6.4.2 Link Monitor

The link monitor detects link integrity, such as LINK10, LINK100, LINK10/ACT, or LINK100/ACT. The specified link LED pin is driven to an active level whenever the link status is established; once the cable is disconnected, the link LED pin is driven to an inactive level, indicating that there is no network connection.

6.4.3 LED Indication

In 10/100M mode, the RX LED blinks to indicate that data is being received.

In 10/100M mode, the TX LED blinks to indicate that data is being sent.

In 10/100M mode, the TX/RX LED blinks to indicate that data is being sent or received.

In 10/100M mode, the LINK/ACTLED is always on to indicate that the connection is successful. When the LED

flashes, it indicates that a data packet is being received or sent.
The LED customization function is supported in 10/100M mode.

6.5 Shutdown Low-power Consumption Mode

Table 6-3 Low power mode configuration

Mode	Description
PWD	Set bit 11 of Register 0 to 1 to put PHY into shutdown mode PWD. In PWD mode, PHY will turn off all analog/digital functions except MDC/MDIO management interface. In PWD mode, MAC can wake up PHY via MDC/MDIO, note that PHY does not provide clock at this time.

6.6 10M/100M Transmit and Receive

6.6.1 100BASE-TX Transmit and Receive

100BASE-TX transmit:
The 4-bit data TXD[3:0] to be sent is encoded by 4B/5B and transmitted through the 25MHz TXC clock signal, which is sent to the linear driver output after parallel-serial conversion.

100BASE-TX receive:
The received signal is compensated by the adaptive equalizer, processed by the ADC module and DSP module, sent to the serial-parallel converter module, and then passed to the MII or RMII interface after 5B/4B decoding.

6.6.2 10BASE-T Transmit and Receive

10BASE-T transmit.
The 4-bit data TXD[3:0] to be sent is transmitted through the TXC signal at 2.5MHz, encoded, and fed to the 10M waveform generator to drive the output of the linear driver module.

10BASE-T receive.
The received signal is passed through the 10M receiver and the data is restored and passed to the MII or RMII interface.

6.7 Automatic Polarity Correction

Automatic correction of polarity errors for receive pairs in 10BASE-T mode and no consideration of polarity in 100BASE-TX mode. In 10BASE-T mode, polarity errors are corrected by detecting validly spaced link pulses. Detection starts with the MDI cross-detection phase and is locked when the 10BASE-T link is connected. The polarity state is unlocked when the link is disconnected.

6.8 Wake-on-LAN (WOL)

6.8.1 Magic Package and Wake-up Frame Format

When receiving a magic package or a wake-up event, for the CH182H1 chip, the MAC and the system can be woken up by interruption, and then the MAC and the system can be restored to normal state to deal with the subsequent work.

For CH182 and CH181 chips except CH182H1, a low level can be output through the power management event pin PMEB (where B stands for active low level), so as to wake up the MAC and the system and carry out the follow-up work. The PMEB pin needs to be pulled up to the power supply voltage through a resistor of 4.7KΩ, which is high by default.

All CH182 chips can monitor the magic package in the network, and only when the following conditions are met will the wake-up of the magic package be triggered:

- The destination address of the received magic packet is recognizable by the CH182. For example, with the device MAC address as the destination address;
- The received magic packet does not contain CRC errors;
- Magic packet pattern match. For example, any part of the packet contains: 6*0xFF+16*DMAC (destination MAC).

Except CH182H and CH181H chips, other CH182 chips can monitor wake-up frames in the network. Wake-up frame events only occur when the following conditions are met:

- The destination address of the received wake-up frame is recognizable by the CH182, e.g., with the device MAC address as the destination address;
- The received wake-up frame does not contain CRC errors;
- The 16-bit CRC of the received wake-up frame matches the 16-bit CRC sample of the local wake-up frame, which can also be configured to allow direct group wake-up.

6.8.2 Wake-on-LAN with Low Level Output

When PHY receives a wake-up frame or magic packet from the opposite end, for CH182H1 chip, it can output an active low level through the INTB pin, so that the MAC and the system can wake up after recognizing the low level. For CH182 and CH181 chips except CH182H1, the low level can be output through PMEB pin, and the MAC or system will wake up after recognizing the low level. The PMEB pin is set by the system or MAC to restore high level.

6.8.3 Wake-on-LAN with Low Level Pulse Output

When PHY receives a wake-up frame or magic packet from the opposite end, for CH182H1 chip, it can output an active low level through the INTB pin, so that the MAC and the system can wake up after recognizing the low level. For CH182 and CH181 chips except CH182H1, the low-level pulse can be output through the PMEB pin, and the MAC or system will wake up after recognizing the low level. The PMEB pin is set by the system or MAC to restore high level.

6.8.4 Wake-on-LAN Pin Type (MII mode)

Name	Type	Normal			Enable WOL
		100M	10M	Idle	
TXC	O/PD	25MHz output	2.5MHz output	25MHz output	O（2.5M/25M）/L/PD(1)
TXEN	I/PD	I	I	I	I/PD
TXD[3:0]	I/PD	I	I	I	I/PD
RXC	O/PD	25MHz output	2.5MHz output	25MHz output	O（2.5M/25M）/L/PD(2)
COL	O/PD	O	O	O	O/L/PD(3)
CRS_DV	O/PD	O	O	O	O/L/PD(3)
RXDV	O/PD	O	O	O	O/L/PD(3)
RXD[0]	O/PD	O	O	O	O/L/PD(3)
RXD[1]	O/PD	O	O	O	O/L/PD(3)
RXD[2]	LI/O/PD	O	O	O	O/L/PD(3)
RXD[3]	O/PD	O	O	O	O/L/PD(3)
RXER	O/PD	O	O	O	O/L/PD(3)
MDC	I/PU	I	I	I	I/PU
MDIO	IO/PU	IO	IO	IO	IO/PU

Note 1: Setting Isolate = 1 (register 0 bit 10) will suspend TXC with pin type L.

Note 2: Setting Isolate = 1 (register 0 bit 10) will suspend RXC with pin type L.

Note 3: Setting Isolate = 1 (register 0 bit 10) will suspend RX all interface signals with pin type L.

6.8.5 Wake-on-LAN Pin Type (RMII mode)

Name	Type	Normal			Enable WOL
		100M	10M	Idle	
TXC (REFCLK)[4]	IO/PD	50MHz Input/output	50MHz Input/output	50MHz Input/output	I/O (50M)(4)
TXEN	I/PD	I	I	I	I/PD
TXD[0:1]	I/PD	I	I	I	I/PD
CRS_DV	O/PD	O	O	O	O/L/PD(3)
RXD[0]	LI/O/PD	O	O	O	O/L/PD(3)
RXD[1]	O/PD	O	O	O	O/L/PD(3)
RXER	O/PD	O	O	O	O/L/PD(3)
MDC	I/PU	I	I	I	I/PU
MDIO	IO/PU	IO	IO	IO	IO/PU

Note 3: Setting Isolate = 1 (register 0 bit 10) will suspend RX all interface signals with pin type L.

Note 4: Setting Isolate = 1 (register 0 bit 10) will suspend TXC with pin type L;

If TXC/REFCLK is in input mode (MAC to PHY), then REFCLK cannot be suspended while WOL is enabled; if TXC/REFCLK is in output mode (PHY to MAC), then REFCLK is not recommended to be suspended;

7. Electrical Characteristics

7.1 Absolute Maximum Value

(Critical or exceeding the absolute maximum value will likely cause the chip to work improperly or even be damaged)

Table 7-1 Absolute maximum parameter table

Symbol	Parameter		Min.	Max.	Unit
AVDD33	AVDD33 or VDD33 supply voltage		-0.4	4.0	V
*VDDK	Internal power supply decoupling terminal voltage		-0.2	1.5	V
VDDIO	Interface I/O pin supply voltage		-0.4	4.0	V
V_{IO}	Control the voltage on the interface pins (VIO power)		-0.4	VIO+0.4	V
V_{IOX}	Voltage on Ethernet pins (AVDD33 power supply)		-0.4	AVDD33+0.4	V
T_s	Storage temperature range		-65	150	℃
T_J	Junction temperature range		-40	125	℃
T_A	Ambient temperature	CH182	-40	85	℃
		CH181H	-10	70	

7.2 Operating Voltage and DC Characteristics

Table 7-2 DC Characteristics Parameter Table (AVDD33=3.3V，VIO=3.3V，TA=25℃)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
AVDD33	AVDD33 or VDD33 supply voltage	AVDD33 pin	3.2	3.3	3.45	V
VDDIO	Interface I/O pin supply voltage	CH182H, CH181H	3.1	3.3	3.5	V
		Other CH182	1.7	3.3	3.5	V
V_{IL}	Input low voltage	VDDIO = 3.3V	0	-	0.8	V
		VDDIO = 1.8V	0	-	0.6	V
V_{IH}	Input high voltage	VDDIO = 3.3V	2.0	-	VIO	V
		VDDIO = 1.8V	1.2	-	VIO	V
I_{IL}	Input low leakage current	Input voltage 0V	-5		5	uA
I_{IH}	Input high leakage current	Input voltage VIO	-5		5	uA
V_{OL}	Output low voltage	IOL = 8mA	-	-	0.4	V
V_{OH}	Output high voltage	IOH = -8mA	VIO-0.4	-	-	V
Rpu	Resistance value of the built-in pull-up resistor		35	60	100	KΩ
Rpd	Resistance value of the built-in pull-down resistor		35	60	100	KΩ
Rpumdio	Resistance value of MDIO built-in pull-up resistor	Open by default		1.5		KΩ

V_{LVR}	AVDD33 or VDD33 voltage threshold for power supply low voltage reset		2.7	2.9	3.1	V

7.3 Supply Current Characteristics

Table 7-3 Current consumption Table (AVDD33=3.3V，VIO=3.3V，T_A=25℃)

Symbol	Parameter	Condition (All current, including network transformer)	Typ.		Unit
			MII mode	RMII mode	
I_{DD}	Supply current in transmission state	The link of 100BASE-TX path is successful and there are packets on the transceiver channel.	60.0	60.4	mA
		The link of 10BASE-TX path is successful and there are packets on the transceiver channel.	28.8	34.2	
	Supply current in idle state	The link of 100BASE-TX path is successful and there are no data packets on the transceiver channel.	61.2	61.4	mA
		The link of 10BASE-TX path is successful and there are no data packets on the transceiver channel.	25.8	28.1	
	Supply current in disconnected state	100BASE-TX and 10BASE-TX paths are not linked and PHY is in auto-negotiation state.。	38.5	38.4	mA
	Supply current in shutdown state	Only SMI interface is working.	0.2	0.2	

7.4 Power-on Timing

Figure 7-1 Power-on timing diagram

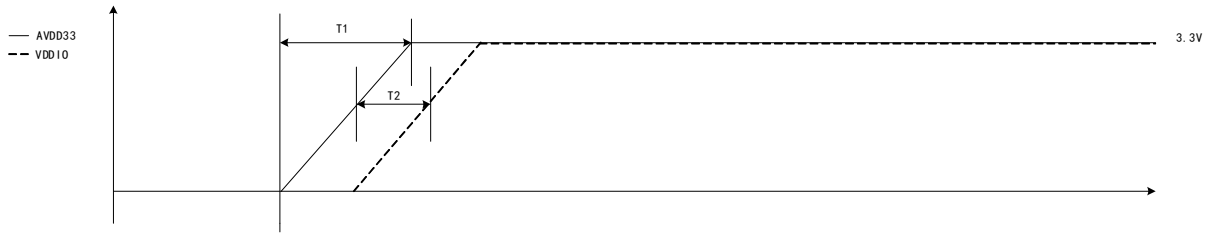


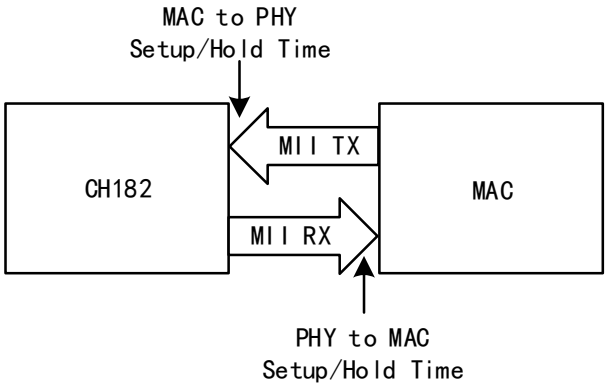
Table 7-4 Power-on timing table

Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	Voltage rise time when AVDD33 is powered on	1		10000	us
T2	Delay time of VDDIO power supply relative to AVDD33 power supply	0	0	1	ms
Tpor	Power-on reset time of PHY chip (PHY accessible thereafter)	6.4	8.5	10.5	ms

Trst	Reset time after RSTB low pulse (PHY accessible thereafter)	10			ms

7.5 MII Transmit Cycle Timing

Figure 7-2 MII interface setting/holding time diagram



The packet sending process from MAC to PHY on the MII interface is as follows:

Figure 7-3 Timing diagram of MII transmit cycle

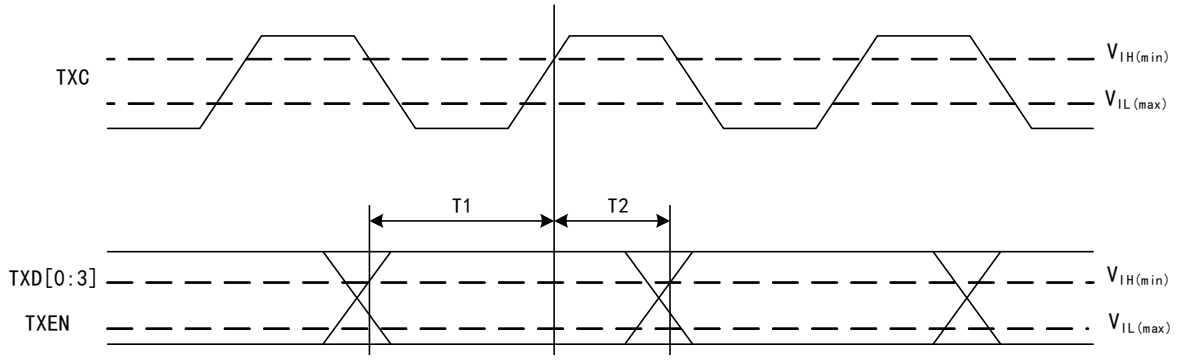


Table 7-5 MII transmission cycle timing table

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
T1	TXEN, TXD[0:3] build to TXC rising edge	100Mbps	7			ns
		10Mbps	5			ns
T2	TXEN, TXD[0:3] is held after the rising edge of TXC	100Mbps	0			ns
		10Mbps	0			ns

7.6 MII Receive Cycle Timing

The packet sending process from PHY to MAC on MII interface is as follows.

Figure 7-4 Timing diagram of MII receive cycle

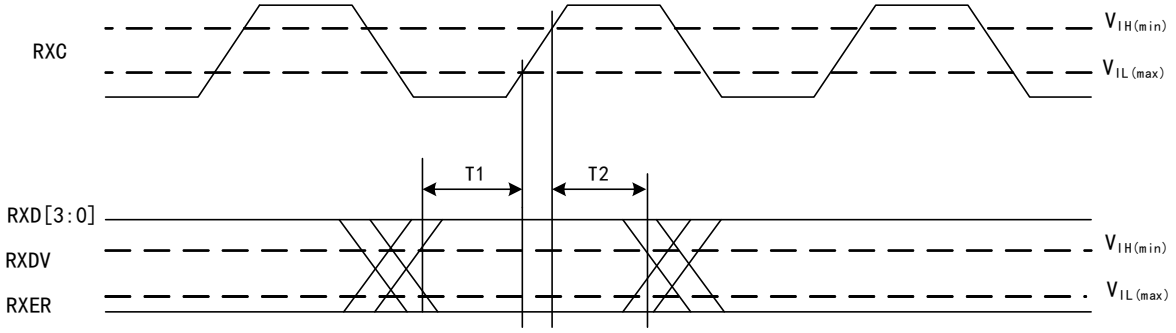


Table 7-6 MII reception cycle timing table

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
T1	RXER, RXDV, RXD[0:3] established to RXC rising edge	100Mbps	5			ns
		10Mbps	5			ns
T2	RXER, RXDV, RXD[0:3] are held after the rising edge of RXC	100Mbps	10			ns
		10Mbps	10			ns

7.7 RMII Transmit and Receive Cycle Timing

Figure 7-5 Schematic diagram of RMII interface settings, hold time and output delay time

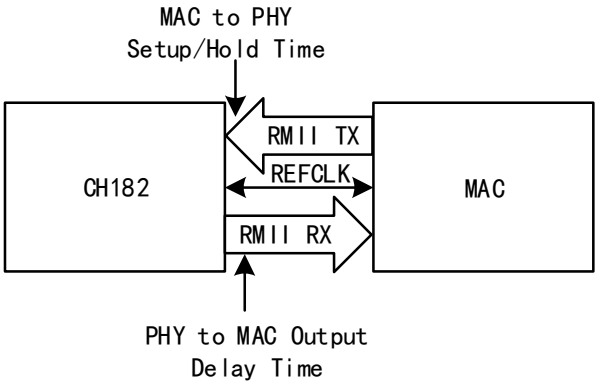


Figure 7-6 Timing diagram of RMII transmit and receive cycles

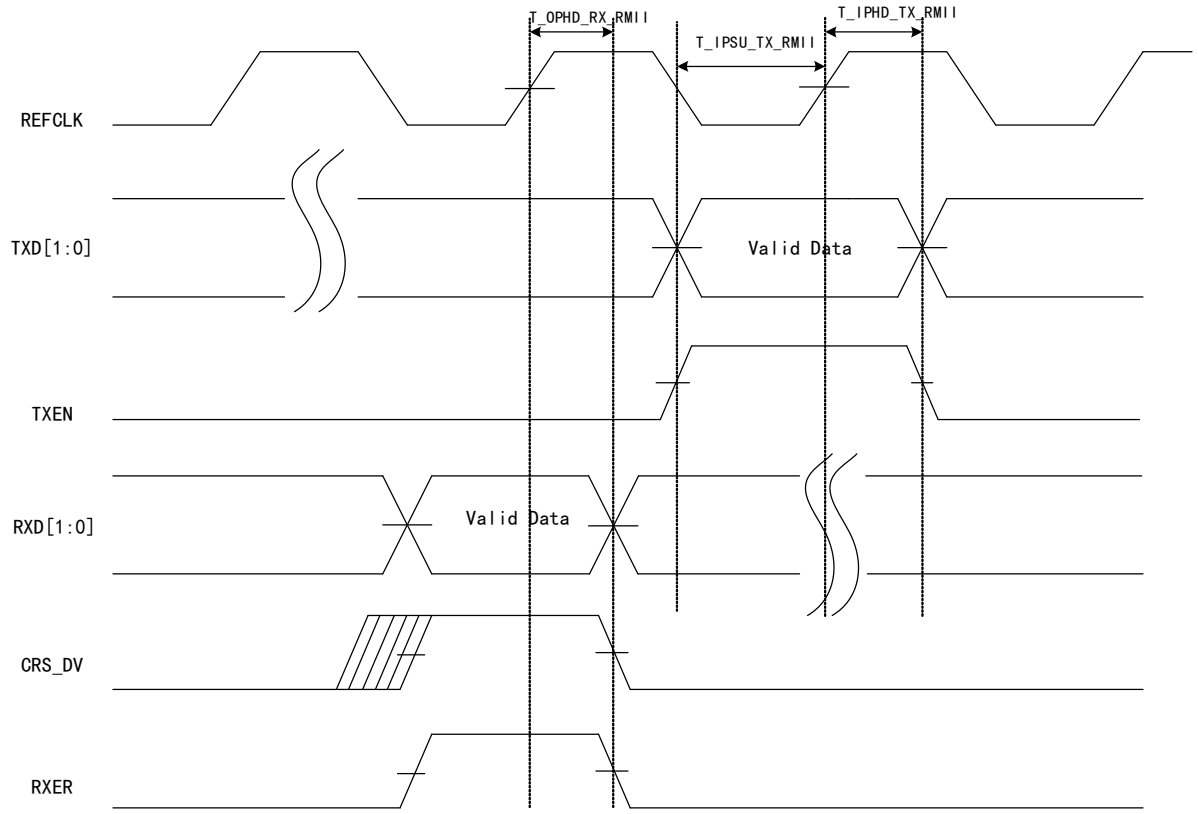


Table 7-7 Timing table of RMII transmission and reception cycles

Symbol	Parameter	Condition	Min.	Typ.	Max.
REFCLK Frequency	Reference clock frequency		50		MHz
REFCLK Duty Cycle	Duty cycle of the reference clock	40		60	%
T_IPSU_TX_RMII	TXD[1:0]/TXEN build time to REFCLK	5			ns
T_IPHD_TX_RMII	TXD[1:0]/TXEN hold time from REFCLK	2			ns
T_OPHD_RX_RMII	RXD[1:0]/CRS_DV/RXER delay time from REFCLK output	2			ns

Note:1. RMII TX timing can be adjusted by 16 bits [11:8] of page 7 register, adjustable resolution is about 1.5ns, default value is recommended;

2. RMII RX timing can be adjusted by page 7 register 16 bits [7:4], adjustable resolution is about 1.5ns, we suggest using the default value.

7.8 MDC/MDIO Timing

Figure 7-7 MDC/MDIO interface settings, hold time and effective time from MDC rising edge

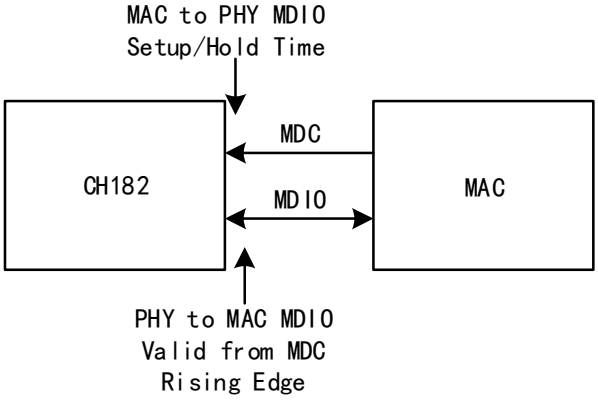


Figure 7-8 MDC/MDIO timing

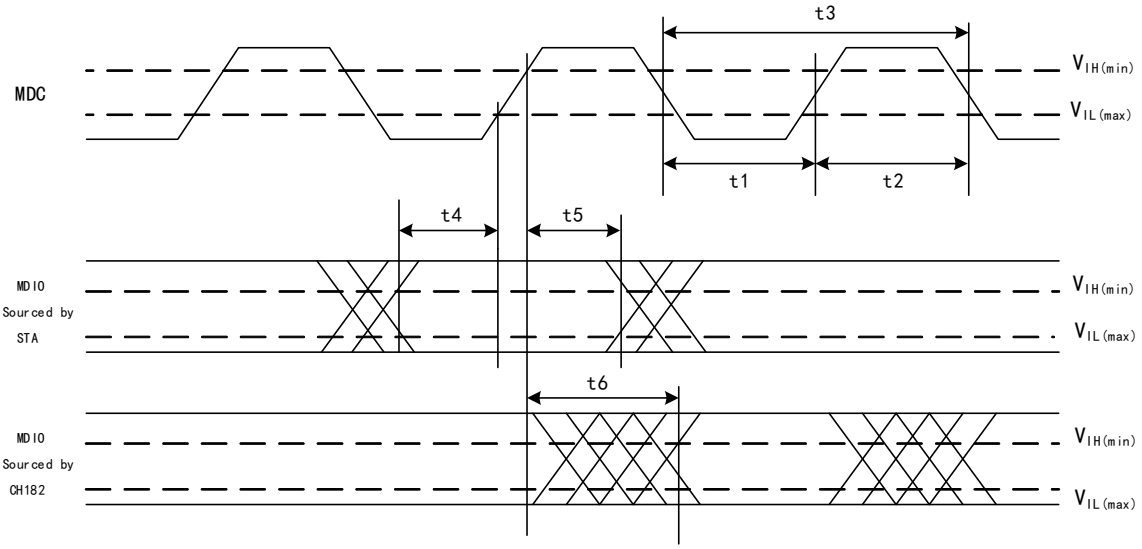


Table 7-8 MDC/MDIO timing table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t1	MDC high pulse width	100			ns
t2	MDC low pulse width	100			ns
t3	MDC cycle	200			ns
t4	MDIO build to MDC rising edge	10			ns
t5	MDIO hold time from the rising edge of MDC	10			ns
t6	MDIO on the rising edge of MDC is valid	0	180		ns

7.9 Crystal Oscillator/clock Characteristics

Table 7-9 Crystal oscillator/clock characteristics table

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
TCKF	Crystal frequency	Recommended no more than 20ppm	24.999	25	25.001	MHz
TPWH	OSC high pulse width	-	15	20	25	ns

TPWL	OSC low pulse width	-	15	20	25	ns

Note: The XI and XO pins already have the two oscillation capacitors required for an external crystal with a load capacitance of 12pF respectively, and only the crystal is required externally.

If an external crystal with a load capacitance of 20pF is selected, then XI and XO need to add an additional 15pF oscillation capacitor to ground respectively.

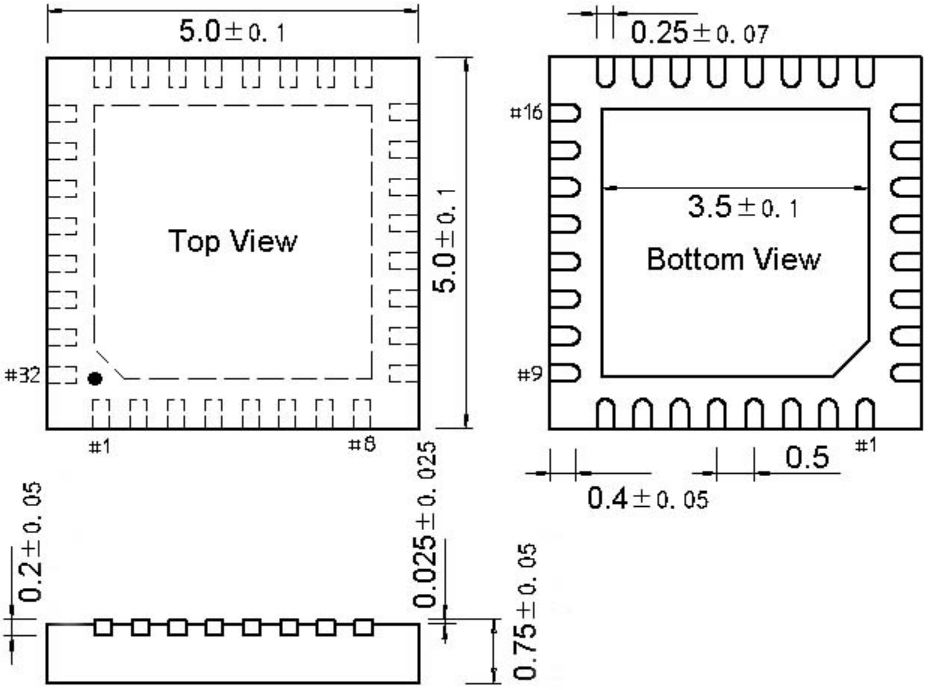
When the XI is connected to GND, it can support 25MHz or 50MHz external clock input from the XO pin.

8. Package Information

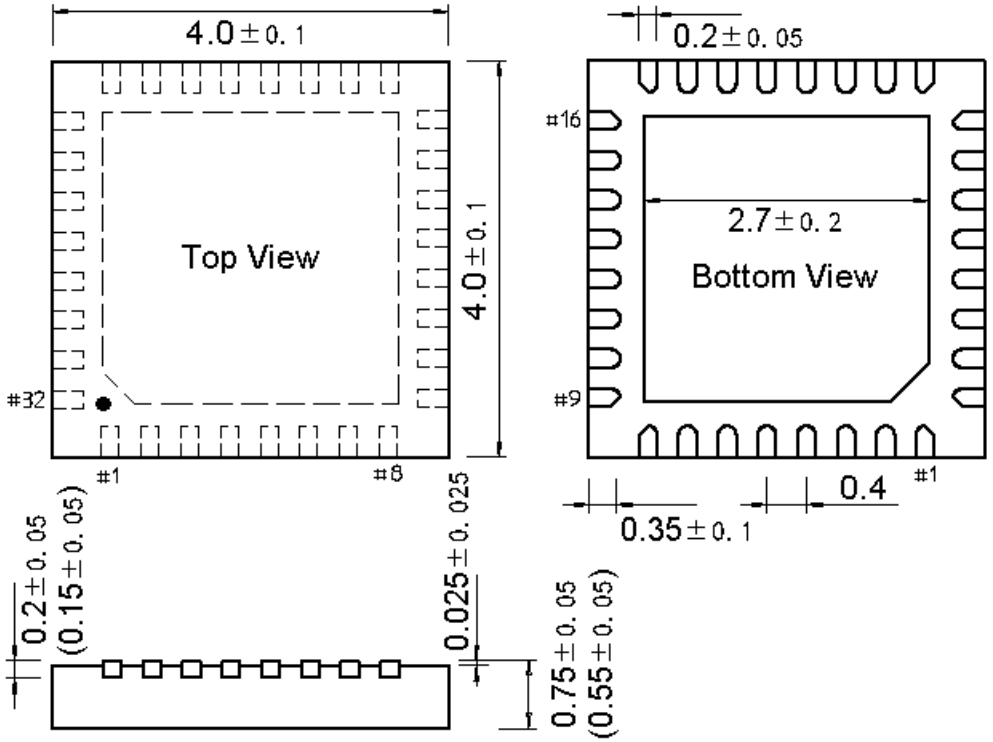
Note: The unit of dimensioning is mm (millimeter).

The pin center spacing is the nominal value without error, and the dimensional error other than that is no more than ±0.2mm.

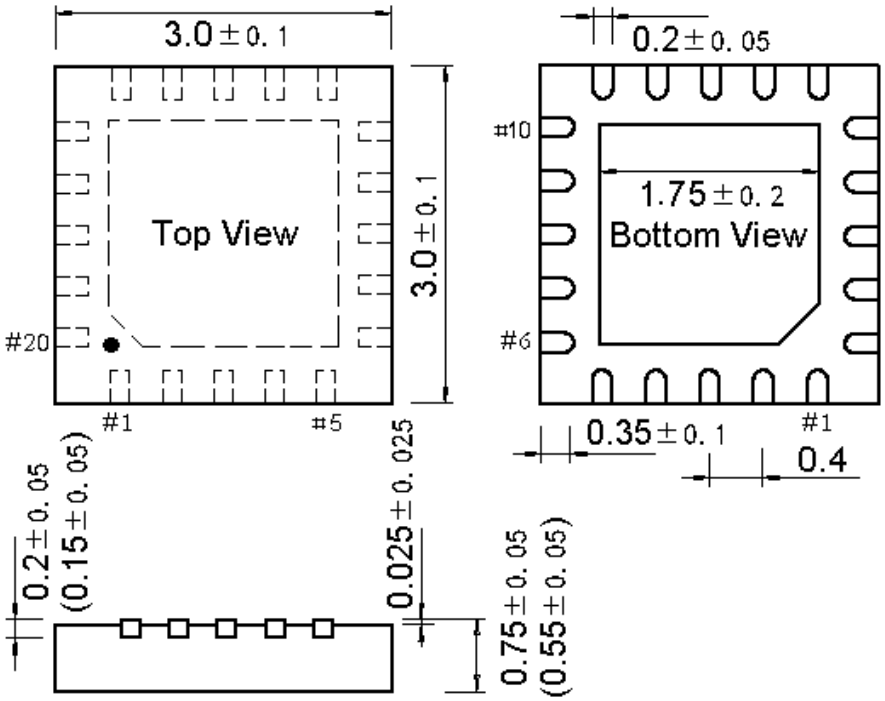
8.1 QFN32X5 Package



8.2 QFN32 Package

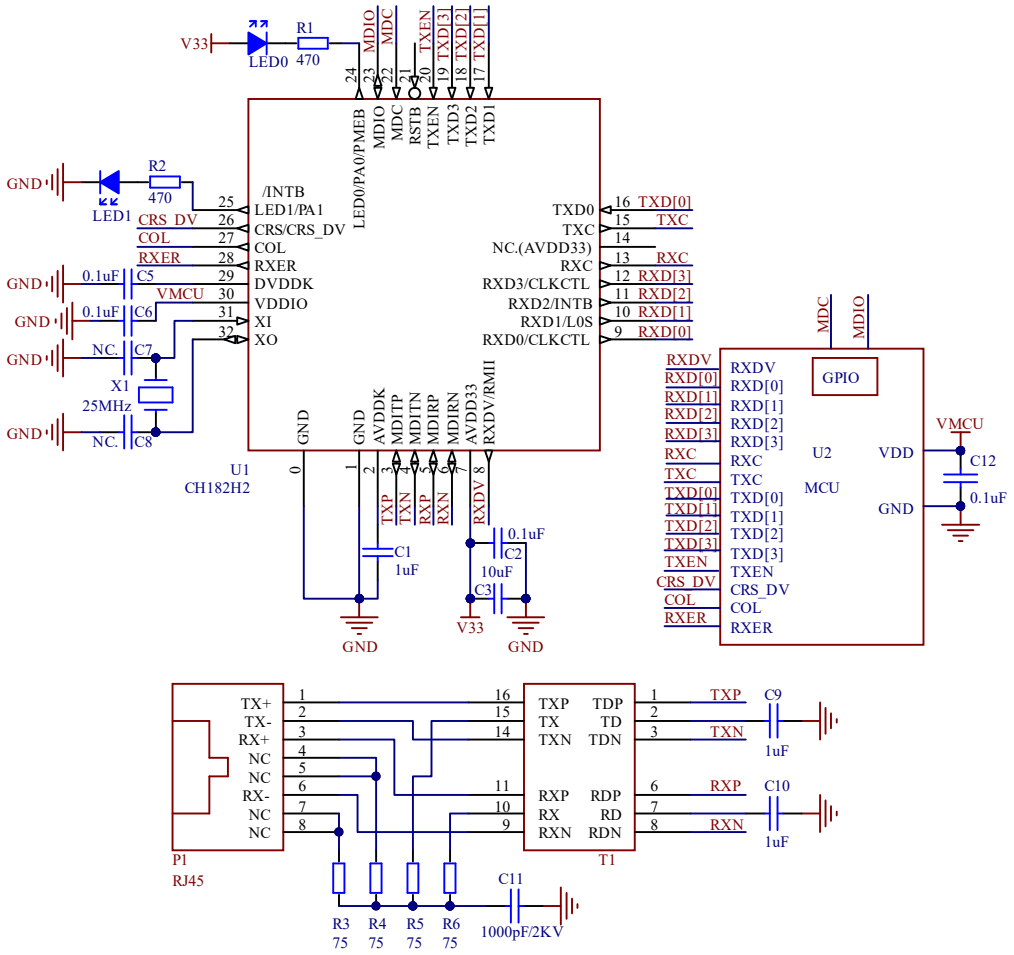


8.3 QFN20 Package



9. Application

9.1 MII Interface Application



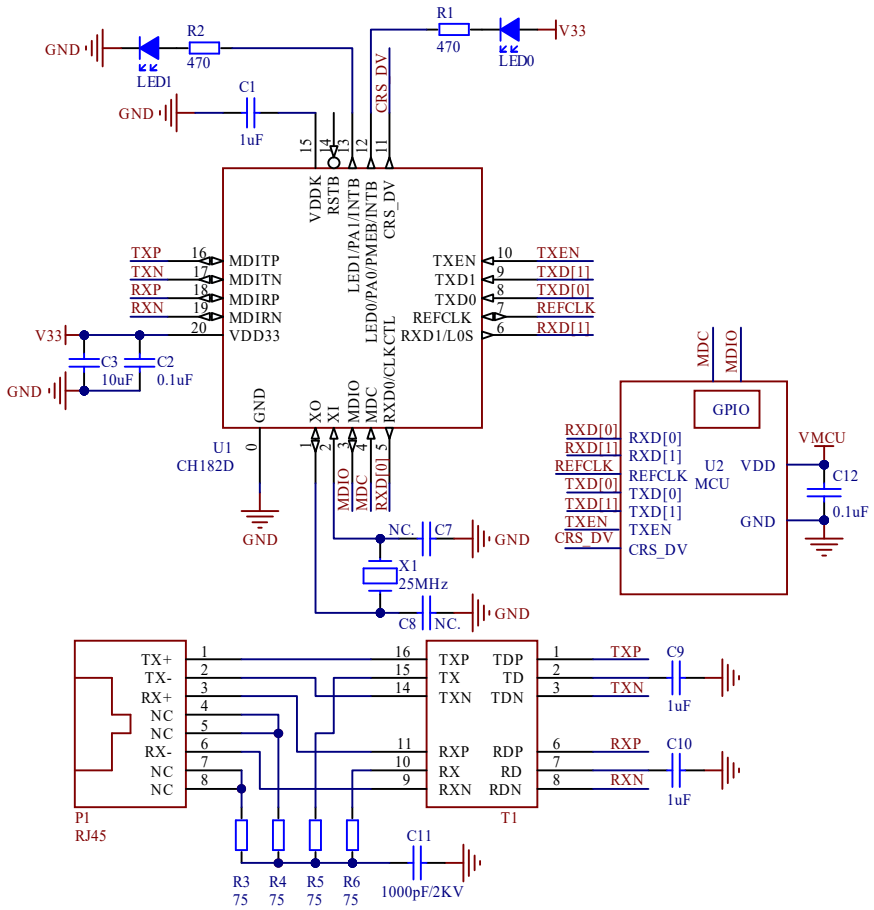
CH182 has built-in part of the oscillation capacitance of crystal X1, and C7 and C8 can be adjusted according to the crystal parameters. For X1 with a load capacitance of 12pF, C7 and C8 are not required; for X1 with a load capacitance of 20pF, C7 and C8 are recommended to be 15pF each.

T1 is an Ethernet network transformer. Its center tap is grounded through capacitor C9/C10 respectively. Do not connect it to any power supply.

CH182 has a built-in Ethernet 50Ω impedance matching resistor. Do not connect an external 49.9Ω or 50Ω resistor, which is equivalent to voltage drive.

CH182 supports Ethernet applications that require no network transformer and capacitor isolation.

9.2 RMII Interface Application



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CH182 supports Ethernet applications that require no network transformer and capacitor isolation.