## Overview

CH32L103 is an industrial-grade low-power general-purpose microcontroller designed based on QingKe RISC-V core.CH32L103 built-in USB and PD PHY, support PDUSB, including USB Host and USB Device functions, USB PD and Type-C fast charging function, built-in low-power timer, provides 1 OPA, 3 CMPs, 4 USARTs, 2 I2Cs, 2 SPIs, 1 CAN, multiple timers, 12-bit ADC, 10-channel touch-key, etc.

## Features

- **Core**
  - QingKe 32-bit RISC-V4C core
  - Support RV32IMAC instruction set and self-extending instructions
  - Fast programmable interrupt controller + hardware interrupt stack
  - Branch prediction, conflict handling mechanism
  - Single-cycle multiplication, hardware division
  - System frequency 96MHz
- **Memory**
  - 20KB volatile data storage area SRAM
  - 64KB program memory area CodeFlash
  - 3328B System BootLoader storage area
  - 256B system non-volatile configuration information memory area
  - 256B user-defined information storage area
- **Power management and low-power:**
  - System power supply $V_{DD}$: 3.3V
  - Low-power modes: Sleep, Stop, Standby
  - $V_{BAT}$ independently powers RTC and backup registers
- **Clock & Reset**
  - Built-in factory-tuned 8MHz RC oscillator
  - Built-in RC oscillator of about 40KHz.
  - Built-in PLL, optional CPU clock up to 96MHz.
  - External support high-speed oscillator 3 ~ 25MHz.
  - External support 32.768KHz low-speed oscillator
  - Power-on/down reset, programmable voltage monitor
- **RTC: 32-bit independent timer**
- **8-channel general-purpose DMA controller**
  - 8 channels, support ring buffer management
  - Support TIMx/ADC/USART/I2C/SPI
- **3-group analog voltage comparator CMP:**
  - 2 input channels each, optional common reference voltage pin
  - Output to I/O or internal direct trigger TIM2
- **1-group OPA/PGA/voltage comparator:**
  - Multiple input channels, selectable multi-step gain
  - Multiple output channels, optional ADC pins
- **12-bit ADC**
  - Analogue input range: $V_{SSA} \sim V_{DDA}$
  - 10-channel external signal + 3-channel internal signal channel
  - On-chip temperature sensor
- **10-channel touch-key detection**
- **16-bit low-power timer**
- **Multiple timers**
  - 1×16-bit advanced-control timers, with dead zone control and emergency brake; can offer PWM complementary output for motor control
  - 2×16-bit general-purpose timers, provide input capture/output comparison/PWM
  - 1×32-bit general-purpose timer
  - 2 watchdog timers (independent watchdog and window watchdog)
  - SysTick: 64-bit counter
- **4-group UART: Support LIN and ISO7816**
- **2 I2C interface: Support SMBus/PMBus**
- **2 SPI interface**
- **1 CAN interface (2.0B active):**
  - Support CAN FD protocol
- **USB 2.0 full-speed controller and PHY:**
  - Support USB Host and USB Device

- **USB PD and Type C controller and PHY:**
- Support DRP, Sink and Source
- Support PDUSB
- **Fast GPIO port**
- 37 I/O ports, support 16 external interrupts

- **Security features: Chip unique ID**
- **Debug mode: 2-wire serial debug interface (SDI)**
- **Package: LQFP, QFN, QSOP, TSSOP**

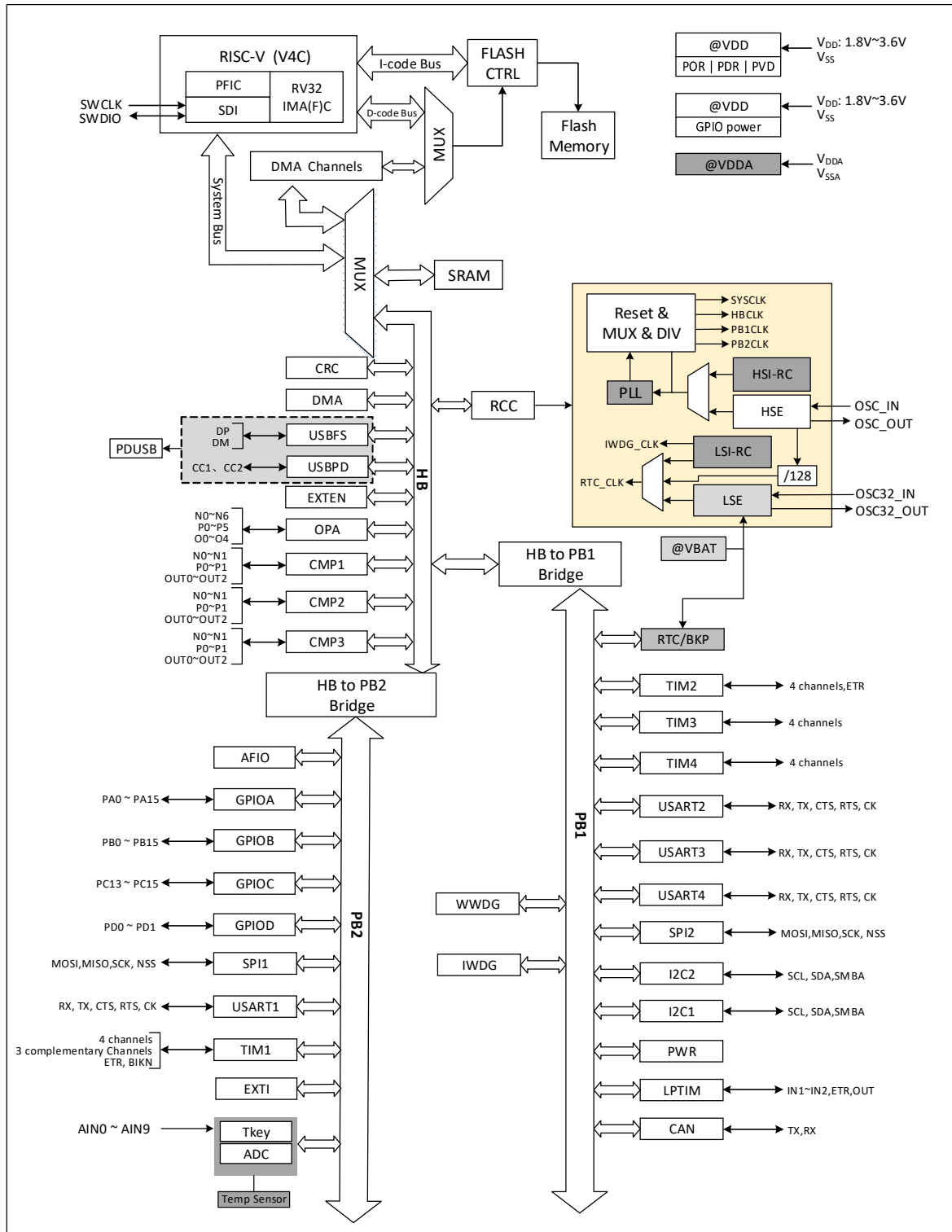| Resource / Model | | C8T6 | K8U6 | G8R6 | F8U6 | F8P6 |
|---|---|---|---|---|---|---|
| Pin Number | | 48 | 32 | 28 | 20 | 20 |
| FLASH (byte) | | 64K | 64K | 64K | 64K | 64K |
| SRAM (byte) | | 20K | 20K | 20K | 20K | 20K |
| GPIO port number | | 37 | 31 | 26 | 19 | 16 |
| Timer | Advanced-control TIM1 (16-bit) | 1 | 1 | 1 | 1 | 1 |
| | General-purpose TIM2, TIM3 (16-bit) | 2 | 2 | 2 | 2 | 2 |
| | General-purpose TIM4 (32-bit) | 1 | 1 | 1 | 1 | 1 |
| | Low-power timer (LPTIM) | √ | √ | √ | √ | √ |
| | Watchdog | 2 ( WWDG + IWDG ) | | | | |
| | SysTick (64-bit) | √ | | | | |
| RTC | | √ | | | | |
| ADC | | 10+3 | 10+3 | 10+3 | 10+3 | 9+3 |
| Tkey | | 10-channel | 10-channel | 10-channel | 10-channel | 9-channel |
| OPA | | 1 | 1 | 1 | 1 | 1 |
| CMP | | 3 | 3 | 3 | 3 | CMP1 CMP2 |
| Communication interface | USART | 4 | 4 | 4 | 4 | 4 |
| | SPI | 2 | SPI1 | 2 | 2 | SPI1 |
| | I2C | 2 | I2C1 | 2 | 2 | I2C1 |
| | CAN | 1 | 1 | 1 | 1 | 1 |
| | Host Device — USB Host Device | Host Device | Host Device | Host Device | Host Device | Device |
| | Host Device — USB PD Type-C | DRP Source Sink | DRP Source Sink Built-in Rd[1] | DRP Source Sink | DRP Source Sink Built-in Rd[1] | DRP Source Sink |
| CPU main frequency | | Max: 96MHz | | | | |
| Rated voltage | | 3.3V | | | | |
| Operating temperature | | Industrial-grade: -40°C~85°C | | | | |
| Package form | | LQFP48 | QFN32 | QSOP28 | QFN20 | TSSOP20 |
| Main applications and features | | General-purpose, Pin compatible | General-purpose. Pin optimized | General-purpose. Motor master | Motor master Pin optimized | General-purpose, Pin compatible |

*Note: 1. CH32L103K8U6 and F8U6 have built-in type-C specification-defined controllable Rd pull-down resistors of about 5.1kΩ.*

# Chapter 1 Specification Information

## 1.1 System Structure

The microcontroller is designed on the basis of the RISC-V instruction set, and its architecture integrates QingKe microprocessor core, arbitration unit, DMA module, SRAM storage and other components through multiple bus groups to achieve interaction. A general-purpose DMA controller is integrated to reduce the CPU load and improve access efficiency, and a multi-level clock management mechanism is applied to reduce the power consumption of peripherals. The following diagram shows the overall internal architecture of the series chip.
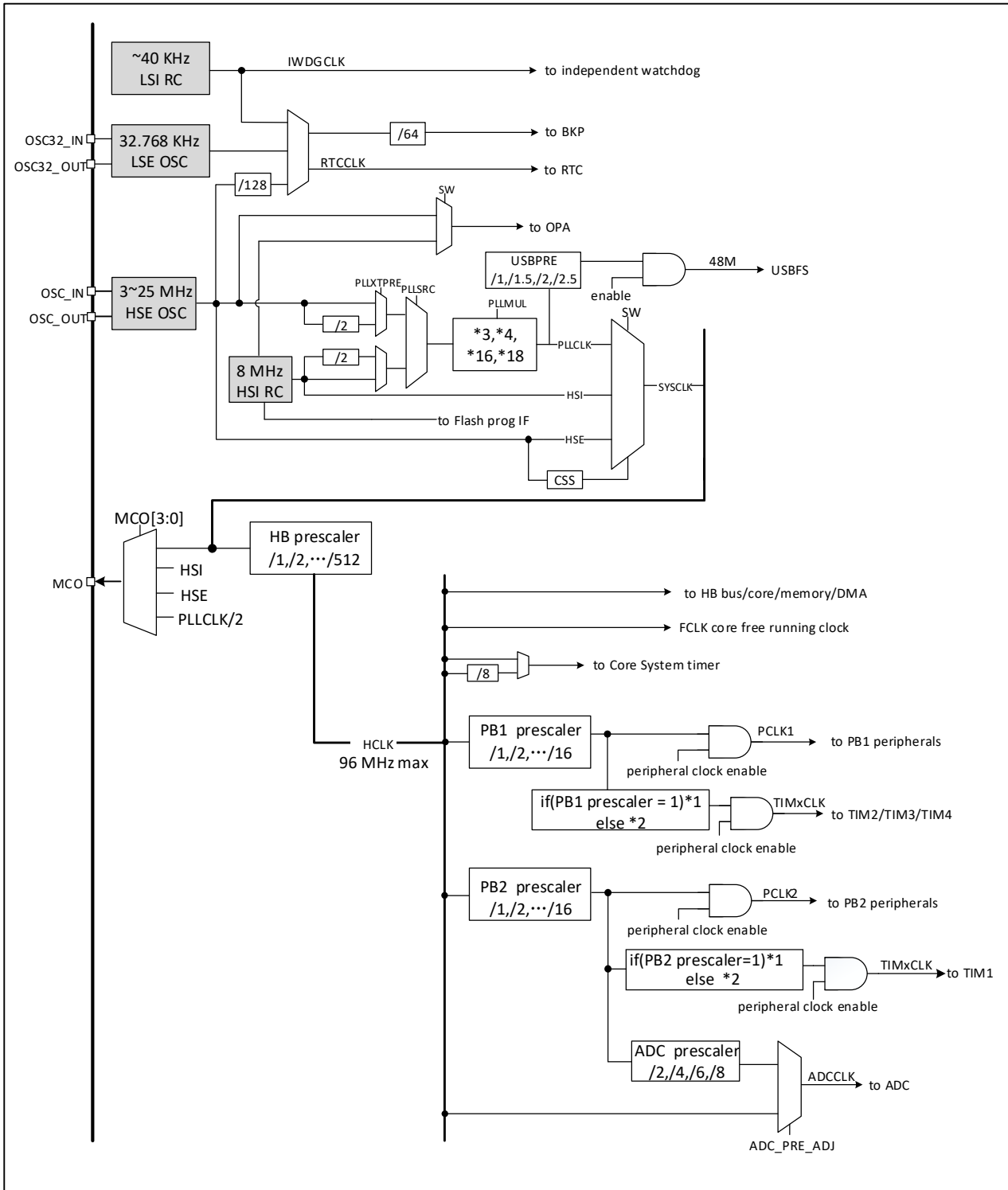
Figure 1-1 System Block Diagram

## 1.2 Memory Map

Figure 1-2 Memory address map

| Address | Region |
|---|---|
| 0x5000 0000 | USBFS |
| 0x4002 7400 | Reserved |
| 0x4002 7000 | USBPD |
| 0x4002 6400 | Reserved |
| 0x4002 6000 | OPA/CMP |
| 0x4002 3C00 | Reserved |
| 0x4002 3800 | EXTEN |
| 0x4002 3400 | Reserved |
| 0x4002 3000 | CRC |
| 0x4002 2400 | Reserved |
| 0x4002 2000 | Flash Interface |
| 0x4002 1400 | Reserved |
| 0x4002 1000 | RCC |
| 0x4002 0400 | Reserved |
| 0x4002 0000 | DMA |
| 0x4001 3C00 | Reserved |
| 0x4001 3800 | USART1 |
| 0x4001 3400 | Reserved |
| 0x4001 3000 | SPI1 |
| 0x4001 2C00 | TIM1 |
| 0x4001 2800 | Reserved |
| 0x4001 2400 | ADC/TouchKey |
| 0x4001 1800 | Reserved |
| 0x4001 1400 | Port D |
| 0x4001 1000 | Port C |
| 0x4001 0C00 | Port B |
| 0x4001 0800 | Port A |
| 0x4001 0400 | EXTI |
| 0x4001 0000 | AFIO |
| 0x4000 7D00 | Reserved |
| 0x4000 7C00 | LPTIM |
| 0x4000 7000 | PWR |
| 0x4000 6C00 | BKP |
| 0x4000 6800 | Reserved |
| 0x4000 6400 | CAN |
| 0x4000 5C00 | Reserved |
| 0x4000 5800 | I2C2 |
| 0x4000 5400 | I2C1 |
| 0x4000 5000 | Reserved |
| 0x4000 4C00 | USART4 |
| 0x4000 4800 | USART3 |
| 0x4000 4400 | USART2 |
| 0x4000 3C00 | Reserved |
| 0x4000 3800 | SPI2 |
| 0x4000 3400 | Reserved |
| 0x4000 3000 | IWDG |
| 0x4000 2C00 | WWDG |
| 0x4000 2800 | RTC |
| 0x4000 0C00 | Reserved |
| 0x4000 0800 | TIM4 |
| 0x4000 0400 | TIM3 |
| 0x4000 0000 | TIM2 |

4G linear address space:

| Address | Region |
|---|---|
| 0xFFFF FFFF | Reserved |
| 0xE010 0000 | Core Private Peripherals |
| 0xE000 0000 | Reserved |
| 0xC000 0000 | Reserved |
| 0x8000 0000 | Reserved |
| 0x5000 0400 | Peripherals |
| 0x4000 0000 | Reserved |
| 0x2000 5000 | 20K SRAM |
| 0x2000 0000 | FLASH |
| 0x0000 0000 | |

Code/System FLASH region:

| Address | Region |
|---|---|
| 0x1FFF FFFF | Reserved |
| 0x1FFF F900 | Option Bytes |
| 0x1FFF F800 | Vendor Bytes |
| 0x1FFF F700 | Reserved |
| 0x1FFF 0D00 | System FLASH (BOOT_3KB+256B) |
| 0x1FFF 0000 | Reserved |
| 0x0801 0000 | Code FLASH 64KB |
| 0x0800 0000 | Aliased to Flash or system memory depending on BOOT pins |
| 0x0000 0000 | |

## 1.3 Clock Tree

4 groups of clock sources are introduced into the system: internal high frequency RC oscillator (HSI), internal low frequency RC oscillator (LSI), external high frequency oscillator (HSE), external low frequency oscillator (LSE). Among them, the low frequency clock source provides a clock reference for RTC and independent watchdogs. The high frequency clock source is directly or indirectly output to the system bus clock (SYSCLK) through PLL frequency doubling. the system clock is provided by each prescaler to provide HB domain, PB1 domain, PB2 domain peripheral control clock and sampling or interface output clock, and part of the module work needs to be provided directly by PLL clock.

Figure 1-3 Clock tree block diagram

~40 KHz LSI RC — IWDGCLK → to independent watchdog

OSC32_IN / OSC32_OUT — 32.768 KHz LSE OSC

/64 → to BKP

RTCCLK → to RTC

/128

SW → to OPA

OSC_IN / OSC_OUT — 3~25 MHz HSE OSC

PLLXTPRE  PLLSRC

USBPRE /1,/1.5,/2,/2.5 — enable — 48M — USBFS

/2

PLLMUL *3, *4, *16, *18 — PLLCLK

SW

8 MHz HSI RC

/2

HSI

SYSCLK

to Flash prog IF

HSE

CSS

MCO[3:0]

HB prescaler /1,/2,···/512

MCO ← HSI / HSE / PLLCLK/2

to HB bus/core/memory/DMA

FCLK core free running clock

/8 → to Core System timer

HCLK 96 MHz max

PB1 prescaler /1,/2,···/16

PCLK1 → to PB1 peripherals

peripheral clock enable

if(PB1 prescaler = 1)*1 else *2 — TIMxCLK → to TIM2/TIM3/TIM4

peripheral clock enable

PB2 prescaler /1,/2,···/16

PCLK2 → to PB2 peripherals

peripheral clock enable

if(PB2 prescaler=1)*1 else *2 — TIMxCLK → to TIM1

peripheral clock enable

ADC prescaler /2,/4,/6,/8 — ADCCLK → to ADC

ADC_PRE_ADJ

## 1.4 Functional Description

### 1.4.1 QingKe RISC-V4C Processor

RISC-V4C supports the IMAC subset of the RISC-V instruction set. The processor is managed internally in a modular fashion and contains units such as a programmable fast interrupt controller (PFIC), memory protection, branch prediction mode and extended instruction support. Externally multiple buses are connected to external unit modules, enabling interaction between external function modules and the core.

The processor with its minimal instruction set, multiple operating modes, and modular custom extensions can be flexibly applied to different scenarios of microcontroller design, such as small area low-power embedded scenarios, high performance application operating system scenarios, etc.

- Support machine and user privileged modes
- Programmable Fast Interrupt Controller (PFIC)
- Multi-level hardware interrupt stack
- 2-wire serial debug interface (SDI)
- Standard memory protection design
- Static or dynamic branch prediction, efficient jumping, conflict detection mechanisms
- Custom extension instructions

### 1.4.2 On-chip Memory

Built-in 20K bytes SRAM, available for storing data, which will be lost after power down. The specific capacity should correspond to the chip model.

Built-in 64K bytes program flash memory storage area (Code FLASH), i.e. user area, for user's application program and constant data storage. The specific size of the area corresponds to the chip model.

Built-in 3328 bytes System FLASH (System FLASH), i.e. BOOT area, used for system boot program storage, built-in bootstrap loading program.

Built-in 256-byte system non-volatile configuration information storage area, used for vendor's configuration word storage, factory-cured, user cannot be modified.

Built-in 256-byte user-defined information storage area for user-selected word storage.

At startup, one of three bootstrap modes can be selected via the bootstrap pins (BOOT0 and BOOT1):

- Bootstrap from program flash memory
- Boot from system memory
- Boot from internal SRAM

The bootstrap loading program is stored in the system memory and the contents of the program flash memory storage area can be reprogrammed via the USART1 and USB interfaces.

### 1.4.3 Power Supply Scheme

- $V_{DD}$ = 1.7 ~ 3.6V: Supplies power to the I/O pins and internal regulator.
- $V_{DDA}$ = 2.0 ~ 3.6V: Supplies power to the analog portion of the high-frequency RC oscillator, ADC, temperature sensor, and PLL. During normal operation. $V_{DDA}$ voltage must not be higher than $V_{DD}$ voltage; when using ADC, $V_{DDA}$ must not be less than 2.4V.
- $V_{BAT}$ = 1.8 ~ 3.6V: When $V_{DD}$ is turned off, power is supplied (via the internal power switcher) separately to the RTC, external low-frequency oscillator, and back-up registers. (Note $V_{BAT}$ power supply)

### 1.4.4 Power Supply Detector

A power-on reset (POR)/power-down reset (PDR) circuit is integrated inside the chip, which is always active to

ensure that the system operates when the power supply exceeds 1.8V; when $V_{DD}$ falls below the set threshold ($V_{POR/PDR}$), it puts the device in reset without the need for an external reset circuit.

In addition, the system has a programmable voltage monitor (PVD), which needs to be turned on by software to compare the voltage magnitude of the $V_{DD}$ supply with the set threshold $V_{PVD}$. Turning on the corresponding edge interrupt of the PVD allows you to receive an interrupt notification when $V_{DD}$ falls to the PVD threshold or rises to the PVD threshold. Refer to Chapter 3 for $V_{POR/PDR}$ and $V_{PVD}$ values.

### 1.4.5 System Voltage Regulator LDO

After resetting, the system voltage regulator is automatically switched on. There are two modes of operation depending on the application mode.

- On mode: Normal running operation, providing stable core power.
- Low-power mode: Low-power operation of the regulator when the CPU is in Standby mode.
- Shutdown mode: The regulator is automatically switched to this mode when the CPU enters the Standby mode, the regulator output is high resistance, the power supply to the core circuit is cut off, and the regulator is in the zero-consumption state.

The regulator is always in on mode after reset, and is turned off in standby mode in shutdown mode, when it is high resistance output.

### 1.4.6 Low-power Mode

The system supports 3 low-power modes, which can achieve the best balance under the conditions of low power consumption, short start-up time and multiple wake-up events.

- Sleep mode (SLEEP)

In sleep mode, only the CPU clock stops, but all peripheral clocks are powered normally and the peripherals are in working state. This mode is the shallowest low-power mode, but can achieve the fastest wake-up.

Exit condition: Any interruption or wake-up event.

- Stop mode (STOP)

This mode FLASH enters the low-power mode or power-off state, and the RC oscillator and HSE crystal oscillator of PLL and HSI are turned off. The stop mode can achieve the lowest power consumption while keeping the contents of SRAM and registers intact.

The stop mode is divided into 4 cases: Stop Mode 1, Stop Mode 2, Stop Mode 3 and Stop Mode 4. For detailed information, please refer to the Low-power Mode related chapter in the CH32L103RM manual.

Exit condition: Any external interrupt / event (EXTI signal), external reset signal on NRST, IWDG reset, in which EXTI signal includes one of 37 external I/O ports, PVD output, RTC alarm clock, USB wake-up signal, USBPD wake-up signal, touch-key (TKEY) wake-up signal, CMP wake-up signal, LPTIM wake-up signal and so on.

- Standby mode (STANDBY)

In this mode, the main LDO of the system is turned off, the wake-up circuit is powered by the low-power LDO, all other digital circuits are powered off, and the FLASH is in a power-off state. The wake-up system from standby mode will reset and SBF (PWR_CSR) will be set. After waking up, the SBF status is queried to know the low-power mode before wake-up, and the SBF is cleared by the CSBF (PWR_CR) bit. In standby mode, the contents of 20KB's SRAM can be maintained (depending on the planned configuration before going to bed), and the contents of the backup register can be retained.

Exit conditions: EXT10~EXT18 any external interrupt / event (EXTI signal), external reset signal on NRST, IWDG reset, in which EXTI signal includes one of 37 external I/O ports, PVD output, RTC alarm clock, touch-key (TKEY) wake-up signal, etc.

### 1.4.7 CRC Calculation Unit

The CRC (Cyclic Redundancy Check) Calculation Unit generates a CRC code from a 32-bit data word using a fixed polynomial generator. In numerous applications, CRC-based techniques are used to verify the consistency of data transmission or storage. Within the scope of the EN/IEC 60335-1 standard, which provides a means of detecting errors in flash memory, the CRC calculation unit can be used to compute the signature of software in real time and compare it with the signature generated at the time of linking and generating that software.

### 1.4.8 Programmable Fast Interrupt Controller (PFIC)

The chip has a built-in Programmable Fast Interrupt Controller (PFIC) that supports up to 255 interrupt vectors, providing flexible interrupt management with minimal interrupt latency. Currently the chip manages 4 core private interrupts and 53 peripheral interrupt management, with other interrupt sources reserved. the PFIC registers are all accessible in both user and machine privileged modes.

- 2 individually maskable interrupts
- Provide one non-maskable interrupt NMI
- Support hardware interrupt stack (HPE) without instruction overhead
- Provide 4 table-free interrupts (VTF) for faster access to interrupt service routines
- Vector table support address or instruction mode
- Interrupt nesting depth can be configured up to 2 levels
- Support interrupt tail linking

### 1.4.9 External Interrupt/Event Controller (EXTI)

The external interrupt/event controller contains a total of 23 edge detectors for generating interrupt/event requests. Each interrupt line can be configured independently of its trigger event (rising or falling edge or double edge) and can be individually masked; a pending register maintains the status of all interrupt requests. Up to 37 general purpose I/O ports are optionally connected to 16 external interrupt lines.

### 1.4.10 General DMA Controller

The system has a built-in general-purpose DMA controller that manages 8 channels to flexibly handle high-speed data transfers between memory to memory, peripheral to memory and memory to peripheral, supporting the ring buffer approach. Each channel has dedicated hardware DMA request logic to support one or more peripheral access requests to memory, with configurable access priority, transfer length, source and destination addresses for transfers, etc.

DMA is used for the main peripherals including: General-purpose/advanced-control timers TIMx, ADC, USART, I2C, SPI.

USB and USB PD have additional dedicated independent DMA channels.

*Note: DMA and CPU access to system SRAM after arbiter arbitration.*

### 1.4.11 Clock and Boot

The system clock source HSI is on by default. After no clock is configured or reset, the RC oscillator of the internal 8MHz is used as the default CPU clock, and then the external 3~25MHz clock or PLL clock can be selected. When clock safe mode is turned on, if HSE is used as the system clock (directly or indirectly), if an external clock failure is detected, the system clock will automatically switch to the internal RC oscillator, while HSE and PLL will automatically turn off; for low-power mode with clock off, the system will also automatically switch to the internal RC oscillator after waking up. If the clock interrupt is enabled, the software can receive the corresponding interrupt. Multiple prescalers are used to configure the frequency of HB, high-speed PB (PB2) and low-speed PB (PB1) areas

provide each peripheral clock, the highest frequency 96MHz, refer to the clock tree block diagram of figure 1-3.

### 1.4.12 RTC and Backup Register

The RTC and the backup register are in the backup power supply area within the system, which is powered by the $V_{DD}$ when the $V_{DD}$ is effective, and automatically switched to the power supply by the $V_{BAT}$ pin when the $V_{DD}$ is invalid.

The RTC real-time clock is a set of 32-bit programmable counters with a time base that supports 20-bit prescaling and is used for long-time measurement. The clock reference comes from a high-speed external clock division (HSE/128), an external crystal low frequency oscillator (LSE), or an internal low-power RC oscillator (LSI). Among them, there is also a backup power supply area in LSE, so when LSE is selected as RTC, the setting and time of RTC can remain unchanged after the system resets or wakes up from Standby mode.

The backup register contains 10 16-bit registers, which can be used to store 20 bytes of user application data. This data can be maintained after waking up on standby, or when the system is reset or the power is reset. When the intrusion detection function is turned on, once the intrusion detection signal is valid, all contents in the backup register will be cleared.

### 1.4.13 Analog-to-digital Converter (ADC) and Touch-key Capacitance Detection (TKey)

The chip has a built-in 12-bit ADC that provides up to 10 external channels and 3 internal channel samples with programmable channel sampling times for single, continuous, sweep or intermittent conversion. Provides analog watchdog function allows very precise monitoring of one or more selected channels for monitoring channel signal voltages, provides configurable analog watchdog reset function to reset the system when monitored voltage exceeds a threshold. Supports external event-triggered transitions. Trigger sources include internal signals from on-chip timers and external pins. Supports operation using DMA.

The internal channels of the ADC are ADC_IN16 to ADC_IN18. The temperature sensor is internally connected to the IN16 input channel for converting the sensor output to a digital value; the internal reference voltage is connected to the IN17 input channel; and VDDA/2 is connected to the IN18 input channel.

The touch-key capacitance detection unit provides up to 10 detection channels and reuses the external channels of the ADC module. The detection result is converted into the output result by the ADC module, and the touch-key state is identified by the user software.

### 1.4.14 Timer and Watchdog

● Advanced-control timer (TIM1)

The advanced-control timer is a 16-bit automatic load increment / decrement counter with a 16-bit programmable prescaler. In addition to the complete general timer function, it can be regarded as a three-phase PWM generator assigned to 6 channels, with a complementary PWM output function with dead-zone insertion, allowing the timer to be updated after a specified number of counter cycles for repeated counting cycles, braking functions, etc. Advanced control timers have the same functions as general timers and have the same internal structure, so advanced control timers can cooperate with other TIM timers through timer linking function to provide synchronization or event linking functions.

● General-purpose timer (TIM2, TIM3, TIM4)

The general-purpose timer is two 16-bit (TIM2, TIM3) and 1 32-bit (TIM4) autoload add / decrement counters with a programmable 16-bit prescaler and four independent channels, each of which supports input capture, output comparison, PWM generation, and single pulse mode output. It can also work with advanced control timers through the timer linking function to provide synchronization or event linking functions. In debug mode, counters can be frozen while PWM outputs are disabled, thus cutting off the switches controlled by these outputs. Any general timer

can be used to generate PWM output. Each timer has an independent DMA request mechanism. These timers can also process the signal of the incremental encoder and the digital output of 1 to 3 Hall sensors.

● Independent watchdog

Independent watchdog is a free-running 12-bit decreasing counter that supports 7 frequency division coefficients. The clock is provided by an internally independent RC oscillator (LSI) of about 40KHz. IWDG works completely independently of the main program, so it is used to reset the entire system in the event of a problem, or to provide timeout management for applications as a free timer. The option byte can be configured as a software or hardware startup watchdog. Counters can be frozen in debug mode.

● Window watchdog

The window watchdog is a 7-bit decrement counter and can be set to run freely. Can be used to reset the entire system when a problem occurs. It is driven by the main clock and has the function of early warning interrupt; in debug mode, the counter can be frozen.

● System time base timer

QingKe microprocessor core comes with a 64-bit optional increment or decrement counter, which is used to generate SYSTICK exceptions (exception number: 12), which can be specially used in real-time operating systems to provide "heartbeat" rhythm for the system, or can be used as a standard 64-bit counter. It has automatic reload function and programmable clock source.

## 1.4.15 Low-power Timer (LPTIM)

The low-power timer is a 16-bit auto-loading incremental counter with a 3-bit programmable prescaler. It can be triggered by either software or hardware inputs and supports PWM outputs. The Low-power Timer wakes up the system from a low-power mode and realizes a "time-out function" with very low-power consumption.

## 1.4.16 Universal Synchronous/Asynchronous Receiver Transmitter (USART)

The chip provides 4 sets of universal synchronous/asynchronous transceivers. It supports full duplex asynchronous serial communication, synchronous unidirectional communication as well as half duplex single line communication, also LIN (Local Interconnect Network), ISO7816 compatible smart card protocol and IrDA SIR ENDEC transmission codec specification, as well as modem (CTS/RTS hardware flow control) operation, and also supports multi-processor communication. It uses a fractional baud rate generator system and supports continuous communication by DMA operation.

## 1.4.17 Serial Peripheral Interface (SPI)

The chip provides 2 serial peripheral SPI interface, support master or slave operation, dynamic switching. Support multi-master mode, full-duplex or half-duplex synchronous transmission, support basic SD card and MMC mode. Programmable clock polarity and phase, data bit width provides 8- or 16-bit selection, hardware CRC generation/check for reliable communication, and continuous communication support for DMA operation.

## 1.4.18 I2C Bus

The chip provides 2 I2C bus interface, capable of working in multi-master or slave mode, performing all I2C bus specific timing, protocols, arbitration, etc. Both standard and fast communication speeds are supported and it is also compatible with SMBus 2.0.

The I2C interface provides 7-bit or 10-bit addressing, and supports dual slave addressing in 7-bit Slave mode. It integrates built-in hardware CRC generator/checker. It also supports DMA operation and supports SMBus bus version 2.0/PMBus bus.

### 1.4.19 Controller Area Network (CAN)

The chip provides 1 group CAN interface, compatible with specification 2.0A and 2.0B (active), baud rate up to 1Mbits/s, supports time-triggered communication function, supports CAN FD protocol, the biggest difference between traditional CAN is that the rate is variable, and the data bit rate is up to 8Mbps. it can receive and send standard frames with 11-bit identifiers, and also can receive and send extended frames with 29-bit identifiers. It can receive and send standard frames with 11-bit identifiers and extended frames with 29-bit identifiers. It has three transmitter mailboxes and two 3-level deep receive FIFOs.

### 1.4.20 Universal Serial Bus USB2.0 Full-speed Host/Device Controller (USBFS)

USB2.0 Full-speed Host Controller and Device Controller (USBFS) following the USB2.0 Full-speed standard and supporting the BC charging protocol. Provides 8 configurable USB device endpoints and a set of host endpoints. Supports control/lot/sync/interrupt transfers, double buffer mechanism, USB bus hang/resume operation and provides standby/wakeup functions. 48MHz clock dedicated to the USBFS module is generated directly from the internal high-speed clock (HSI).

### 1.4.21 USB PD and Type-C Controller (USB PD)

Built-in USB Power Delivery controller and PD transceiver PHY, support USB Type-C master-slave detection, automatic BMC codec and CRC, hardware edge control, support USB PD2.0 and PD3.0 power delivery control, support fast charging, support UFP/PD powered end Sink and DFP/PD powered end Source applications, DRP application as well as dynamic switching, some models have built-in controllable Rd pull-down resistor and support PDUSB.

### 1.4.22 General-purpose Input / Output (GPIO)

The system provides 4 sets of GPIO ports with a total of 37 GPIO pins. Each pin can be configured by software to output (push-pull or open-drain), input (with or without pull-up and pull-down), or reuse peripheral function ports. Most GPIO pins are shared with digital or analog multiplexing peripherals. Except for the ports with analog input function, all GPIO pins have greater current drive capability. Provides a locking mechanism to freeze the IO configuration to avoid accidental writing to the I/O register.

Most of the IO pin power supply in the system is provided by $V_{DD}$. By changing the $V_{DD}$ power supply, the IO pin output level will be changed to adapt to the external communication interface level. Please refer to the pin description for the specific pin.

### 1.4.23 Operational Amplifier/Comparator (OPA)

The chip has a built-in 1-group op-amp (OPA), which can also be used as a voltage comparator. Its input can be selected for multiple channels by changing the configuration, including amplification selection for the programmable gain op-amp (PGA), and its output can be selected for 2 channels by changing the configuration, internally associated to ADC channels. External analogue small signal amplification is supported for feeding into the ADC for small signal ADC conversion.

### 1.4.24 Voltage Comparator (CMP)

The chip has 3 built-in rail-to-rail analog voltage comparators with optional hysteresis characteristics. The voltage comparison results are triggered by the GPIO output or internally directly into the input channels CH1 ~ CH3 of the TIM2.

## 1.4.25 2-wire SDI Serial Debug Interface

The core comes with a 2-wire serial debug interface (SDI), including SWDIO and SWCLK pins. The default debug interface pin function is turned on after the system is powered on or reset, and the SDI can be turned off according to the need after the main program is running.

# Chapter 2 Pinouts and Pin Definition

## 2.1 Pinouts

CH32L103C8T6

| Pin | Signal |
|---|---|
| 48 | VDD |
| 47 | VSS |
| 46 | PB9 |
| 45 | PB8 |
| 44 | BOOT0 |
| 43 | PB7/CC2 |
| 42 | PB6/CC1 |
| 41 | PB5 |
| 40 | PB4 |
| 39 | PB3 |
| 38 | PA15 |
| 37 | PA14/SWCLK |

| Pin | Signal |
|---|---|
| 1 | VBAT |
| 2 | PC13/TAMPER/RTC |
| 3 | PC14/OSC32IN |
| 4 | PC15/OSC32OUT |
| 5 | OSC_IN/PD0 |
| 6 | OSC_OUT/PD1 |
| 7 | NRST |
| 8 | VSSA |
| 9 | VDDA |
| 10 | PA0/WKUP/ADC0/OPAP4 |
| 11 | PA1/ADC1/OPAN4 |
| 12 | PA2/ADC2/OPAO2 |

■ @VDD power

■ @VDD&VBAT power

| Pin | Signal |
|---|---|
| 36 | VDD |
| 35 | VSS |
| 34 | PA13/SWDIO |
| 33 | PA12/UDP |
| 32 | PA11/UDM |
| 31 | PA10 |
| 30 | PA9 |
| 29 | PA8 |
| 28 | PB15/OPAP0 |
| 27 | PB14/OPAP2 |
| 26 | PB13 |
| 25 | PB12 |

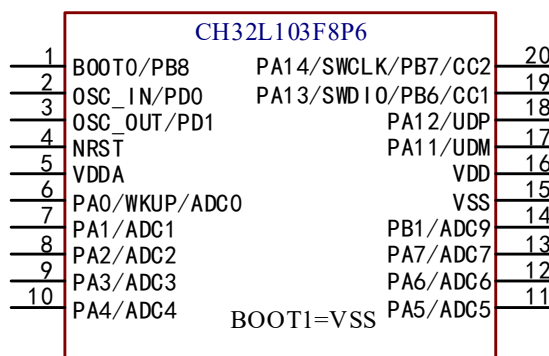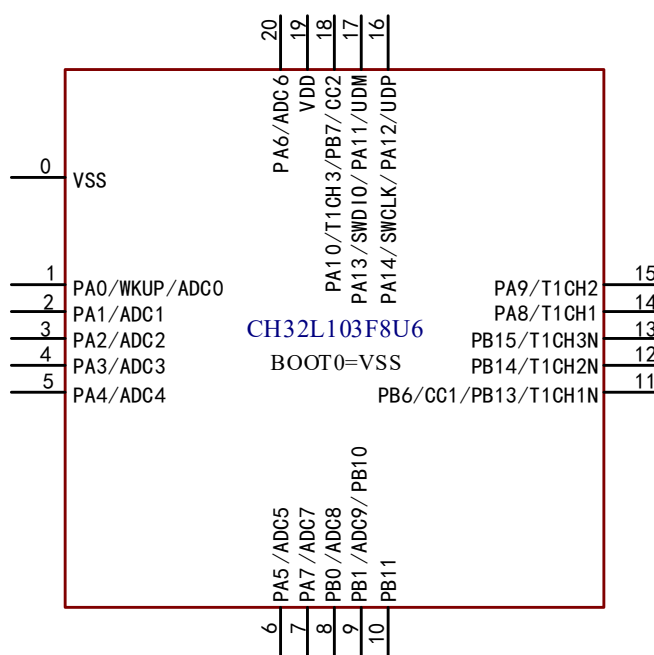| Pin | Signal |
|---|---|
| 13 | PA3/ADC3/OPA00 |
| 14 | PA4/ADC4/OPAO3 |
| 15 | PA5/ADC5/OPAN3 |
| 16 | PA6/ADC6/OPAP5/OPAN1 |
| 17 | PA7/ADC7/OPAP3/OPAN5 |
| 18 | PB0/ADC8/OPAP1/OPAO4 |
| 19 | PB1/ADC9/OPAO1 |
| 20 | PB2/BOOT1 |
| 21 | PB10/OPAN2/OPAN6 |
| 22 | PB11/OPAN0 |
| 23 | VSS |
| 24 | VDD |

CH32L103K8U6

| Pin | Signal |
|---|---|
| 32 | PB8 |
| 31 | BOOT0/PB9 |
| 30 | PB7/CC2 |
| 29 | PB6/CC1 |
| 28 | PB5 |
| 27 | PB4 |
| 26 | PB3 |
| 25 | PA15 |

| Pin | Signal |
|---|---|
| 0 | VSS |
| 1 | VDD |
| 2 | PC14/OSC32IN |
| 3 | PC15/OSC32OUT |
| 4 | OSC_IN/PD0 |
| 5 | OSC_OUT/PD1 |
| 6 | PA0/WKUP/ADC0 |
| 7 | PA1/ADC1 |
| 8 | PA2/ADC2 |

| Pin | Signal |
|---|---|
| 24 | PA14/SWCLK |
| 23 | PA13/SWDIO |
| 22 | PA12/UDP |
| 21 | PA11/UDM |
| 20 | PA10 |
| 19 | PA9 |
| 18 | PA8 |
| 17 | PB15 |

| Pin | Signal |
|---|---|
| 9 | PA3/ADC3 |
| 10 | PA4/ADC4 |
| 11 | PA5/ADC5 |
| 12 | PA6/ADC6 |
| 13 | PA7/ADC7 |
| 14 | PB0/ADC8 |
| 15 | PB1/ADC9 |
| 16 | PB2/BOOT1 |

**CH32L103G8R6**

| Pin | Left | Right | Pin |
|---|---|---|---|
| 1 | PA14/SWCLK/PB5/CMP3P0 | PA13/SWDIO/PA12/UDP | 28 |
| 2 | PB6/CC1/SCL/T4CH1 | PA11/UDM/T1CH4 | 27 |
| 3 | PB7/CC2/SDA/T4CH2 | PA10/T1CH3 | 26 |
| 4 | PB3/CMPxN | PA9/T1CH2 | 25 |
| 5 | PB8/T4CH3/CMP2P | PA8/T1CH1 | 24 |
| 6 | VDD | PB15/T1CH3N | 23 |
| 7 | VSS | PB14/T1CH2N | 22 |
| 8 | PD0 | PB13/T1CH1N | 21 |
| 9 | PA0/WKUP/ADC0 | PB12/T1BK/CMP3O | 20 |
| 10 | PA1/ADC1 | PB11/CMP3N1 | 19 |
| 11 | PA2/ADC2/CMP1P | PB1/ADC9/OPA0/PB10/CMP3P1 | 18 |
| 12 | PA3/ADC3 | PA7/ADC7/OPAN | 17 |
| 13 | PA4/ADC4 | PB0/ADC8/OPAP | 16 |
| 14 | PA5/ADC5 | PA6/ADC6 | 15 |

BOOT0=VSS

**CH32L103F8U6**

Top pins (left to right): 20 PA6/ADC6, 19 VDD, 18 PB7/CC2, 17 PA11/UDM, 16 PA12/UDP

Top labels: PA10/T1CH3/PB7/CC2, PA13/SWDIO/PA11/UDM, PA14/SWCLK/PA12/UDP

| Pin | Left | Right | Pin |
|---|---|---|---|
| 0 | VSS | | |
| 1 | PA0/WKUP/ADC0 | PA9/T1CH2 | 15 |
| 2 | PA1/ADC1 | PA8/T1CH1 | 14 |
| 3 | PA2/ADC2 | PB15/T1CH3N | 13 |
| 4 | PA3/ADC3 | PB14/T1CH2N | 12 |
| 5 | PA4/ADC4 | PB6/CC1/PB13/T1CH1N | 11 |

BOOT0=VSS

Bottom pins (left to right): 6 PA5/ADC5, 7 PA7/ADC7, 8 PB0/ADC8, 9 PB1/ADC9/PB10, 10 PB11

**CH32L103F8P6**

| Pin | Left | Right | Pin |
|---|---|---|---|
| 1 | BOOT0/PB8 | PA14/SWCLK/PB7/CC2 | 20 |
| 2 | OSC_IN/PD0 | PA13/SWDIO/PB6/CC1 | 19 |
| 3 | OSC_OUT/PD1 | PA12/UDP | 18 |
| 4 | NRST | PA11/UDM | 17 |
| 5 | VDDA | VDD | 16 |
| 6 | PA0/WKUP/ADC0 | VSS | 15 |
| 7 | PA1/ADC1 | PB1/ADC9 | 14 |
| 8 | PA2/ADC2 | PA7/ADC7 | 13 |
| 9 | PA3/ADC3 | PA6/ADC6 | 12 |
| 10 | PA4/ADC4 | PA5/ADC5 | 11 |

BOOT1=VSS

*Note: The alternate functions in the pin diagram are abbreviated.*

Example: ADC: ADC_ (ADC0: ADC_IN0)

   T: TIME_ (T1CH3:TIM1_CH3, T1CH1N: TIM1_CH1N, T1BK: TIM1_BKIN)

   OPA: OPA_ (OPAP4: OPA_P4, OPAN4: OPA_N4, OPAO2: OPA_O2)

   UDP: USBDP

   UDM: USBDM

## 2.2 Pin Description

Note that the pin function descriptions in the table below are for all functions and do not refer to specific chip models. Peripheral resources may vary from model to model, so please check the availability of this function against the chip model resource table before viewing.

Table 2-1 QFN20/QSOP28/QFN32/LQFP48 Pin definitions

| Pin No. | | | | Pin name | Pin type[1] | I/O level | Main function (after reset) | Default alternate function | Remapping function[10] |
|---|---|---|---|---|---|---|---|---|---|
| QFN20 | QSOP28 | QFN32 | LQFP48 | | | | | | |
| - | - | - | 1 | $V_{BAT}$ | P | - | $V_{BAT}$ | | |
| - | - | - | 2 | PC13-TAMPER-RTC[2] | I/O | - | PC13[3] | TAMPER RTC | |
| - | - | 2 | 3 | PC14-OSC32_IN[2] | I/O/A | - | PC14[3] | OSC32_IN | |
| - | - | 3 | 4 | PC15-OSC32_OUT[2] | I/O/A | - | PC15[3] | OSC32_OUT | |
| - | 8 | 4 | 5 | OSC_IN | I/O/A | - | OSC_IN | | PD0[4] USART3_TX_3 USART3_RX_2 CAN_RX_3 |
| - | - | 5 | 6 | OSC_OUT | I/O/A | - | OSC_OUT | | PD1[4] USART3_TX_2 USART3_RX_3 CAN_TX_3 |
| - | - | - | 7 | NRST | I | - | NRST | | |
| - | - | - | 8 | $V_{SSA}$ | P | - | $V_{SSA}$ | | |
| - | - | - | 9 | $V_{DDA}$ | P | - | $V_{DDA}$ | | |
| 1 | 9 | 6 | 10 | PA0-WKUP | I/O/A | - | PA0 | WKUP ADC_IN0 TIM2_CH1_ETR USART2_CTS OPA_P4 | TIM2_CH1_ETR_2 USART2_CTS_2 USART2_CTS_3 |
| 2 | 10 | 7 | 11 | PA1 | I/O/A | - | PA1 | ADC_IN1 TIM2_CH2 USART2_RTS OPA_N4 | TIM1_CH1_2 TIM1_CH1_3 TIM2_CH2_2 TIM1_CH2N_5 USART2_RTS_2 USART2_RTS_3 |
| 3 | 11 | 8 | 12 | PA2 | I/O/A | - | PA2 | ADC_IN2 CMP1_P0 OPA_O2 | TIM1_CH4_4 TIM2_CH2_4 TIM2_CH2_5 |

| Pin No. | | | | Pin name | Pin type[1] | I/O level | Main function (after reset) | Default alternate function | Remapping function[10] |
|---|---|---|---|---|---|---|---|---|---|
| QFN20 | QSOP28 | QFN32 | LQFP48 | | | | | | |
| | | | | | | | | TIM2_CH3<br>USART2_TX | TIM2_CH3_1<br>USART1_CTS_2 |
| 4 | 12 | 9 | 13 | PA3 | I/O/A | - | PA3 | ADC_IN3<br>OPA_O0<br>TIM2_CH4<br>USART2_RX | TIM1_ETR_3<br>TIM1_CH4_5<br>TIM2_CH1_ETR_4<br>TIM2_CH4_1<br>USART1_CK_2 |
| 5 | 13 | 10 | 14 | PA4 | I/O/A | - | PA4 | ADC_IN4<br>OPA_O3<br>USART2_CK<br>SPI1_NSS | TIM2_CH4_7<br>USART1_TX_2<br>USART1_RX_3<br>USART2_CK_2<br>USART2_CK_3 |
| 6 | 14 | 11 | 15 | PA5 | I/O/A | - | PA5 | ADC_IN5<br>SPI1_SCK<br>OPA_N3 | TIM2_CH3_7<br>USART1_TX_3<br>USART1_RX_2<br>USART4_TX_1 |
| 20 | 15 | 12 | 16 | PA6 | I/O/A | - | PA6 | ADC_IN6<br>TIM3_CH1<br>SPI1_MISO<br>OPA_N1<br>OPA_P5 | TIM1_BKIN_1<br>TIM2_CH4_4<br>TIM2_CH4_5<br>USART1_CK_3<br>USART1_CK_4<br>USART4_CK_1 |
| 7 | 17 | 13 | 17 | PA7 | I/O/A | - | PA7 | SPI1_MOSI<br>ADC_IN7<br>TIM3_CH2<br>OPA_N5<br>OPA_P3 | TIM1_CH1N_1<br>TIM1_CH2_2<br>TIM1_CH2_3<br>USART4_CTS_1 |
| 8 | 16 | 14 | 18 | PB0 | I/O/A | - | PB0 | ADC_IN8<br>TIM3_CH3<br>USART4_TX<br>CMP1_OUT0<br>OPA_P1<br>OPA_O4 | TIM1_CH2N_1<br>TIM1_CH2N_2<br>TIM1_CH2N_3<br>TIM3_CH3_1 |
| 9 | 18 | 15 | 19 | PB1[7][8] | I/O/A | - | PB1 | ADC_IN9<br>TIM3_CH4<br>USART4_RX<br>CMP1_N0<br>OPA_O1 | TIM1_CH1_5<br>TIM1_CH4_2<br>TIM1_CH4_3<br>TIM1_CH2N_4<br>TIM1_CH3N_1<br>TIM3_CH4_1 |

| Pin No. | | | | Pin name | Pin type[1] | I/O level | Main function (after reset) | Default alternate function | Remapping function[10] |
|---|---|---|---|---|---|---|---|---|---|
| QFN20 | QSOP28 | QFN32 | LQFP48 | | | | | | |
| - | - | 16 | 20 | PB2[5] | I/O/A | FT | PB2 BOOT1[5] | USART4_CK CMP1_P1 | LPT_OUT_1 |
| 9 | 18 | - | 21 | PB10[7][8] | I/O/A | FT | PB10 | USART3_TX I2C2_SCL CMP1_OUT1 CMP3_P1 OPA_N2 OPA_N6 | TIM4_CH1_1 TIM2_CH3_2 TIM2_CH3_3 |
| 10 | 19 | - | 22 | PB11 | I/O/A | FT | PB11 | CMP2_OUT1 CMP3_N1 OPA_N0 USART3_RX I2C2_SDA | TIM1_CH1N_2 TIM1_CH1N_3 TIM2_CH4_2 TIM2_CH4_3 TIM4_CH2_1 USART1_TX_4 I2C1_SDA_3 |
| 0 | 7 | 0 | 23 | V$_{SS}$ | P | - | V$_{SS}$ | | |
| 19 | 6 | 1 | 24 | V$_{DD}$ | P | - | V$_{DD}$ | | |
| - | 20 | - | 25 | PB12 | I/O/A | FT | PB12 | CMP3_OUT1 TIM1_BKIN LPT_IN1 USART3_CK I2C2_SMBA SPI2_NSS | TIM1_CH3_4 TIM2_CH3_4 TIM2_CH3_5 USART1_TX_5 USART3_CK_2 USART3_CK_3 SPI1_NSS_3 |
| 11 | 21 | - | 26 | PB13[8] | I/O | FT | PB13 | TIM1_CH1N LPT_IN2 USART3_CTS SPI2_SCK | USART3_CTS_2 USART3_CTS_3 |
| 12 | 22 | - | 27 | PB14 | I/O/A | FT | PB14 | TIM1_CH2N LPT_ETR USART3_RTS SPI2_MISO OPA_P2 | USART3_RTS_2 USART3_RTS_3 |
| 13 | 23 | 17 | 28 | PB15 | I/O/A | FT | PB15 | TIM1_CH3N LPT_OUT SPI2_MOSI OPA_P0 | |

| Pin No. | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| QFN20 | QSOP28 | QFN32 | LQFP48 | Pin name | Pin type(1) | I/O level | Main function (after reset) | Default alternate function | Remapping function(10) |
| 14 | 24 | 18 | 29 | PA8 | I/O | FT | PA8 | MCO<br>TIM1_CH1<br>USART1_CK | TIM1_CH1_1<br>USART1_CK_1 |
| 15 | 25 | 19 | 30 | PA9 | I/O | FT | PA9 | TIM1_CH2<br>USART1_TX | TIM1_CH2_1 |
| 18 | 26 | 20 | 31 | PA10(8) | I/O | FT | PA10 | TIM1_CH3<br>USART1_RX | TIM1_CH3_1 |
| 17 | 27 | 21 | 32 | PA11(8) | I/O/A | FT | PA11 | TIM1_CH4<br>USART1_CTS<br>USBDM<br>CAN_RX | TIM1_CH4_1<br>USART1_CTS_1<br>USART2_TX_2<br>USART2_RX_3 |
| 16 | 28 | 22 | 33 | PA12(7)(8) | I/O/A | FT | PA12 | USART1_RTS<br>USBDP<br>CAN_TX<br>TIM1_ETR | USART1_RTS_1<br>TIM1_ETR_1<br>TIM1_BKIN_4<br>TIM1_BKIN_5<br>TIM2_CH1_ETR_5<br>TIM2_CH1_ETR_7<br>USART1_RX_5<br>USART2_TX_3<br>USART2_RX_2<br>I2C1_SDA_2<br>SPI1_NSS_2 |
| 17 | | 23 | 34 | PA13(7)(8) | I/O | FT | SWDIO | | TIM1_ETR_5<br>TIM1_BKIN_2<br>TIM1_BKIN_3<br>USART1_RTS_2<br>USART1_RTS_4<br>I2C1_SCL_2 |
| - | - | | 35 | V$_{SS}$ | P | - | V$_{SS}$ | | |
| - | - | | 36 | V$_{DD}$ | P | - | V$_{DD}$ | | |
| 16 | 1 | 24 | 37 | PA14(7)(8) | I/O | FT | SWCLK | | TIM1_CH3_2<br>TIM1_CH3_3<br>TIM1_CH1N_4<br>TIM1_CH1N_5<br>USART1_CTS_4 |

| Pin No. | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| QFN20 | QSOP28 | QFN32 | LQFP48 | Pin name | Pin type[1] | I/O level | Main function (after reset) | Default alternate function | Remapping function[10] |
| - | - | 25 | 38 | PA15 | I/O | FT | PA15 | | TIM2_CH1_ETR_1<br>TIM2_CH1_ETR_3<br>USART4_RTS_1<br>SPI1_NSS_1 |
| - | 4 | 26 | 39 | PB3 | I/O/A | FT | PB3 | CMP1_N1<br>CMP2_N0<br>CMP3_N0<br>USART4_CTS | TIM2_CH2_1<br>TIM2_CH2_3<br>SPI1_SCK_1 |
| - | - | 27 | 40 | PB4 | I/O/A | FT | PB4 | CMP3_OUT0<br>USART4_RTS | TIM3_CH1_1<br>SPI1_MISO_1 |
| - | 1 | 28 | 41 | PB5[7] | I/O/A | FT | PB5 | I2C1_SMBA<br>CMP2_OUT0<br>CMP3_P0 | LPT_IN1_1<br>TIM3_CH2_1<br>USART4_RX_1<br>I2C1_SMBA_2<br>I2C1_SMBA_3<br>SPI1_MOSI_1 |
| 11 | 2 | 29 | 42 | PB6[8] | I/O/A | FT | PB6 | TIM4_CH1<br>I2C1_SCL<br>CC1<br>CMP2_P1 | LPT_ETR_1<br>USART1_TX_1<br>USART1_CK_5<br>SPI1_SCK_2<br>SPI1_SCK_3<br>TIM1_ETR_2<br>TIM1_ETR_4<br>TIM1_CH3_5 |
| 18 | 3 | 30 | 43 | PB7[8] | I/O/A | FT | PB7 | TIM4_CH2<br>I2C1_SDA<br>CC2<br>CMP2_N1 | LPT_IN2_1<br>USART1_RX_1<br>USART1_CTS_3<br>USART1_CTS_5<br>SPI1_MOSI_2<br>SPI1_MOSI_3<br>TIM1_CH1_4<br>TIM1_CH3N_5 |
| - | - | 31 | 44 | BOOT0[6] | I | - | BOOT0 | | |
| - | 5 | 32 | 45 | PB8 | I/O/A | FT | PB8 | TIM4_CH3<br>CMP2_P0 | TIM4_CH3_1<br>USART1_RTS_3<br>USART1_RTS_5<br>SPI1_MISO_2<br>SPI1_MISO_3 |

| Pin No. | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| QFN20 | QSOP28 | QFN32 | LQFP48 | Pin name | Pin type[1] | I/O level | Main function (after reset) | Default alternate function | Remapping function[10] |
| | | | | | | | | | CAN_RX_2 TIM1_CH2_4 TIM1_CH2_5 TIM2_CH2_7 |
| - | - | 31 | 46 | PB9[6] | I/O/A | FT | PB9 | TIM4_CH4 | TIM4_CH4_1 USART1_RX_4 I2C1_SCL_3 CAN_TX_2 TIM1_CH3N_2 TIM1_CH3N_3 TIM1_CH3N_4 |
| - | - | - | 47 | $V_{SS}$ | P | - | $V_{SS}$ | | |
| - | - | - | 48 | $V_{DD}$ | P | - | $V_{DD}$ | | |

Table 2-2 TSSOP20 Pin definitions

| Pin No. | | | | | | |
|---|---|---|---|---|---|---|
| TSSOP20 | Pin name | Pin type[1] | I/O level | Main function (after reset) | Default alternate function | Remapping function[12] |
| 2 | OSC_IN | I/O/A | - | OSC_IN | | PD0[4] USART3_TX_3 USART3_RX_2 CAN_RX_3 |
| 3 | OSC_OUT | I/O/A | - | OSC_OUT | | PD1[4] USART3_TX_2 USART3_RX_3 CAN_TX_3 |
| 4 | NRST | I | - | NRST | | |
| 5 | $V_{DDA}$ | P | - | $V_{DDA}$ | | |
| 6 | PA0-WKUP | I/O/A | - | PA0 | WKUP ADC_IN0 TIM2_CH1_ETR USART2_CTS OPA_P4 | TIM2_CH1_ETR_2 USART2_CTS_2 USART2_CTS_3 |
| 7 | PA1 | I/O/A | - | PA1 | ADC_IN1 TIM2_CH2 USART2_RTS OPA_N4 | TIM1_CH1_2 TIM1_CH1_3 TIM2_CH2_2 TIM1_CH2N_5 USART2_RTS_2 |

| Pin No. | | | | | | |
| --- | --- | --- | --- | --- | --- | --- |
| TSSOP20 | Pin name | Pin type[1] | I/O level | Main function (after reset) | Default alternate function | Remapping function[12] |
| | | | | | | USART2_RTS_3 |
| 8 | PA2 | I/O/A | - | PA2 | ADC_IN2 CMP1_P0 OPA_O2 TIM2_CH3 USART2_TX | TIM1_CH4_4 TIM2_CH2_4 TIM2_CH2_5 TIM2_CH3_1 USART1_CTS_2 |
| 9 | PA3 | I/O/A | - | PA3 | ADC_IN3 OPA_O0 TIM2_CH4 USART2_RX | TIM1_ETR_3 TIM1_CH4_5 TIM2_CH1_ETR_4 TIM2_CH4_1 USART1_CK_2 |
| 10 | PA4 | I/O/A | - | PA4 | ADC_IN4 OPA_O3 USART2_CK SPI1_NSS | TIM2_CH4_7 USART1_TX_2 USART1_RX_3 USART2_CK_2 USART2_CK_3 |
| 11 | PA5 | I/O/A | - | PA5 | ADC_IN5 SPI1_SCK OPA_N3 | TIM2_CH3_7 USART1_TX_3 USART1_RX_2 USART4_TX_1 |
| 12 | PA6 | I/O/A | - | PA6 | ADC_IN6 TIM3_CH1 SPI1_MISO OPA_N1 OPA_P5 | TIM1_BKIN_1 TIM2_CH4_4 TIM2_CH4_5 USART1_CK_3 USART1_CK_4 USART4_CK_1 |
| 13 | PA7 | I/O/A | - | PA7 | SPI1_MOSI ADC_IN7 TIM3_CH2 OPA_N5 OPA_P3 | TIM1_CH1N_1 TIM1_CH2_2 TIM1_CH2_3 USART4_CTS_1 |
| 14 | PB1 | I/O/A | - | PB1 | ADC_IN9 TIM3_CH4 USART4_RX CMP1_N0 OPA_O1 | TIM1_CH1_5 TIM1_CH4_2 TIM1_CH4_3 TIM1_CH2N_4 TIM1_CH3N_1 TIM3_CH4_1 |
| - | PB10 | I/O/A | FT | PB10 | USART3_TX | TIM4_CH1_1 |

| Pin No. TSSOP20 | Pin name | Pin type(1) | I/O level | Main function (after reset) | Default alternate function | Remapping function(12) |
|---|---|---|---|---|---|---|
| | | | | | I2C2_SCL CMP1_OUT1 CMP3_P1 OPA_N2 OPA_N6 | TIM2_CH3_2 TIM2_CH3_3 |
| - | PB11 | I/O/A | FT | PB11 | CMP2_OUT1 CMP3_N1 OPA_N0 USART3_RX I2C2_SDA | TIM1_CH1N_2 TIM1_CH1N_3 TIM2_CH4_2 TIM2_CH4_3 TIM4_CH2_1 USART1_TX_4 I2C1_SDA_3 |
| 15 | V$_{SS}$ | P | - | V$_{SS}$ | | |
| 16 | V$_{DD}$ | P | - | V$_{DD}$ | | |
| - | PB13 | I/O | FT | PB13 | TIM1_CH1N LPT_IN2 USART3_CTS SPI2_SCK | USART3_CTS_2 USART3_CTS_3 |
| - | PB14 | I/O/A | FT | PB14 | TIM1_CH2N LPT_ETR USART3_RTS SPI2_MISO OPA_P2 | USART3_RTS_2 USART3_RTS_3 |
| - | PB15 | I/O/A | FT | PB15 | TIM1_CH3N LPT_OUT SPI2_MOSI OPA_P0 | |
| - | PA8 | I/O | FT | PA8 | MCO TIM1_CH1 USART1_CK | TIM1_CH1_1 USART1_CK_1 |
| - | PA9 | I/O | FT | PA9 | TIM1_CH2 USART1_TX | TIM1_CH2_1 |
| - | PA10 | I/O | FT | PA10 | TIM1_CH3 USART1_RX | TIM1_CH3_1 |
| 17 | PA11 | I/O/A | FT | PA11 | TIM1_CH4 USART1_CTS USBDM CAN_RX | TIM1_CH4_1 USART1_CTS_1 USART2_TX_2 USART2_RX_3 |

| Pin No. TSSOP20 | Pin name | Pin type(1) | I/O level | Main function (after reset) | Default alternate function | Remapping function(12) |
|---|---|---|---|---|---|---|
| 18 | PA12 | I/O/A | FT | PA12 | USART1_RTS USBDP CAN_TX TIM1_ETR | USART1_RTS_1 TIM1_ETR_1 TIM1_BKIN_4 TIM1_BKIN_5 TIM2_CH1_ETR_5 TIM2_CH1_ETR_7 USART1_RX_5 USART2_TX_3 USART2_RX_2 I2C1_SDA_2 SPI1_NSS_2 |
| 19 | PA13(9) | I/O | FT | SWDIO | | TIM1_ETR_5 TIM1_BKIN_2 TIM1_BKIN_3 USART1_RTS_2 USART1_RTS_4 I2C1_SCL_2 |
| 20 | PA14(9) | I/O | FT | SWCLK | | TIM1_CH3_2 TIM1_CH3_3 TIM1_CH1N_4 TIM1_CH1N_5 USART1_CTS_4 |
| 19 | PB6(9) | I/O/A | FT | PB6 | TIM4_CH1 I2C1_SCL CC1 CMP2_P1 | LPT_ETR_1 USART1_TX_1 USART1_CK_5 SPI1_SCK_2 SPI1_SCK_3 TIM1_ETR_2 TIM1_ETR_4 TIM1_CH3_5 |
| 20 | PB7(9) | I/O/A | FT | PB7 | TIM4_CH2 I2C1_SDA CC2 CMP2_N1 | LPT_IN2_1 USART1_RX_1 USART1_CTS_3 USART1_CTS_5 SPI1_MOSI_2 SPI1_MOSI_3 TIM1_CH1_4 TIM1_CH3N_5 |
| 1 | BOOT0(6) | I | - | BOOT0 | | |

| Pin No. TSSOP20 | Pin name | Pin type[1] | I/O level | Main function (after reset) | Default alternate function | Remapping function[12] |
|---|---|---|---|---|---|---|
|  | PB8[6] | I/O/A | FT | PB8 | TIM4_CH3 CMP2_P0 | TIM4_CH3_1 USART1_RTS_3 USART1_RTS_5 SPI1_MISO_2 SPI1_MISO_3 CAN_RX_2 TIM1_CH2_4 TIM1_CH2_5 TIM2_CH2_7 |

*Note 1: Explanation of table abbreviations:*

*I = TTL/CMOS level Schmitt input; O = CMOS level tri-state output;*

*A = analog signal input or output; P = power supply; FT = tolerant 5V;*

*Note 2: when the backup domain is powered by $V_{DD}$ (internal analog switch connected to $V_{DD}$): PC14 and PC15 can be used for GPIO or LSE pins, PC13 can be used as a general-purpose Imax O port, TAMPER pin, RTC calibration clock, RTC alarm clock or second output; as an output pin, it can only work in 2MHz mode, and the maximum drive load is 30pF. When the backup domain is $V_{BAT}$ (analog switch connection to BAT after $V_{DD}$ disappears): PC14 and PC15 can only be used for LSE pins, PC13 can be used as TAMPER pins, RTC alarm clock or second output.*

*Note 3: these pins are in the main function state when the backup domain is powered on for the first time, and even if they are reset, the state of these pins is controlled by the backup domain register (these registers will not be reset by the master reset system). For specific information on how to control these IO ports, please refer to the relevant sections of the battery backup domain and BKP registers in the CH32L103RM manual.*

*Note 4: For the CH32L103C8T6 chip, pin 5 and pin 6 are configured as OSC_IN and OSC_OUT function pins by default after chip reset, and the software can reset these two pins to PD0 and PD1 functions; for the CH32L103K8U6 chip, pin 4 and pin 5 are configured as OSC_IN and OSC_OUT function pins by default after chip reset. The software can reset these two pins to PD0 and PD1 functions; For the CH32L103G8R6 chip, pin 8 is configured as the OSC_IN function pin by default after chip reset, and the software can reset these two pins to PD0 function; for the CH32L103F8P6 chip, pin 2 and pin 3 are configured as the OSC_IN and OSC_OUT function pins by default after chip reset, and the software can reset these two pins to PD0 and PD1 functions. For more detailed information, please refer to the Multiplexed Function I/O section and the Debug Setup section of the CH32L103RM manual.*

*Note 5: BOOT0 pin will be pulled down to the GND internally. The BOOT0 pin leads out, but the BOOT1/PB2 pin does not lead out of the chip, the internal BOOT1/PB2 pin will be pulled down to the GND. If you enter the low-power mode to configure the IO port state, it is recommended that the BOOT1/PB2 pin use the input drop-down mode to prevent additional current generation.*

*Note 6: For CH32L103K8U6 chips, BOOT0 and PB9 pins are short sealed inside the chip, and PB9 pins no longer support voltage 5V; for CH32L103F8P6 chips, BOOT0 and PB8 pins are short sealed inside the chip, and PB8 pins no longer support voltage 5V. It is recommended to connect an external 470K pull-down resistor to ensure that the BOOT0 is low during power-up in order to enter the program flash memory bootstrap mode. After normal operation,*

*PB9, PB3 and PB8 pins can be used for output as needed.*

*Note 7: For the CH32L103G8R6 chip, the PA14 and PB5 pins are short sealed inside the chip, so it is forbidden to configure both IO as the output function; when the PB1 and PB10 pins are short sealed inside the chip, the PB10 pin no longer supports voltage tolerant 5V, and it is forbidden to configure both IO as the output function. The PA12 and PA13 pins are short-connected and sealed inside the chip, so it is forbidden to configure both IO as the output function.*

*Note 8: For the CH32L103F8U6 chip, the PB1 and PB10 pins are shorted and sealed inside the chip, so the PB10 pin no longer supports voltage 5V, and both IO are prohibited from being configured as the output function; the PB6 and PB13 pins are shorted and sealed inside the chip, and both IO are prohibited from being configured as the output function; PA12 and PA14 pins are shorted inside the chip, and both IO are prohibited from being configured as the output function. The PA11 and PA13 pins are short-connected and sealed inside the chip, so it is forbidden to configure both IO as the output function, while the PA10 and PB7 pins are short-connected and sealed inside the chip, so it is forbidden to configure both IO as the output function.*

*Note 9: For the CH32L103F8P6 chip, PA13 and PB6 pins are short-connected and sealed inside the chip, and both IO are prohibited from being configured as output functions; PA14 and PB7 pins are short-connected and sealed inside the chip, and both IO are prohibited from being configured as output functions.*

*Note 10: The underlined value of the remapping function indicates the configuration value of the corresponding bit in the AFIO register. For example, CAN_RX_2 indicates that the corresponding bit configuration of the AFIO register is 10b.*

## 2.3 Pin Alternate Functions

*Note: The pin function in the table below refer to all functions and does not involve specific model(s). There are differences in peripheral resources between different models. Please confirm whether this function is available according to the particular model's resource table before viewing this table.*

Table 2-3 Pin alternate and remapping functions

| Alternate Pin | ADC | TIM1 | TIM2/3/4 | USART | CMP | SYS | I2C | SPI | CAN | USB | OPA | LPTIM |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PA0 | ADC_IN0 | | TIM2_CH1_ETR<br>TIM2_CH1_ETR_2 | USART2_CTS<br>USART2_CTS_2<br>USART2_CTS_3 | | WKUP | | | | | OPA_P4 | |
| PA1 | ADC_IN1 | TIM1_CH1_2<br>TIM1_CH1_3<br>TIM1_CH2N_5 | TIM2_CH2<br>TIM2_CH2_2 | USART2_RTS<br>USART2_RTS_2<br>USART2_RTS_3 | | | | | | | OPA_N4 | |
| PA2 | ADC_IN2 | TIM1_CH4_4 | TIM2_CH2_4<br>TIM2_CH2_5<br>TIM2_CH3<br>TIM2_CH3_1 | USART1_CTS_2<br>USART2_TX | CMP1_P0 | | | | | | OPA_O2 | |
| PA3 | ADC_IN3 | TIM1_ETR_3<br>TIM1_CH4_5 | TIM2_CH1_ETR_4<br>TIM2_CH4<br>TIM2_CH4_1 | USART1_CK_2<br>USART2_RX | | | | | | | OPA_O0 | |
| PA4 | ADC_IN4 | | TIM2_CH4_7 | USART1_TX_2<br>USART1_RX_3<br>USART2_CK<br>USART2_CK_2<br>USART2_CK_3 | | | | SPI1_NSS | | | OPA_O3 | |
| PA5 | ADC_IN5 | | TIM2_CH3_7 | USART1_TX_3<br>USART1_RX_2<br>USART4_TX_1 | | | | SPI1_SCK | | | OPA_N3 | |
| PA6 | ADC_IN6 | TIM1_BKIN_1 | TIM2_CH4_4<br>TIM2_CH4_5<br>TIM3_CH1 | USART1_CK_3<br>USART1_CK_4<br>USART4_CK_1 | | | | SPI1_MISO | | | OPA_N1<br>OPA_P5 | |
| PA7 | ADC_IN7 | TIM1_CH2_2<br>TIM1_CH2_3<br>TIM1_CH1N_1 | TIM3_CH2 | USART4_CTS_1 | | | | SPI1_MOSI | | | OPA_N5<br>OPA_P3 | |
| PA8 | | TIM1_CH1<br>TIM1_CH1_1 | | USART1_CK<br>USART1_CK_1 | | MCO | | | | | | |
| PA9 | | TIM1_CH2<br>TIM1_CH2_1 | | USART1_TX | | | | | | | | |
| PA10 | | TIM1_CH3<br>TIM1_CH3_1 | | USART1_RX | | | | | | | | |
| PA11 | | TIM1_CH4<br>TIM1_CH4_1 | | USART1_CTS<br>USART1_CTS_1<br>USART2_TX_2<br>USART2_RX_3 | | | | | CAN_RX | USBDM | | |
| PA12 | | TIM1_BKIN_4 | TIM2_CH1_ETR_5 | USART1_RX_5 | | | I2C1_SDA_2 | SPI1_NSS_2 | CAN_TX | USBDP | | |

| Alternate Pin | ADC | TIM1 | TIM2/3/4 | USART | CMP | SYS | I2C | SPI | CAN | USB | OPA | LPTIM |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | TIM1_BKIN_5<br>TIM1_ETR<br>TIM1_ETR_1 | TIM2_CH1_ETR_7 | USART1_RTS<br>USART1_RTS_1<br>USART2_TX_3<br>USART2_RX_2 | | | | | | | | |
| PA13 | | TIM1_ETR_5<br>TIM1_BKIN_2<br>TIM1_BKIN_3 | | USART1_RTS_2<br>USART1_RTS_4 | | SWDIO | I2C1_SCL_2 | | | | | |
| PA14 | | TIM1_CH3_2<br>TIM1_CH3_3<br>TIM1_CH1N_4<br>TIM1_CH1N_5 | | USART1_CTS_4 | | SWCLK | | | | | | |
| PA15 | | | TIM2_CH1_ETR_1<br>TIM2_CH1_ETR_3 | USART4_RTS_1 | | | | SPI1_NSS_1 | | | | |
| PB0 | ADC_IN8 | TIM1_CH2N_1<br>TIM1_CH2N_2<br>TIM1_CH2N_3 | TIM3_CH3<br>TIM3_CH3_1 | USART4_TX | CMP1_OUT0 | | | | | | OPA_P1<br>OPA_O4 | |
| PB1 | ADC_IN9 | TIM1_CH1_5<br>TIM1_CH4_2<br>TIM1_CH4_3<br>TIM1_CH2N_4<br>TIM1_CH3N_1 | TIM3_CH4<br>TIM3_CH4_1 | USART4_RX | CMP1_N0 | | | | | | OPA_O1 | |
| PB2 | | | | USART4_CK | CMP1_P1 | | BOOT1 | | | | | LPT_OUT_1 |
| PB3 | | | TIM2_CH2_1<br>TIM2_CH2_3 | USART4_CTS | CMP1_N1<br>CMP2_N0<br>CMP3_N0 | | | SPI1_SCK_1 | | | | |
| PB4 | | | TIM3_CH1_1 | USART4_RTS | CMP3_OUT0 | | | SPI1_MISO_1 | | | | |
| PB5 | | | TIM3_CH2_1 | USART4_RX_1 | CMP2_OUT0<br>CMP3_P0 | | I2C1_SMBA<br>I2C1_SMBA_2<br>I2C1_SMBA_3 | SPI1_MOSI_1 | | | | LPT_IN1_1 |
| PB6 | | TIM1_ETR_2<br>TIM1_ETR_4<br>TIM1_CH3_5 | TIM4_CH1 | USART1_TX_1<br>USART1_CK_5 | CMP2_P1 | | I2C1_SCL | SPI1_SCK_2<br>SPI1_SCK_3 | | CC1 | | LPT_ETR_1 |
| PB7 | | TIM1_CH1_4<br>TIM1_CH3N_5 | TIM4_CH2 | USART1_RX_1<br>USART1_CTS_3<br>USART1_CTS_5 | CMP2_N1 | | I2C1_SDA | SPI1_MOSI_2<br>SPI1_MOSI_3 | | CC2 | | LPT_IN2_1 |
| PB8 | | TIM1_CH2_4<br>TIM1_CH2_5 | TIM4_CH3<br>TIM4_CH3_1<br>TIM2_CH2_7 | USART1_RTS_3<br>USART1_RTS_5 | CMP2_P0 | | | SPI1_MISO_2<br>SPI1_MISO_3 | CAN_RX_2 | | | |
| PB9 | | TIM1_CH3N_2<br>TIM1_CH3N_3<br>TIM1_CH3N_4 | TIM4_CH4<br>TIM4_CH4_1 | USART1_RX_4 | | | I2C1_SCL_3 | | CAN_TX_2 | | | |
| PB10 | | | TIM4_CH1_1<br>TIM2_CH3_2<br>TIM2_CH3_3 | USART3_TX | CMP1_OUT1<br>CMP3_P1 | | I2C2_SCL | | | | OPA_N2<br>OPA_N6 | |

| Alternate Pin | ADC | TIM1 | TIM2/3/4 | USART | CMP | SYS | I2C | SPI | CAN | USB | OPA | LPTIM |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PB11 | | TIM1_CH1N_2<br>TIM1_CH1N_3 | TIM2_CH4_2<br>TIM2_CH4_3<br>TIM4_CH2_1 | USART1_TX_4<br>USART3_RX | CMP2_OUT1<br>CMP3_N1 | | I2C1_SDA_3<br>I2C2_SDA | | | | OPA_N0 | |
| PB12 | | TIM1_CH3_4<br>TIM1_BKIN | TIM2_CH3_4<br>TIM2_CH3_5 | USART1_TX_5<br>USART3_CK<br>USART3_CK_2<br>USART3_CK_3 | CMP3_OUT1 | | I2C2_SMBA | SPI1_NSS_3<br>SPI2_NSS | | | | LPT_IN1 |
| PB13 | | TIM1_CH1N | | USART3_CTS<br>USART3_CTS_2<br>USART3_CTS_3 | | | | SPI2_SCK | | | | LPT_IN2 |
| PB14 | | TIM1_CH2N | | USART3_RTS<br>USART3_RTS_2<br>USART3_RTS_3 | | | | SPI2_MISO | | | OPA_P2 | LPT_ETR |
| PB15 | | TIM1_CH3N | | | | | | SPI2_MOSI | | | OPA_P0 | LPT_OUT |
| PC13 | | | | | | RTC TAMPER | | | | | | |
| PC14 | | | | | | OSC32_IN | | | | | | |
| PC15 | | | | | | OSC32_OUT | | | | | | |
| PD0 | | | | USART3_TX_3<br>USART3_RX_2 | | OSC_IN | | | CAN_RX_3 | | | |
| PD1 | | | | USART3_TX_2<br>USART3_RX_3 | | OSC_OUT | | | CAN_TX_3 | | | |

# Chapter 3 Electrical Characteristics

## 3.1 Test Conditions

Unless otherwise specified and indicated, all voltages are referenced to $V_{SS}$.

All minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and clock frequency. Typical values are based on normal temperature (25°C) and $V_{DD} = 3.3V$ environment, which are given only as design guidelines.

The data based on comprehensive evaluation, design simulation or technology characteristics are not tested in production. On the basis of comprehensive evaluation, the minimum and maximum values refer to sample tests. Unless otherwise specified that is tested, the characteristic parameters are guaranteed by comprehensive evaluation or design.

Power supply scheme:

Figure 3-1 Typical circuit for conventional power supply
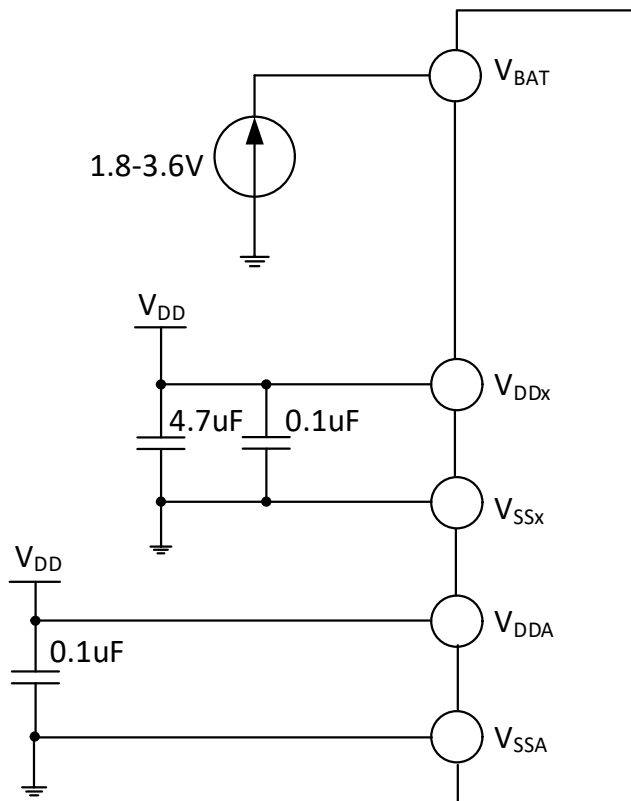


## 3.2 Absolute Maximum Ratings

Critical or exceeding the absolute maximum value may cause the chip to operate improperly or even be damaged.

Table 3-1 Absolute maximum ratings

| Symbol | Description | Min. | Max. | Unit |
|--------|-------------|------|------|------|
| $T_A$ | Ambient temperature during operation | -40 | 85 | °C |
| $T_S$ | Ambient temperature during storage | -40 | 125 | °C |
| $V_{DD}$-$V_{SS}$ | External mains supply voltage (including VDDA and VDD) | -0.3 | 4.0 | V |
| $V_{IN}$ | FT (tolerant 5V) input voltage on pins | $V_{SS}$-0.3 | 5.5 | V |

| | | | | |
|---|---|---|---|---|
| | Voltage on other pins | $V_{SS}$-0.3 | $V_{DD}$+0.3 | V |
| $|\triangle V_{DD\_x}|$ | Voltage difference between each VDD of the main supply pins | | 50 | mV |
| $|\triangle V_{SS\_x}|$ | Voltage difference between different ground pins | | 50 | mV |
| $V_{ESD(HBM)}$ | ESD Electrostatic Discharge Voltage (HBM) on Normal I/O Pins | 4K | | V |
| | ESD voltage (HBM) on USB pins | 4K | | V |
| $I_{VDD}$ | Total current through $V_{DD}$/$V_{DDA}$ power line (supply current) | | 150 | mA |
| $I_{Vss}$ | Total current through $V_{SS}$ ground line (outgoing current) | | 150 | mA |
| $I_{IO}$ | Pour current on arbitrary I/O and control pins | | 25 | mA |
| | Source current on arbitrary I/O and control pins | | -25 | mA |
| $I_{INJ(PIN)}$ | NRST pin injection current | | +/-5 | mA |
| | OSC_IN pin of HSE and OSC_IN pin of LSE injection current | | +/-5 | mA |
| | Injection current on other pins | | +/-5 | mA |
| $\sum I_{INJ(PIN)}$ | Total injection current on all IO and control pins | | +/-25 | mA |

## 3.3 Electrical Characteristics

### 3.3.1 Operating Conditions

Table 3-2 General operating conditions

| Symbol | Parameter | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $F_{HCLK}$ | Internal HB clock frequency | | | 96 | MHz |
| $F_{PCLK1}$ | Internal PB1 clock frequency | | | 96 | MHz |
| $F_{PCLK2}$ | Internal PB2 clock frequency | | | 96 | MHz |
| $V_{DD}$ | Standard operating voltage | | 1.8 | 3.6 | V |
| | | Use USB | 3.0 | 3.6 | |
| $V_{DDA}$ | Operating voltage of the analog section (without ADC) | | 2.0 | 3.6 | V |
| | Operating voltage of the analog section (with ADC) | | 2.4 | 3.6 | |
| $V_{BAT}$[1] | Backup unit operating voltage | No more than $V_{DD}$ | 1.8 | 3.6 | V |
| $T_A$ | Ambient temperature | | -40 | 85 | °C |
| $T_J$ | Junction temperature range | | -40 | 105 | °C |

*Note: 1. The battery to $V_{BAT}$ cable should be as short as possible.*

Table 3-3 Power-on and power-down conditions

| Symbol | Parameter | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $t_{VDD}$ | $V_{DD}$ rising speed | | 0 | ∞ | us/V |
| | $V_{DD}$ falling speed | | 70 | ∞ | |

*Note: 1. The battery to $V_{BAT}$ cable should be as short as possible.*

### 3.3.2 Built-in Reset and Power Control Block Characteristics

Table 3-4 Reset and voltage monitor (For PDR, select high threshold gear)

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{PVD}$[2] | Level selection of programmable voltage detector | PLS[2:0] = 000 (rising edge) | | 1.75 | | V |
| | | PLS[2:0] = 000 (falling edge) | | 1.70 | | V |
| | | PLS[2:0] = 001 (rising edge) | | 1.93 | | V |
| | | PLS[2:0] = 001 (falling edge) | | 1.87 | | V |
| | | PLS[2:0] = 010 (rising edge) | | 2.14 | | V |
| | | PLS[2:0] = 010 (falling edge) | | 2.08 | | V |
| | | PLS[2:0] = 011 (rising edge) | | 2.35 | | V |
| | | PLS[2:0] = 011 (falling edge) | | 2.28 | | V |
| | | PLS[2:0] = 100 (rising edge) | | 2.54 | | V |
| | | PLS[2:0] = 100 (falling edge) | | 2.46 | | V |
| | | PLS[2:0] = 101 (rising edge) | | 2.72 | | V |
| | | PLS[2:0] = 101 (falling edge) | | 2.63 | | V |
| | | PLS[2:0] = 110 (rising edge) | | 2.92 | | V |
| | | PLS[2:0] = 110 (falling edge) | | 2.83 | | V |
| | | PLS[2:0] = 111 (rising edge) | | 3.1 | | V |
| | | PLS[2:0] = 111 (falling edge) | | 3.01 | | V |
| $V_{PVDhyst}$[1] | PVD hysteresis | | 0.05 | 0.08 | 0.1 | V |
| $V_{POR/PDR}$[1] | Power-on/power-down reset threshold | Rising edge | 1.44 | 1.54 | 1.70 | V |
| | | Falling edge | 1.42 | 1.53 | 1.68 | V |
| $V_{PDRhyst}$[1] | PDR hysteresis | | | 10 | 20 | mV |
| $t_{RSTTEMPO}$ | Reset duration | | 6 | 6.5 | 30 | ms |

*Note: 1. Design parameters;*

*2. Normal temperature test value.*

### 3.3.3 Embedded Reference Voltage

Table 3-5 Embedded reference voltage

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{REFINT}$ | Built-in reference voltage | $T_A = -40°C \sim 85°C$ | 1.17 | 1.2 | 1.23 | V |
| $T_{S\_vrefint}$ | ADC sampling time when reading the internal reference voltage | Slow sampling recommended | | | 20 | us |

### 3.3.4 Supply Current Characteristics

Current consumption is a comprehensive index of a variety of parameters and factors. These parameters and factors include operating voltage, ambient temperature, I/O pin load, software configuration of the product, the operating frequency, flip rate of the I/O pin, the location of the program in memory and the executed code, etc. The current consumption measurement method is as follows:

Figure 3-2 Current consumption measurement
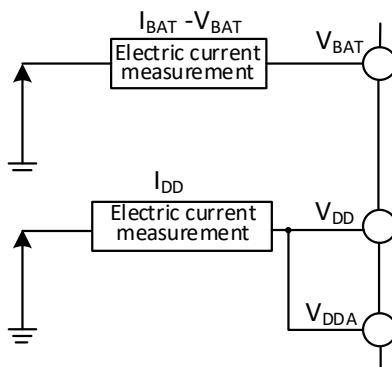


The microcontroller is in the following conditions:

Tested with room temperature VDD = 3.3V: Bit CC1_PD of R16_PORT_CC1 and Bit CC2_PD of R16_PORT_CC2 are both = 1, PB6/CC1 and PB7/CC2 pins are configured as non-pull-down inputs, and all other I/O pins are configured as pull-down inputs running on the high-speed internal RC oscillator HSI with HSI = 8M. $F_{PLCK1}$=$F_{HCLK}$/2 and $F_{PLCK2}$=$F_{HCLK}$ to enable or disable the power consumption of all peripheral clocks.

Table 3-6 Data Processing Code Running from FLASH, Setting LDOTRIM[1:0]=10, LDO_EC=0

| Symbol | Parameter | Condition | | | Typ. | | Unit |
|---|---|---|---|---|---|---|---|
| | | HSILP | PLLON | $F_{HCLK}$ | Enable all peripherals | Disable all peripherals | |
| $I_{DD}$[1] | Supply current in Run mode | 0 | 1 | 96MHz | 7.46 | 4.70 | mA |
| | | 0 | 1 | 48MHz | 5.13 | 3.77 | |
| | | 0 | 1 | 8MHz | 2.23 | 1.95 | |
| | | 0 | 1 | 1MHz | 1.46 | 1.43 | |
| | | 1 | 1 | 1MHz | 1.27 | 1.24 | |
| | | 0 | 0 | 8MHz | 2.14 | 1.87 | |
| | | 0 | 0 | 1MHz | 1.37 | 1.34 | |
| | | 1 | 0 | 1MHz | 1.19 | 1.17 | |
| | Supply current in sleep mode (when peripherals are powered and clock is held) | 0 | 1 | 96MHz | 5.58 | 2.82 | mA |
| | | 0 | 1 | 48MHz | 3.52 | 2.14 | |
| | | 0 | 1 | 8MHz | 1.74 | 1.47 | |
| | | 0 | 1 | 1MHz | 1.40 | 1.37 | |
| | | 1 | 1 | 1MHz | 1.21 | 1.18 | |
| | | 0 | 0 | 8MHz | 1.65 | 1.38 | |
| | | 0 | 0 | 1MHz | 1.31 | 1.28 | |
| | | 1 | 0 | 1MHz | 1.13 | 1.10 | |

*Note: 1. The above are measured parameters.*

*2. When CC1_PD and CC2_PD = 1 and the PB6/CC1 and PB7/CC2 pins are configured as pull-down inputs, the current consumption will be approximately 5uA in addition to the table above.*

Table 3-7-1 Data processing code runs from SRAM, FLASH enters low-power mode(1), Set LDOTRIM[1:0]=10

| Symbol | Parameter | Condition | | | Typ. | | Unit |
|---|---|---|---|---|---|---|---|
| | | HSILP | PLLON | $F_{HCLK}$[3] | Enable all peripherals | Disable all peripherals | |
| $I_{DD}$[2] | Supply current in Run mode | 0 | 1 | 96MHz | 7.08 | 4.29 | mA |
| | | 0 | 1 | 48MHz | 3.77 | 2.37 | |
| | | 0 | 1 | 8MHz | 0.91 | 0.63 | |
| | | 0 | 1 | 1MHz | 0.40 | 0.37 | |
| | | 1 | 1 | 8MHz | 0.68 | 0.46 | |
| | | 1 | 1 | 1MHz | 0.21 | 0.17 | |
| | | 0 | 0 | 8MHz | 0.83 | 0.56 | |
| | | 0 | 0 | 1MHz | 0.31 | 0.28 | |
| | | 1 | 0 | 1MHz | 0.13 | 0.10 | |
| | | 1 | 0 | 500KHz | 0.10 | 0.08 | |
| | | 1 | 0 | 125KHz | 0.07 | 0.07 | |
| | Supply current in sleep mode (when peripherals are powered and clock is held) | 0 | 1 | 96MHz | 4.60 | 1.81 | mA |
| | | 0 | 1 | 48MHz | 2.52 | 1.13 | |
| | | 0 | 1 | 8MHz | 0.72 | 0.44 | |
| | | 0 | 1 | 1MHz | 0.38 | 0.34 | |
| | | 1 | 1 | 8MHz | 0.48 | 0.25 | |
| | | 1 | 1 | 1MHz | 0.18 | 0.15 | |
| | | 0 | 0 | 8MHz | 0.63 | 0.35 | |
| | | 0 | 0 | 1MHz | 0.28 | 0.26 | |
| | | 1 | 0 | 1MHz | 0.11 | 0.07 | |
| | | 1 | 0 | 500KHz | 0.08 | 0.07 | |
| | | 1 | 0 | 125KHz | 0.07 | 0.06 | |

*Note: 1. When FLASH_LP_REG=1 and FLASH_LP=1, FLASH enters low-power mode.*

*2. The above are measured parameters.*

*3. When FHCLK exceeds 16MHz, set LDO_EC=0, otherwise set LDO_EC=1 by default.*

*4. When CC1_PD and CC2_PD = 1 and the PB6/CC1 and PB7/CC2 pins are configured as pull-down inputs, the current consumption will be approximately 5uA in addition to the table above.*

Table 3-7-2 Data processing code runs from SRAM, FLASH does not enter low-power mode(1), set LDOTRIM[1:0]=10

| Symbol | Parameter | Condition | | | Typ. | | Unit |
|---|---|---|---|---|---|---|---|
| | | HSILP | PLLON | $F_{HCLK}$[3] | Enable all peripherals | Disable all peripherals | |
| $I_{DD}$[2] | Supply current in Run mode | 0 | 1 | 96MHz | 7.87 | 5.09 | mA |
| | | 0 | 1 | 48MHz | 4.68 | 3.28 | |
| | | 0 | 1 | 8MHz | 1.97 | 1.69 | |
| | | 0 | 1 | 1MHz | 1.44 | 1.40 | |
| | | 1 | 1 | 8MHz | 1.71 | 1.47 | |
| | | 1 | 1 | 1MHz | 1.23 | 1.20 | |

| | | 0 | 0 | 8MHz | 1.85 | 1.57 | |
|---|---|---|---|---|---|---|---|
| | | 0 | 0 | 1MHz | 1.34 | 1.31 | |
| | | 1 | 0 | 1MHz | 1.16 | 1.13 | |
| | Supply current in sleep mode (when peripherals are powered and clock is held) | 0 | 1 | 96MHz | 5.64 | 2.84 | mA |
| | | 0 | 1 | 48MHz | 3.56 | 2.16 | |
| | | 0 | 1 | 8MHz | 1.75 | 1.48 | |
| | | 0 | 1 | 1MHz | 1.41 | 1.38 | |
| | | 1 | 1 | 8MHz | 1.51 | 1.28 | |
| | | 1 | 1 | 1MHz | 1.21 | 1.18 | |
| | | 0 | 0 | 8MHz | 1.66 | 1.39 | |
| | | 0 | 0 | 1MHz | 1.32 | 1.29 | |
| | | 1 | 0 | 1MHz | 1.14 | 1.11 | |

*Note: 1. When FLASH_LP_REG=0, FLASH does not enter low-power mode.*

*2. The above are measured parameters.*

*3. When FHCLK exceeds 16MHz, set LDO_EC=0, otherwise set LDO_EC=1 by default.*

*4. When CC1_PD and CC2_PD = 1, and PB6/CC1 and PB7/CC2 pins are configured as pull-down inputs, the current consumption will be about 5uA in addition to the above table.*

Table 3-7-3 Data processing code runs from SRAM, FLASH enters low-power mode(1), Setting LDOTRIM[1:0]=01

| Symbol | Parameter | Condition | | | Typ. | | Unit |
|---|---|---|---|---|---|---|---|
| | | HSILP | PLLON | $F_{HCLK}$(3) | Enable all peripherals | Disable all peripherals | |
| $I_{DD}$(2) | Supply current in Run mode | 0 | 1 | 96MHz | 6.32 | 3.78 | mA |
| | | 0 | 1 | 48MHz | 3.41 | 2.11 | |
| | | 0 | 1 | 8MHz | 0.86 | 0.60 | |
| | | 0 | 1 | 1MHz | 0.39 | 0.36 | |
| | | 1 | 1 | 8MHz | 0.63 | 0.42 | |
| | | 1 | 1 | 1MHz | 0.20 | 0.16 | |
| | | 0 | 0 | 8MHz | 0.76 | 0.52 | |
| | | 0 | 0 | 1MHz | 0.30 | 0.27 | |
| | | 1 | 0 | 1MHz | 0.13 | 0.09 | |
| | | 1 | 0 | 500KHz | 0.09 | 0.08 | |
| | | 1 | 0 | 125KHz | 0.07 | 0.06 | |
| | Supply current in sleep mode (when peripherals are powered and clock is held) | 0 | 1 | 96MHz | 4.22 | 1.67 | mA |
| | | 0 | 1 | 48MHz | 2.33 | 1.05 | |
| | | 0 | 1 | 8MHz | 0.68 | 0.42 | |
| | | 0 | 1 | 1MHz | 0.37 | 0.34 | |
| | | 1 | 1 | 8MHz | 0.45 | 0.24 | |
| | | 1 | 1 | 1MHz | 0.17 | 0.14 | |
| | | 0 | 0 | 8MHz | 0.59 | 0.34 | |
| | | 0 | 0 | 1MHz | 0.27 | 0.25 | |
| | | 1 | 0 | 1MHz | 0.10 | 0.07 | |

| | | 1 | 0 | 500KHz | 0.08 | 0.06 | |
| | | 1 | 0 | 125KHz | 0.06 | 0.06 | |

*Note: 1. When FLASH_LP_REG=1 and FLASH_LP=1, FLASH enters low-power mode.*

*2. The above are measured parameters.*

*3. When FHCLK exceeds 16MHz, set LDO_EC=0, otherwise set LDO_EC=1 by default.*

*4. When CC1_PD and CC2_PD = 1 and the PB6/CC1 and PB7/CC2 pins are configured as pull-down inputs, the current consumption will be approximately 5uA in addition to the table above.*

Table 3-8-1 Data processing code runs from FLASH, typical current consumption in Stop and Standby mode

| Symbol | Parameter | Condition | | | | | | | | Typ. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | HIS, HSE, LSI, LSE | RAMLV | R18KS TY | R2KS TY | LDO_ EC | LPDS | PDDS | LDO | | |
| $I_{DD}$ | Supply current in STOP mode1 | All disabled | Invalid | Invalid | Invalid | 0 | 0 | 0 | 10 | 34.63 | uA |
| | Supply current in STOP mode2 | All disabled | Invalid | Invalid | Invalid | 1 | 0 | 0 | 10 | 23.88 | |
| | Supply current in STOP mode3 | All disabled | 0 | Invalid | Invalid | X | 1 | 0 | 10 | 4.55 | |
| | Supply current in STOP mode4 | All disabled | 1 | Invalid | Invalid | X | 1 | 0 | 10 | 4.08 | |
| | Supply current in STANDBY mode | Only enable LSI | 0 | 1 | 1 | Invalid | Invalid | 1 | 10 | 2.97 | uA |
| | | All disabled | 0 | 1 | 1 | Invalid | Invalid | 1 | 10 | 2.82 | |
| | | All disabled | 1 | 1 | 1 | Invalid | Invalid | 1 | 10 | 1.89 | |
| | | Only enable LSI | 1 | 0 | 1 | Invalid | Invalid | 1 | 10 | 0.74 | |
| | | All disabled | 1 | 0 | 1 | Invalid | Invalid | 1 | 10 | 0.59 | |
| | | Only enable LSI | Invalid | 0 | 0 | Invalid | Invalid | 1 | 10 | 0.51 | |
| | | All disabled | Invalid | 0 | 0 | Invalid | Invalid | 1 | 10 | 0.37 | |
| $I_{DD\_VBAT}$ | Supply current for backup domain (Remove $V_{DD}$ and $V_{DDA}$ and use only $V_{BAT}$ supply) | Only enable LSE | Invalid | 0 | 0 | Invalid | Invalid | 1 | 10 | 0.75 | uA |
| | | All disabled | Invalid | 0 | 0 | Invalid | Invalid | 1 | 10 | 0.37 | |

*Note: 1. The above are measured parameters.*

*2. When CC1_PD and CC2_PD = 1 and the PB6/CC1 and PB7/CC2 pins are configured as pull-down inputs,*

*the current consumption in the stop mode will be about 5uA in addition to the above table.*

*3. CH32L103K8U6 and F8U6 have a built-in 5.1kΩ pull-down resistor. Since the function of the 5.1kΩ pull-down resistor is forced to be turned on in standby mode, there is no need to configure in Note 2, and the current consumption of the CH32L103K8U6 and F8U6 chips in standby mode will be about 5uA in addition to the above table.*

Table 3-8-2 Data processing code runs from FLASH, typical current consumption in Stop mode

| Symbol | Parameter | 条件 | | | | | | | | Typ. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | HIS, HSE LSI, LSE | RAMLV | R18KSTY | R2KSTY | LDO_EC | LPDS | PDDS | LDO | | |
| $I_{DD}$ | Supply current in STOP mode1 | All disabled | Invalid | Invalid | Invalid | 0 | 0 | 0 | 01 | 30.94 | uA |
| | Supply current in STOP mode2 | All disabled | Invalid | Invalid | Invalid | 1 | 0 | 0 | 01 | 20.22 | |

*Note: 1. The above are measured parameters.*

*2. When CC1_PD and CC2_PD = 1 and the PB6/CC1 and PB7/CC2 pins are configured as pull-down inputs, the current consumption in the stop mode will be approximately 5uA in addition to the above table.*

### 3.3.5 External Clock Source Characteristics

Table 3-9 From external high-speed clock

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $F_{HSE\_ext}$ | External clock frequency | | 3 | 8 | 25 | MHz |
| $V_{HSEH}$[1] | OSC_IN input pin high level voltage | | $0.8V_{DD}$ | | $V_{DD}$ | V |
| $V_{HSEL}$[1] | OSC_IN input pin low level voltage | | 0 | | $0.2V_{DD}$ | V |
| $C_{in(HSE)}$ | OSC_IN input capacitance | | | 5 | | pF |
| $DuCy_{HSE}$ | Duty Cycle | | | 50 | | % |
| $I_L$ | OSC_IN input leakage current | | | | ±1 | uA |

*Note 1: Failure to meet this condition may cause a level recognition error.*

Figure 3-3 Low frequency clock circuit for external clock source
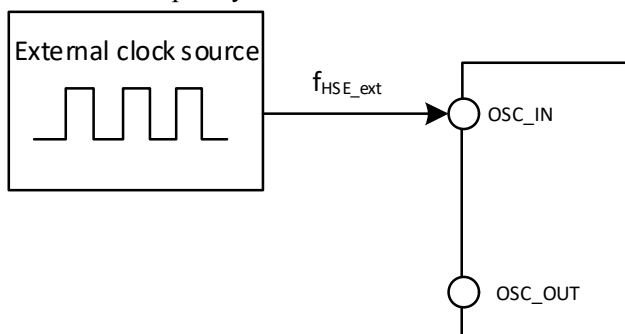
Table 3-10 From external low-speed clock

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|--------|-----------|-----------|------|------|------|------|
| $F_{LSE\_ext}$ | User external clock frequency | | | 32.768 | 1000 | KHz |
| $V_{LSEH}$ | OSC32_IN input pin high level voltage | | $0.8V_{DD}$ | | $V_{DD}$ | V |
| $V_{LSEL}$ | OSC32_IN input pin low voltage | | 0 | | $0.2V_{DD}$ | V |
| $C_{in(LSE)}$ | OSC32_IN input capacitance | | | 5 | | pF |
| $DuCy_{LSE}$ | Duty cycle | | | 50 | | % |
| $I_L$ | OSC32_IN input leakage current | | | | ±1 | uA |

Figure 3-4 Low frequency clock circuit for external clock source
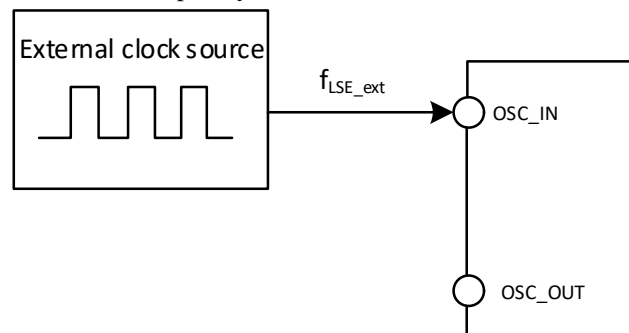


Table 3-11 High-Speed external clocks generated using one crystal/ceramic resonator

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|--------|-----------|-----------|------|------|------|------|
| $F_{OSC\_IN}$ | Resonator frequency | | 3 | 8 | 25 | MHz |
| $R_F$ | Feedback resistance | | | 250 | | kΩ |
| C | Suggested load capacitance with corresponding crystal serial impedance $R_S$ | $R_S$=60Ω[1] | | 20 | | pF |
| $I_2$[1] | HSE drive current | $V_{DD}$ = 3.3V，20p load | | 1 | | mA |
| | | Low-power, $V_{DD}$ = 3.3V, 20p load | | 0.55 | | mA |
| $g_m$[1] | Oscillator transconductance | Startup | | 21 | | mA/V |
| $t_{SU(HSE)}$ | Startup time | $V_{DD}$ stabilization | | 1.5[2] | 4.5 | ms |

*Note: 1. 25M crystal ESR is recommended not to exceed 60 ohms, below 25M can be relaxed appropriately.*

*2. Start-up time refers to the time difference from when HSEON is turned on to when HSERDY is set.*

Circuit reference design and requirements:

The load capacitance of the crystal is based on the crystal manufacturer's recommendation, usually CL1=CL2.

Figure 3-5 Typical circuit for external 8M crystal
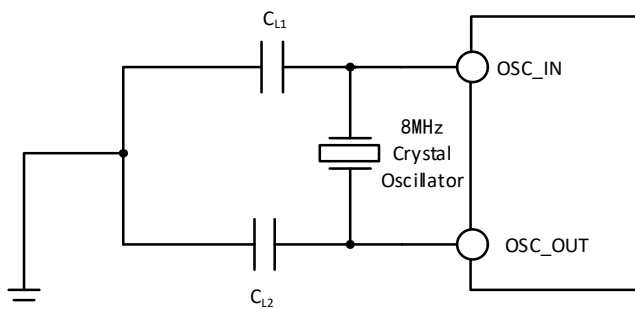


Table 3-12 Low-speed external clocks generated using a crystal/ceramic resonator ($f_{LSE}$=32.768KHz)

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $R_F$ | Feedback resistance | | | 5 | | MΩ |
| $C_{L1}/C_{L2}$ | Suggested load capacitance with corresponding crystal serial impedance $R_S$ | $R_S$ = 70KΩ | | | 15 | pF |
| $i_2$[1] | LSE drive current | $V_{DD}$ = 3.3V | | 0.36 | | uA |
| $g_m$[1] | Oscillator transconductance | Startup | | 26 | | uA/V |
| $t_{SU(LSE)}$ | Startup time | $V_{DD}$ stabilization | | 1000[1] | | ms |

*Note: The startup time is the time difference between when LSEON is turned on and when LSERDY is set.*

Circuit reference design and requirements:

The load capacitance of the crystal is based on the crystal manufacturer's recommendation, usually CL1=CL2, optional about 12pF.

Figure 3-6 Typical Circuit for External 32.768K Crystal
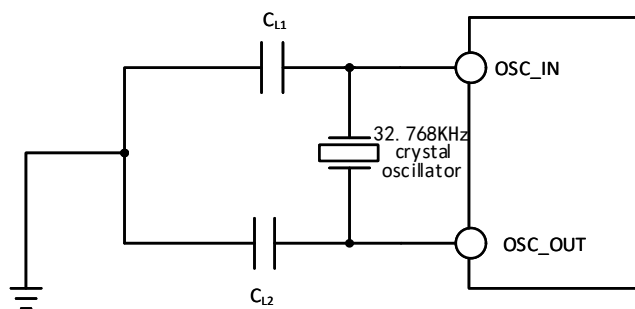


*Note: The load capacitance CL is calculated by the following formula: CL = CL1 × CL2 / (CL1 + CL2) + Cstray, where $C_{stray}$ is the capacitance of the pins and the capacitance associated with the PCB board or PCB, and its typical value is between 2pF and 7pF.*

### 3.3.6 Internal Clock Source Characteristics

Table 3-13 Internal High-Speed (HSI) RC Oscillator Characteristics

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $F_{HSI}$ | Frequency (after calibration) | | | 8 | | MHz |
| | | Low-power mode | 0.9 | 1 | 1.1 | MHz |
| $DuCy_{HSI}$ | Duty cycle | | 45 | 50 | 55 | % |

| | | | | | | |
|---|---|---|---|---|---|---|
| ACC$_{HSI}$ | Accuracy of HSI oscillator (after calibration) | T$_A$ = 0°C~70°C | -1.8 | | 1.8 | % |
| | | T$_A$ = -40°C~85°C | -3 | | 2.5 | % |
| t$_{SU(HSI)}$ | HSI oscillator startup stabilization time | | | | 8 | us |
| I$_{DD(HSI)}$ | HSI oscillator power consumption | | | 200 | | uA |
| | | Low-power mode | | 24 | | uA |

Table 3-14 Internal Low-Speed (LSI) RC Oscillator Characteristics

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| F$_{LSI}$ | Frequency | | 27 | 37 | 47 | KHz |
| DuCy$_{LSI}$ | Duty cycle | | 45 | 50 | 55 | % |
| t$_{SU(LSI)}$ | LSI oscillator startup stabilization time | | | 400 | | us |
| I$_{DD(LSI)}$ | LSI oscillator power consumption | | | 280 | | nA |

### 3.3.7 PLL Characteristics

Table 3-15 PLL Characteristics

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| F$_{PLL\_IN}$ | PLL input clock | | 3 | 8 | 25 | MHz |
| | PLL input clock duty cycle | | 40 | | 60 | % |
| F$_{PLL\_OUT}$ | PLL multiplier output clock | | 18 | | 96[1] | MHz |
| t$_{LOCK}$ | PLL lock time | | | 80 | 200 | us |
| I$_{DD(PLL)}$ | PLL power consumption | Input frequency 8M, Output frequency 96M | | 0.15 | | mA |

*Note 1: The appropriate multiplier frequency must be selected to meet the PLL output frequency range.*

### 3.3.8 Wakeup Time from Low-power Mode

Table 3-16 Wakeup time from low-power mode[1]

| Symbol | Parameter | Condition | Typ. | Unit |
|---|---|---|---|---|
| t$_{wusleep}$ | Wakeup from Sleep mode | Wake up using HSI RC clock | 0.2 | us |
| t$_{wustop}$ | Wakeup from Stop mode | Wake up using HSI RC clock | 7 | us |
| t$_{WUSTDBY}$ | Wakeup from Standby mode | Wake up using HSI RC clock | 72 | us |

*Note: The above are measured parameters.*

### 3.3.9 Memory Characteristics

Table 3-17 Flash memory characteristics

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| t$_{prog\_page}$ | Page (256 bytes) programming time | | | 2.0 | 2.5 | ms |
| t$_{erase\_page}$ | Page (256 bytes) erase time | | | 6.2 | 7.5 | ms |
| t$_{erase\_sec}$ | Sector (1K bytes) erase time | | | 6.2 | 7.5 | ms |

Table 3-18 Flash memory endurance and data retention

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|--------|-----------|-----------|------|------|------|------|
| $N_{END}$ | Endurance | $T_A = 25°C$ | 100K | | | Times |
| $t_{RET}$ | Data retention period | | 10 | | | Years |

## 3.3.10 I/O Port Characteristics

Table 3-19 General-purpose I/O static characteristics

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|--------|-----------|-----------|------|------|------|------|
| $V_{IH}$ | Standard I/O pin, input high-level voltage | | $0.41*(V_{DD}-1.8)+1.3$ | | $V_{DD}+0.3$ | V |
| | FT IO pin, input high-level voltage | | $0.42*(V_{DD}-1.8)+1.2$ | | 5.5 | V |
| $V_{IL}$ | Standard I/O pin, input low-level voltage | | -0.3 | | $0.28*(V_{DD}-1.8)+0.6$ | V |
| | FT IO pin, input low-level voltage | | -0.3 | | $0.32*(V_{DD}-1.8)+0.55$ | V |
| $V_{hys}$ | Standard I/O pin Schmitt trigger voltage hysteresis | | 150 | | | mV |
| | FT I/O Schmitt trigger voltage hysteresis | | 90 | | | mV |
| $I_{lkg}$ | Standard I/O pin input leakage current | | | | 1 | uA |
| | FT I/O pin input leakage current | | | | 3 | uA |
| $R_{PU}$ | Pull-up equivalent group | | 30 | 40 | 50 | kΩ |
| $R_{PD}$ | Pull-down equivalent group | | 30 | 40 | 50 | kΩ |
| $C_{IO}$ | I/O pin capacitor | | | 5 | | pF |

*Note: The above are guaranteed design parameters.*

Output Drive Current Characteristics

The GPIOs (General-purpose Input/Output Ports) can absorb or output up to ±8mA of current and absorb or output ±20mA of current (not strictly up to $V_{OL}/V_{OH}$). In user applications, the total current driven by all IO pins must not exceed the absolute maximum ratings given in section 3.2:

Table 3-20 Output voltage characteristics

| Symbol | Parameter | Condition | Min. | Max. | Unit |
|--------|-----------|-----------|------|------|------|
| $V_{OL}$ | Output low, 8 pins absorb current | TTL port, $I_{IO} = +8mA$ $2.7V< V_{DD} <3.6V$ | | 0.4 | V |
| $V_{OH}$ | Output high, 8 pins absorb current | | $V_{DD}-0.4$ | | |
| $V_{OL}$ | Output low, 8 pins absorb current | CMOS port, $I_{IO} = +8mA$ $2.7V< V_{DD} <3.6V$ | | 0.4 | V |
| $V_{OH}$ | Output high, 8 pins absorb current | | $V_{DD}-0.4$ | | |
| $V_{OL}$ | Output low, 8 pins absorb current | $I_{IO} = +20mA$ $2.7V< V_{DD} <3.6V$ | | 0.8 | V |
| $V_{OH}$ | Output high, 8 pins absorb current | | $V_{DD}-$ | | |

| | | | 1.2 | | |
|---|---|---|---|---|---|
| $V_{OL}$ | Output low, 8 pins absorb current | $I_{IO}$ = +6mA<br>2.4V< $V_{DD}$ <2.7V | | 0.8 | V |
| $V_{OH}$ | Output high, 8 pins absorb current | | $V_{DD}$-1.2 | | |

*Note: If more than one IO pin is driven at the same time in the above conditions, the sum of the currents must not exceed the absolute maximum ratings given in section 3.2. Also when multiple IO pins are driven at the same time, the high current at the power/ground point can cause a voltage drop that prevents the voltage of the internal IOs from reaching the supply voltage in the table, which results in a drive current that is less than the nominal value.*

Table 3-21 Input/Output AC Characteristics

| MODEx[1:0] configuration | Symbol | Parameter | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| 10 （2MHz） | $F_{max(IO)out}$ | Maximum Frequency | CL=50pF, $V_{DD}$=2.7-3.6V | | 2 | MHz |
| | $t_{f(IO)out}$ | Output high-to-low level fall time | CL=50pF, $V_{DD}$=2.7-3.6V | | 125 | ns |
| | $t_{r(IO)out}$ | Output low-to-high rise time | | | 125 | ns |
| 01 （10MHz） | $F_{max(IO)out}$ | Maximum Frequency | CL=50pF, $V_{DD}$=2.7-3.6V | | 10 | MHz |
| | $t_{f(IO)out}$ | Output high-to-low level fall time | CL=50pF, $V_{DD}$=2.7-3.6V | | 25 | ns |
| | $t_{r(IO)out}$ | Output low-to-high rise time | | | 25 | ns |
| 11 （50MHz） | $F_{max(IO)out}$ | Maximum Frequency | CL=30pF, $V_{DD}$=2.7-3.6V | | 50 | MHz |
| | | | CL=50pF, $V_{DD}$=2.7-3.6V | | 30 | MHz |
| | $t_{f(IO)out}$ | Output low-to-high rise time Maximum Frequency | CL=30pF, $V_{DD}$=2.7-3.6V | | 5 | ns |
| | | | CL=50pF, $V_{DD}$=2.7-3.6V | | 8 | ns |
| | $t_{r(IO)out}$ | Output high-to-low level fall time | CL=30pF, $V_{DD}$=2.7-3.6V | | 5 | ns |
| | | | CL=50pF, $V_{DD}$=2.7-3.6V | | 8 | ns |
| | $t_{EXTIpw}$ | EXTI controller detects the pulse width of the external signal | | 10 | | ns |

## 3.3.11 NRST Pin Characteristics

Table 3-22 External reset pin characteristics

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{IL(NRST)}$ | NRST input low level voltage | | -0.3 | | 0.28*($V_{DD}$-1.8)+0.6 | V |
| $V_{IH(NRST)}$ | NRST input high level voltage | | 0.41*($V_{DD}$-1.8)+1.3 | | $V_{DD}$+0.3 | V |
| $V_{hys(NRST)}$ | NRST Schmitt trigger voltage hysteresis | | 150 | | | mV |
| $R_{PU}$[1] | Pull-up equivalent resistance | | 30 | 40 | 50 | kΩ |
| $V_{F(NRST)}$ | NRST input can be filtered | | | | 100 | ns |

| | for pulse width | | | | | |
|---|---|---|---|---|---|---|
| $V_{NF(NRST)}$ | NRST input cannot be filtered pulse width | | 300 | | | ns |

*Note: 1. The pull-up resistor is a real resistor in series with a switchable PMOS implementation. The resistance of this PMOS/NMOS switch is very small (about 10%).*

Circuit reference design and requirements:

Figure 3-7 Typical circuit of external reset pin
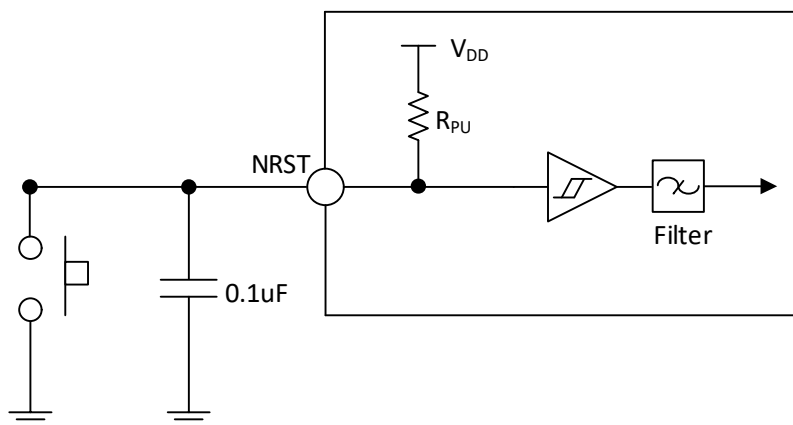


*Note: The capacitors shown are optional and can be used to filter out key jitter.*

## 3.3.12 USB PD Interface Characteristics

Table 3-23-1 PD interface I/O characteristics

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| tRise | Rising time | The time between 10% and 90% of the range, with the minimum value being the time under no-load conditions. | 240 | 400 | | ns |
| tFall | Falling time | The time between 10% and 90% of the range, with the minimum value being the time under no-load conditions. | 240 | 400 | | ns |
| $V_{Swing}$ | Output voltage swing (Peak-to-peak) | | 1.04 | 1.12 | 1.20 | V |
| $Z_{Driver}$ | Output impedance | | 26 | | 90 | $\Omega$ |

Table 3-23-2 Type-C I/O characteristics

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| | | | | 80 | | uA |
| $I_{pu}$ | Pull-up current | PAD < $V_{DD}$-0.6V | | 180 | | uA |
| | | | | 330 | | uA |
| Rd | Pull-down current | $V_{DD} \geq$ 1.6V or external pull-up 330uA | 4.08 | 5.1 | 6.12 | k$\Omega$ |

### 3.3.13 TIM Timer Characteristics

Table 3-24 TIMx characteristics

| Symbol | Parameter | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $t_{res(TIM)}$ | Timer reference clock | | 1 | | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK}$ = 48MHz | 20.8 | | ns |
| $F_{EXT}$ | Timer external clock frequency on CH1 to CH4 | | 0 | $f_{TIMxCLK}/2$ | MHz |
| | | $f_{TIMxCLK}$ = 48MHz | 0 | 24 | MHz |
| $R_{esTIM}$ | Timer resolution | | | 16 | Bit |
| $t_{COUNTER}$ | 16-bit counter clock cycle when the internal clock is selected | | 1 | 65536 | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK}$ = 48MHz | 0.02 | 1363 | us |
| $t_{MAX\_COUNT}$ | Maximum possible count | | | 65535 | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK}$ = 48MHz | | 1363 | us |

### 3.3.14 I2C Interface Characteristics

Figure 3-8 I2C bus timing diagram
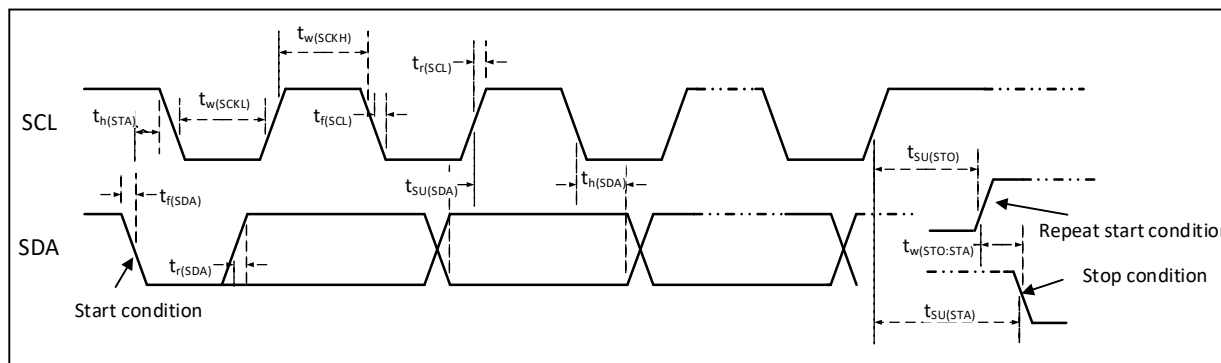


Table 3-25 I2C interface characteristics

| Symbol | Parameter | Standard I2C | | Fast I2C | | Unit |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| $t_{w(SCKL)}$ | SCL clock low level time | 4.7 | | 1.2 | | us |
| $t_{w(SCKH)}$ | SCL clock high level time | 4.0 | | 0.6 | | us |
| $t_{SU(SDA)}$ | SDA data setup time | 250 | | 100 | | ns |
| $t_{h(SDA)}$ | SDA data hold time | 0 | | 0 | 900 | ns |
| $t_{r(SDA)}/t_{r(SCL)}$ | SDA and SCL rise time | | 1000 | 20 | | ns |
| $t_{f(SDA)}/t_{f(SCL)}$ | SDA and SCL fall time | | 300 | | | ns |
| $t_{h(STA)}$ | Start condition hold time | 4.0 | | 0.6 | | us |
| $t_{SU(STA)}$ | Repeated start condition setup time | 4.7 | | 0.6 | | us |
| $t_{SU(STO)}$ | Stop condition setup time | 4.0 | | 0.6 | | us |
| $t_{w(STO:STA)}$ | Time from stop condition to start condition | 4.7 | | 1.2 | | us |

| | (bus free) | | | | | |
|---|---|---|---|---|---|---|
| $C_b$ | Capacitive load for each bus | | 400 | | 400 | pF |

### 3.3.15 SPI Interface Characteristics

Figure 3-9 SPI timing diagram in Master mode


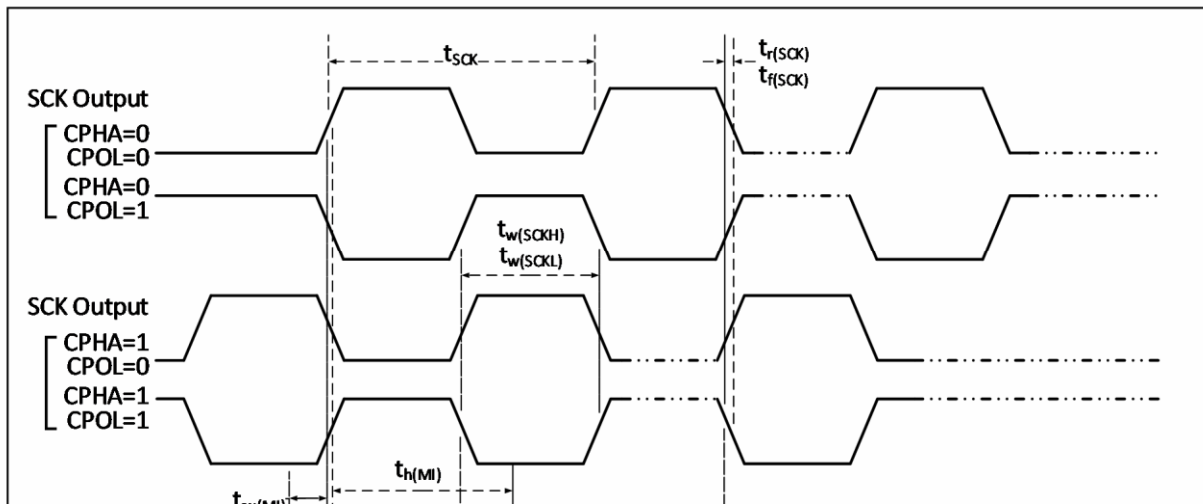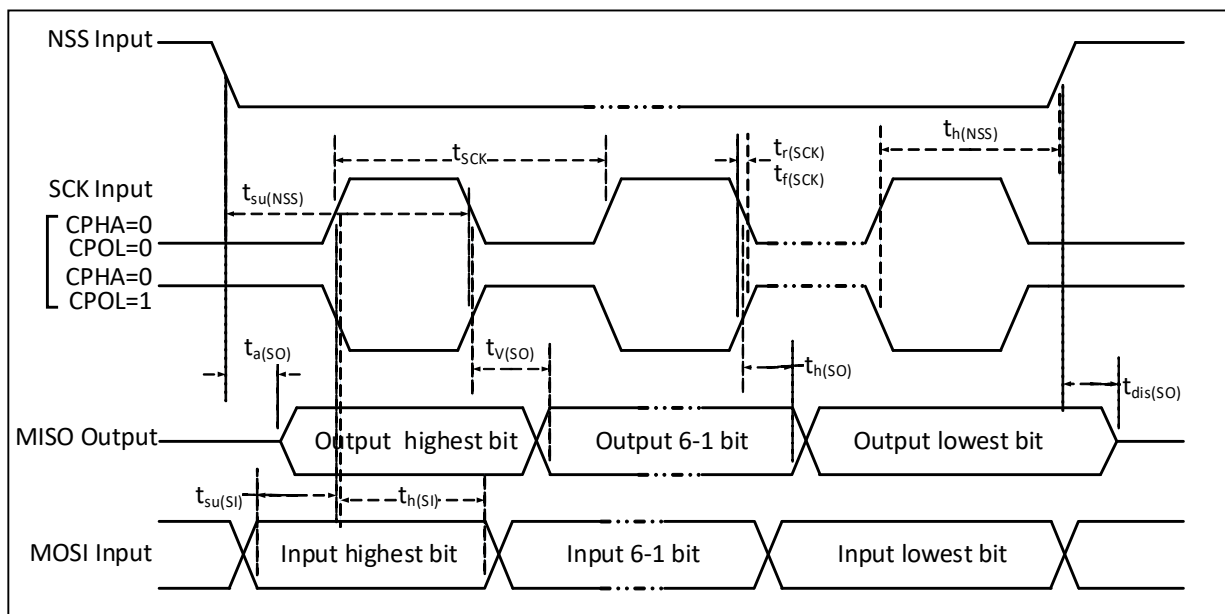
Figure 3-10 SPI timing diagram in Slave mode (CPHA=0)

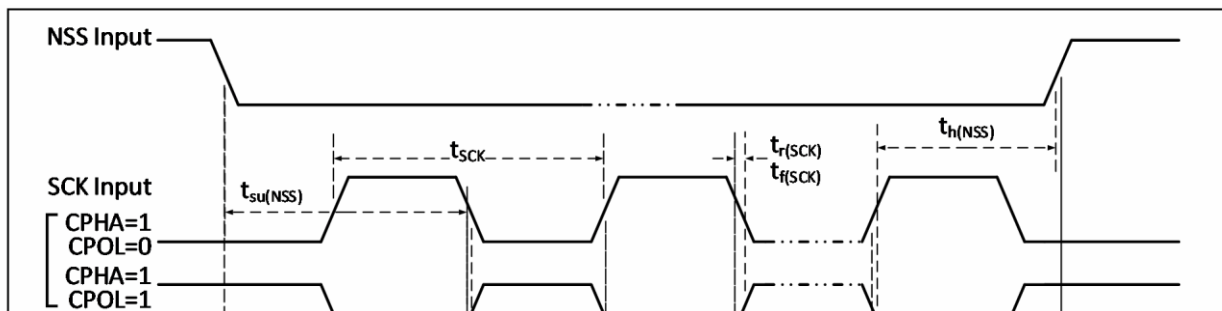Figure 3-11 SPI timing diagram in Slave mode (CPHA=1)



Table 3-26 SPI interface characteristics

| Symbol | Parameter | Condition | | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| $f_{SCK}/t_{SCK}$ | SPI clock frequency | Master mode | | | 32 | MHz |
| | | Slave mode | | | 32 | MHz |
| $t_{r(SCK)}/t_{f(SCK)}$ | SPI clock rise and fall time | Load capacitance: C = 30pF | | | 8 | ns |
| $t_{SU(NSS)}$ | NSS setup time | Slave mode | | $2t_{HCLK}$ | | ns |
| $t_{h(NSS)}$ | NSS hold time | Slave mode | | $2t_{HCLK}$ | | ns |
| $t_{w(SCKH)}/t_{w(SCKL)}$ | SCK high-level and low-level time | Master mode, $f_{PCLK}$ = 24MHz, Prescaler factor = 4 | | 70 | 97 | ns |
| $t_{SU(MI)}$ | Data input setup time | Master mode | HSRXEN = 0 | 15 | | ns |
| | | Master mode | HSRXEN = 1 | $15-0.5t_{SCK}$ | | |
| $t_{SU(SI)}$ | | Slave mode | | 4 | | ns |
| $t_{h(MI)}$ | Data input hold time | Master mode | HSRXEN = 0 | -4 | | ns |
| | | Master mode | HSRXEN = 1 | $0.5t_{SCK}-4$ | | |
| $t_{h(SI)}$ | | Slave mode | | 4 | | ns |
| $t_{a(SO)}$ | Data output access time | Slave mode, $f_{PCLK}$ = 20MHz | | 0 | $1t_{HCLK}$ | ns |
| $t_{dis(SO)}$ | Data output disable time | Slave mode | | 0 | 10 | ns |
| $t_{V(SO)}$ | Data output valid time | Slave mode (After enabling edge) | | | 15 | ns |
| $t_{V(MO)}$ | | Master mode (After enabling edge) | | | 5 | ns |
| $t_{h(SO)}$ | Data output hold time | Slave mode (After enabling edge) | | 8 | | ns |
| $t_{h(MO)}$ | | Master mode (After enabling edge) | | 0 | | ns |

### 3.3.16 USB Interface Characteristics

Table 3-27 USB interface I/O characteristics

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|

| | | | | | | |
|---|---|---|---|---|---|---|
| $V_{DD}$ | USB operating voltage | Selection of USB parameters according to $V_{DD}$ voltage | 3.0 | | 3.6 | V |
| $V_{SE}$ | Single-ended receiver threshold | Rated voltage | 1.2 | | 1.9 | V |
| $V_{OL}$ | Static output low level | | | | 0.3 | V |
| $V_{OH}$ | Static output high level | | 2.8 | | | V |
| $V_{BC\_REF}$ | BC comparator reference voltage | | | 0.4 | | V |
| $V_{BC\_SRC}$ | BC protocol output voltage | | | 0.6 | | V |

### 3.3.17 12-bit ADC Characteristics

Table 3-28 ADC characteristics

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DDA}$ | Supply voltage | $f_S < 200KHz$ | 1.8 | | 3.6 | V |
| | | $f_S = 2.4MHz$ | 3 | | 3.6 | V |
| $I_{DDA}$ | Supply current | $f_S = 2.4MHz$ Buffer off | | 1.2 | | mA |
| | | $f_S = 2.4MHz$ Buffer on | | 1.96 | | mA |
| | | $f_S = 1MHz$ Buffer off | | 0.45 | | mA |
| | | $f_S = 1MHz$ Buffer on | | 1.21 | | mA |
| $f_{ADC}$ | ADC clock frequency | | | 14 | 48 | MHz |
| $f_S$ | Sampling rate | | 0.05 | | 2.4 | MHz |
| $f_{TRIG}$ | External trigger frequency | $f_{ADC} = 14MHz$ | | | 875 | KHz |
| | | | | | 16 | $1/f_{ADC}$ |
| | | $f_{ADC} = 48MHz$ | | | 2.2 | MHz |
| | | | | | 22 | $1/f_{ADC}$ |
| $V_{AIN}$ | Conversion voltage range | | 0 | | $V_{DDA}$ | V |
| $R_{AIN}$ | External input impedance | | | | 50 | kΩ |
| $R_{ADC}$ | Sampling switch resistance | | | 0.6 | 1.5 | kΩ |
| $C_{ADC}$ | Internal sample and hold capacitor | | | 4 | | pF |
| $t_{CAL}$ | Calibration time | $f_{ADC} = 14MHz$ | | | 7.14 | us |
| | | | | | 100 | $1/f_{ADC}$ |
| $t_{Iat}$ | Injected trigger conversion latency | $f_{ADC} = 14MHz$ | | | 0.143 | us |
| | | $f_{ADC} = 48MHz$ | | | 0.042 | us |
| | | | | | 2 | $1/f_{ADC}$ |
| $t_{Iatr}$ | Regular trigger conversion latency | $f_{ADC} = 14MHz$ | | | 0.143 | us |
| | | $f_{ADC} = 48MHz$ | | | 0.042 | us |
| | | | | | 2 | $1/f_{ADC}$ |
| $t_s$ | Sampling time | $f_{ADC} = 14MHz$ | 0.107 | | 17.1 | us |
| | | | 1.5 | | 239.5 | $1/f_{ADC}$ |
| | | $f_{ADC} = 48MHz$ | | 0.125 | | us |
| | | | | 7.5 | | $1/f_{ADC}$ |
| $t_{STAB}$ | Power-on time | | | | 1 | us |
| $t_{CONV}$ | Total conversion time | $f_{ADC} = 14MHz$ | 1 | | 18 | us |

| | | | 14 | | 252 | $1/f_{ADC}$ |
|---|---|---|---|---|---|---|
| (including sampling time) | $f_{ADC}$ = 48MHz | | | 0.417 | | us |
| | | | | 20 | | $1/f_{ADC}$ |

*Note: The above are guaranteed design parameters.*

Formula: Maximum $R_{AIN}$

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln 2^{N+2}} - R_{ADC}$$

The above formula is used to determine the maximum external impedance such that the error can be less than 1/4 LSB. where N=12 (indicating 12-bit resolution).

Table 3-29 Maximum $R_{AIN}$ at $f_{ADC}$ = 14MHz

| $T_S$ (cycle) | $t_S$ (us) | Maximum $R_{AIN}$(kΩ) |
|---|---|---|
| 1.5 | 0.11 | 1.2 |
| 7.5 | 0.54 | 12.3 |
| 13.5 | 0.96 | 23.3 |
| 28.5 | 2.04 | 50 |
| 41.5 | 2.96 | 75 |
| 55.5 | 3.96 | No limit |
| 71.5 | 5.11 | No limit |
| 239.5 | 17.1 | No limit |

Table 3-30 ADC error

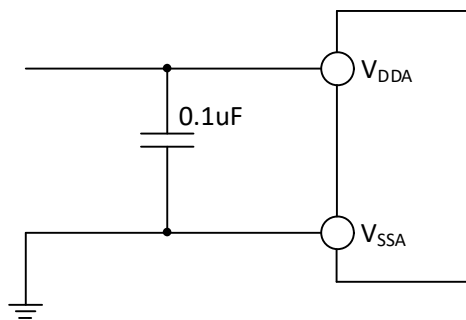| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| ET | Total error | $f_{ADC}$ = 48MHz, | | ±3 | ±6 | |
| EO | Offset error | $R_{AIN}$ <10kΩ, | | ±2 | ±5 | |
| EG | Gain error | $V_{DD}$ = 3.3V, | | ±1 | ±3 | LSB |
| ED | Differential nonlinear error | Measurements | | ±1 | ±6 | |
| EL | Integral nonlinear error | are calibrated | | ±2 | ±6 | |

*Note: The above are guaranteed design parameters.*

Figure 3-12 ADC typical connection diagram
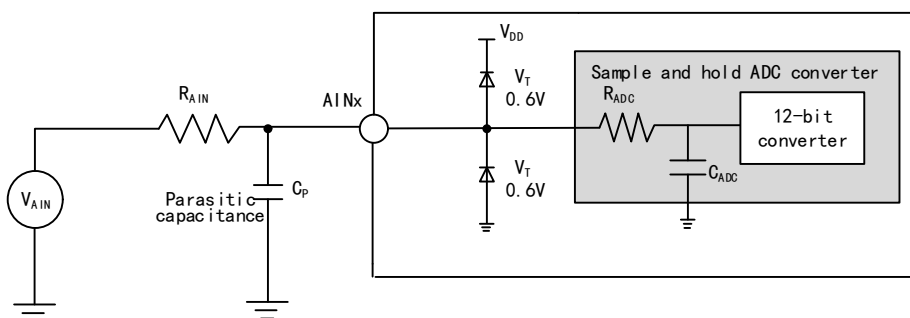


Cp indicates the parasitic capacitance on the PCB and pads (About 5pF), which may be related to the quality of the pads and PCB layout. Larger values of Cp will reduce the conversion accuracy and the solution is to reduce the $f_{ADC}$

value.

Figure 3-13 Analog power supply and decoupling circuit reference



### 3.3.18 TS Characteristics

Table 3-31 TS characteristics

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|--------|-----------|-----------|------|------|------|------|
| $R_{TS}$ | Temperature sensor measurement range | | -40 | | 85 | °C |
| $A_{TSC}$ | Measurement error of temperature sensors | | | ±12 | | °C |
| Avg_Slope | Average slope (negative temperature coefficient) | | 3.7 | 4.2 | 4.7 | mV/°C |
| $V_{25}$ | Voltage at 25°C | | 1.4 | 1.45 | 1.5 | V |
| $T_{S\_temp}$ | ADC sampling time when reading temperature | $f_{ADC} = 14MHz$ | | | 20 | us |

### 3.3.19 OPA Characteristics

Table 3-32-1 OPA characteristics

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|--------|-----------|-----------|------|------|------|------|
| $V_{DDA}$ | Supply voltage | Recommended not less than 2.4V | 1.8 | 3.3 | 3.6 | V |
| $V_{CM}$ | Common mode input voltage | | 0 | | $V_{DDA}$ | V |
| $V_{IOFFSET0}$ | Input offset voltage | Before calibration | | 2 | 8 | mV |
| $V_{IOFFSET}$ | Input offset voltage | After calibration | | 0.2 | 0.8 | mV |
| $I_{LOAD}$ | Drive current | $R_{LOAD} = 4k\Omega$ | | | 900 | uA |
| $I_{LOAD\_PGA}$ | PGA mode drive current | | | | 500 | uA |
| $I_{DDOPAMP}$ | Current consumption | No load, static mode | | 165 | | uA |
| $C_{MRR}$[1] | Common mode rejection ratio | @1kHz | | 96 | | dB |
| $P_{SRR}$[1] | Power supply rejection ratio | @1kHz | | 82 | | dB |
| $Av$[1] | Open loop gain | $C_{LOAD} = 5pF$ | | 115 | | dB |
| $G_{BW}$[1] | Unit gain bandwidth | $C_{LOAD} = 5pF$ | | 7 | | MHz |

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $P_M$[1] | Phase margin | $C_{LOAD}$ = 5pF | | 75 | | |
| $S_R$[1] | Slew rate limited | $C_{LOAD}$ = 5pF | | 3.2 | | V/us |
| $t_{WAKUP}$[1] | Setup time from shutdown to wake up, 0.1% | Input $V_{DDA}$/2, $C_{LOAD}$ = 50pF, $R_{LOAD}$ = 4kΩ | | | 0.8 | us |
| $R_{LOAD}$ | Resistive load | | 4 | | | kΩ |
| $C_{LOAD}$ | Capacitive load | | | | 50 | pF |
| $V_{OHSAT}$[2] | High saturation output voltage | $R_{LOAD}$ = 4kΩ | $V_{DDA}$-250 | $V_{DDA}$-150 | | mV |
| | | $R_{LOAD}$ = 20kΩ | $V_{DDA}$-50 | $V_{DDA}$-30 | | |
| $V_{OLSAT}$[2] | Low saturation output voltage | $R_{LOAD}$ = 4kΩ | | 3 | 10 | mV |
| | | $R_{LOAD}$ = 20kΩ | | 3 | 10 | |
| PGA Gain[1] | NSEL=010b mode in phase | Gain = 32, PB10 = GND | -3 | | 3 | % |
| | Internal in-phase PGA | Gain = 8, $V_{INP}$ <($V_{DDA}$/7) | -1 | | 1 | % |
| | | Gain = 16, $V_{INP}$ <($V_{DDA}$/15) | -1 | | 1 | % |
| | | Gain = 32, $V_{INP}$ <($V_{DDA}$/31) | -1 | | 1 | % |
| | | Gain = 64, $V_{INP}$ <($V_{DDA}$/63) | -1 | | 1 | % |
| Delta R | Absolute change in resistance | | -15 | | 15 | % |
| eN[1] | Equivalent input voltage noise | $R_{LOAD}$ = 4kΩ@1kHz | | 100 | | nV/ sqrt(Hz) |
| | | $R_{LOAD}$ = 20kΩ@1KHz | | 60 | | |

Note: 1. Design parameters are guaranteed;

2. Load current will limit saturated output voltage.

Table 3-32-2 OPA characteristics (low-power mode)

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DDA}$ | Supply voltage | Recommended not less than 2.4V | 1.8 | 3.3 | 3.6 | V |
| $V_{CM}$ | Common mode input voltage | | 0 | | $V_{DDA}$ | V |
| $V_{IOFFSET}$ | Input offset voltage | | | 2 | 12 | mV |
| $I_{LOAD}$ | Drive current | $R_{LOAD}$ = 10kΩ | | | 360 | uA |
| $I_{LOAD\_PGA}$ | PGA mode drive current | | | | 500 | uA |
| $I_{DDOPAMP}$ | Current consumption | No load, static mode | | 33 | | uA |
| $C_{MRR}$[1] | Common mode rejection ratio | @1kHz | | 90 | | dB |
| $P_{SRR}$[1] | Power supply rejection | @1kHz | | 78 | | dB |

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| | ratio | | | | | |
| $A_V$[1] | Open loop gain | $C_{LOAD}$ = 5pF | | 115 | | dB |
| $G_{BW}$[1] | Unit gain bandwidth | $C_{LOAD}$ = 5pF | | 3.5 | | MHz |
| $P_M$[1] | Phase margin | $C_{LOAD}$ = 5pF | | 76 | | |
| $S_R$[1] | Slew rate limited | $C_{LOAD}$ = 5pF | | 1.5 | | V/us |
| $t_{WAKUP}$[1] | Setup time from shutdown to wake up, 0.1% | Input $V_{DDA}/2$，$C_{LOAD}$ = 30pF, $R_{LOAD}$ = 4kΩ | | | 1.1 | us |
| $R_{LOAD}$ | Resistive load | | 10 | | | kΩ |
| $C_{LOAD}$ | Capacitive load | | | | 30 | pF |
| $V_{OHSAT}$[2] | High saturation output voltage | $R_{LOAD}$ = 10kΩ | $V_{DDA}$-300 | $V_{DDA}$-180 | | mV |
| | | $R_{LOAD}$ = 20kΩ | $V_{DDA}$-60 | $V_{DDA}$-35 | | |
| $V_{OLSAT}$[2] | Low saturation output voltage | $R_{LOAD}$ = 10kΩ | | 4 | 15 | mV |
| | | $R_{LOAD}$ = 20kΩ | | 4 | 15 | |
| PGA Gain[1] | NSEL=010b mode in phase | Gain = 32, PB10 = GND | -3 | | 3 | % |
| | Internal in-phase PGA | Gain = 8, $V_{INP}$ <($V_{DDA}/7$) | -1 | | 1 | % |
| | | Gain = 16, $V_{INP}$ <($V_{DDA}/15$) | -1 | | 1 | % |
| | | Gain = 32, $V_{INP}$ <($V_{DDA}/31$) | -1 | | 1 | % |
| | | Gain = 64, $V_{INP}$ <($V_{DDA}/63$) | -1 | | 1 | % |
| Delta R | Absolute change in resistance | | -15 | | 15 | % |
| $e_N$[1] | Equivalent input voltage noise | $R_{LOAD}$ = 10kΩ@1kHz | | 100 | | nV/ sqrt(Hz) |
| | | $R_{LOAD}$ = 20kΩ@1KHz | | 80 | | |

*Note: 1. Design parameters are guaranteed;*

    *2. Load current will limit saturated output voltage.*

### 3.3.20 CMP Characteristics

Table 3-33-1 CMP characteristics

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DDA}$ | Supply voltage | | 1.8 | 3.3 | 3.6 | V |
| $V_{CM}$ | Common mode input voltage | | 0 | | $V_{DDA}$ | V |
| $V_{IOFFSET}$ | Input offset voltage | | | 2.8 | 10 | mV |
| $I_{DDOPAMP}$ | Current consumption | | | 43 | | uA |
| $t_D$[1] | Comparator delay. $V_{INP}$ varies from ($V_{INN}$-100mV) to ($V_{INN}$+100mV) change | $0 \leq V_{INN} \leq V_{DDA}$ | | 16 | 40 | ns |

*Note: 1. Design parameters are guaranteed.*

Table 3-33-2 CMP characteristics (low-power mode)

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DDA}$ | Supply voltage | | 1.8 | 3.3 | 3.6 | V |
| $V_{CM}$ | Common mode input voltage | | 0 | | $V_{DDA}$ | V |
| $V_{IOFFSET}$ | Input offset voltage | | | 4 | | mV |
| $I_{DDOPAMP}$ | Current consumption | | | 3.5 | | uA |
| $t_D{}^{(1)}$ | Comparator delay. $V_{INP}$ varies from ($V_{INN}$-100mV) to ($V_{INN}$+100mV) change | $0 \leq V_{INN} \leq V_{DDA}$ | | 251 | 400 | ns |

*Note: 1. Design parameters are guaranteed.*

# Chapter 4 Package and Ordering Information

## Packages

| Order model | Package form | Body size | Pin pitch | Package description | Packing type |
|---|---|---|---|---|---|
| CH32L103C8T6 | LQFP48 | 7*7mm | 0.5mm | Low Profile Quad Flat Pack | Tray |
| CH32L103K8U6 | QFN32 | 4*4mm | 0.4mm | Quad Flat No-Lead Package | Tray |
| CH32L103G8R6 | QSOP28 | 3.9*9.9mm | 0.635mm | Quarter-sized Outline Package | Tube |
| CH32L103F8U6 | QFN20 | 3*3mm | 0.4mm | Quad Flat No-Lead Package | Tape & Reel |
| CH32L103F8P6 | TSSOP20 | 4.4*6.5mm | 0.65mm | Thin Shrink Small Outline Package | Tube, Tape & Reel |

*Note: 1. The packing type of QFP/QFN is usually tray.*

*2. Size of tray: The size of Tray is generally a uniform size (322.6\*135.9\*7.62). There are differences in the size of the restriction holes for different package types, and there are differences between different packaging factories for tubes, please confirm with the manufacturer for details.*

*Note: All dimensions are in millimeters. The pin center spacing values are nominal values, with no error. Other than that, the dimensional error is not greater than the greater of ±0.2mm or 10%.*

Figure 4-1 LQFP48 package
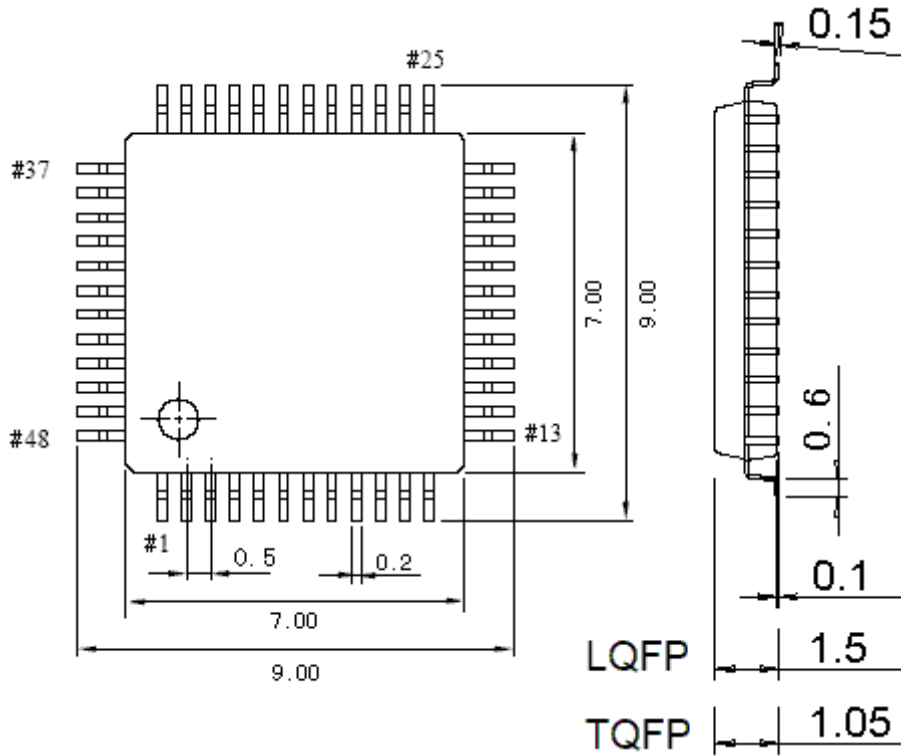


Figure 4-2 QFN32 package

Figure 4-3 QSOP28 package



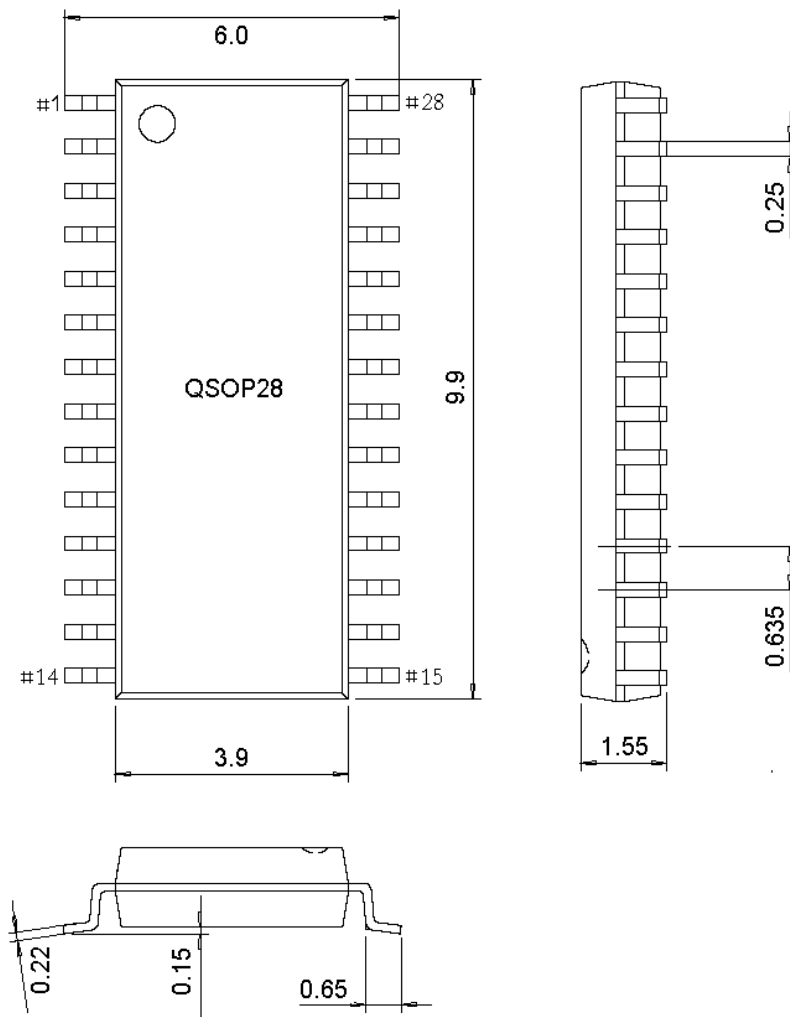Figure 4-4 QFN20 package

Figure 4-5 QFN20 package

# Series Product Naming Rules

Example:          CH32          V          3          03          R          8          T          6

**Device family**

F = ARM-based, general-purpose MCU

V = QingKe RISC-V-based, general-purpose MCU

L = QingKe RISC-V-based, low-power MCU

X = QingKe RISC-V-based, Dedicated architecture or special IO

**Product type**

0 = QingKe V2/V4 core, great value version, main frequency @ 48M

1 = M3 / QingKe V3/V4 core, basic version, main frequency @ 72M

2 = M3 / QingKe V4 non-floating-point core, enhanced version, main frequency @ 144M

3 = QingKe V4F floating-point core, main frequency @ 144M

**Device subfamily**

03 = General-purpose

05 = Connectivity (USB high-speed, SDIO, dual-CAN)

07 = Interconnectivity (USB high-speed, CAN, Ethernet, DVP, SDIO, FSMC)

08 = Wireless (BLE5.X, CAN, USB, Ethernet)

35 = Connectivity (USB, USB PD)

**Pin count**

| | | |
|---|---|---|
| J = 8 pins | A = 16 pins | F = 20 pins |
| G = 28 pins | K = 32 pins | T = 36 pins |
| C = 48 pins | R = 64 pins | W = 68 pins |
| V = 100 pins | Z = 144 pins | |

**Flash memory size**

4 = 16 Kbytes of Flash memory

6 = 32 Kbytes of Flash memory

7 = 48 Kbytes of Flash memory

8 = 64 Kbytes of Flash memory

B = 128 Kbytes of Flash memory

C = 256 Kbytes of Flash memory

**Package**

| | | | | |
|---|---|---|---|---|
| T = LQFP | U = QFN | R = QSOP | P = TSSOP | M = SOP |

**Temperature range**

6 = -40℃~85℃ (Industrial-grade)

7 = -40℃~105℃ (Automotive-grade 2)

3 = -40℃~125℃ (Automotive-grade 1)

D = -40℃~150℃ (Automotive-grade 0)