7-port USB HUB Controller Chip CH338

Datasheet

Version: V1.1

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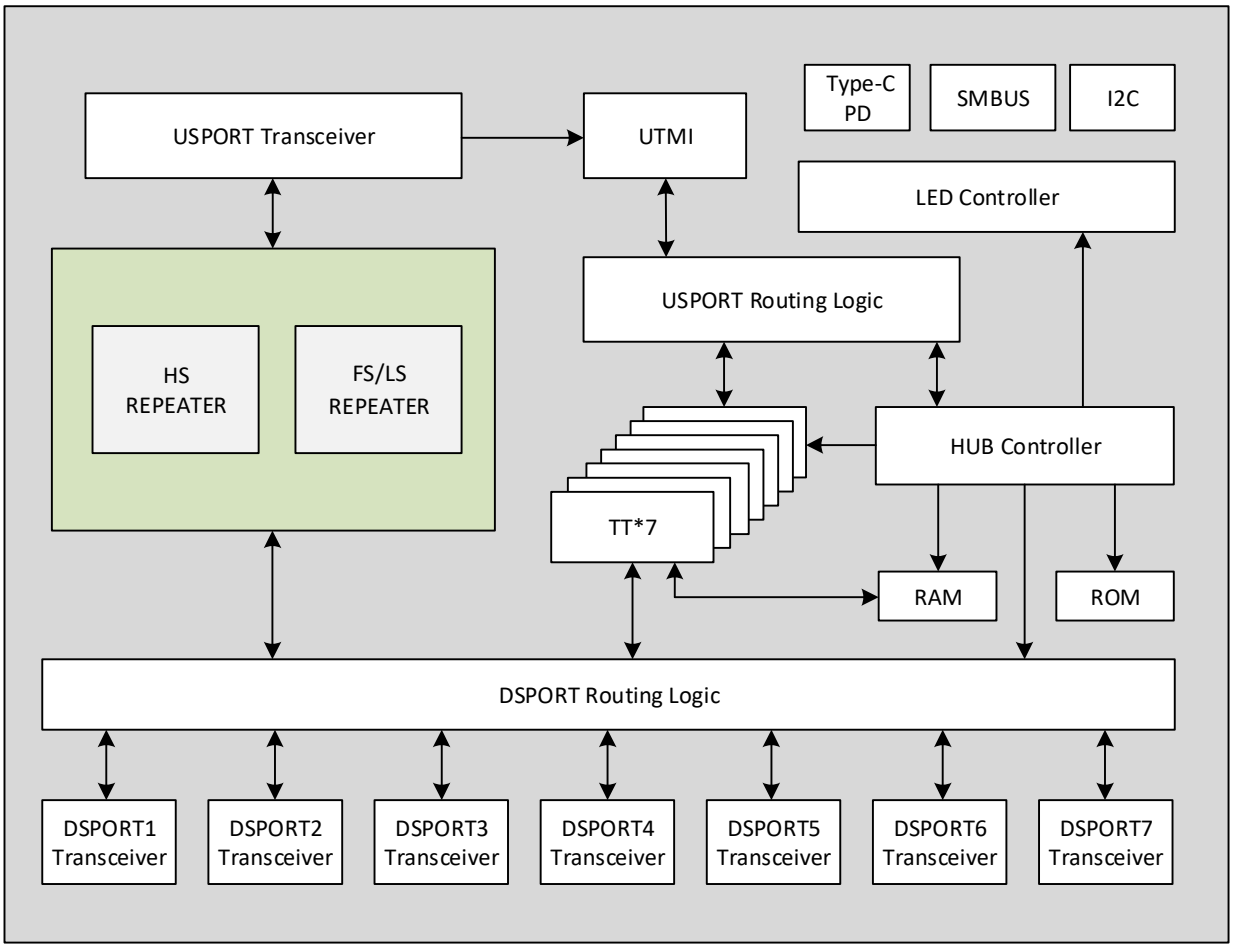
1. Overview

CH338 is a 7-port USB HUB controller chip that complies with the USB2.0 protocol specification. The upstream port supports USB2.0 high-speed and full-speed, the downstream port supports USB2.0 high-speed 480Mbps, full-speed 12Mbps and low-speed 1.5Mbps. It not only supports the low-cost STT mode (A single TT schedules 7 downstream ports in a time-sharing manner), but also supports the high-performance MTT mode (7 TTs each correspond to one port and are processed concurrently). In addition to the HUB controller function, some models also support PD function.

Industrial-grade design, streamlined peripherals, can be applied to computer and industrial computer motherboards, peripherals, embedded systems, etc.

The figure below is the system block diagram of CH338.

Figure 1-1 System block diagram



The figure above is the internal structure block diagram of the HUB controller system. HUB controller mainly includes three modules: Repeater, TT and controller. The controller is similar to an MCU processor and is used for global management and control. When the speed of the upstream port and the downstream port are consistent, the routing logic will connect the port to the Repeater. When the speed of the upstream port and the downstream port are inconsistent, the routing logic will connect the port to the TT.

TT is divided into two types: single TT and multiple TT, namely STT and MTT. STT is a time-sharing scheduling of a single TT core to process transactions sent by the USB host to all downstream ports. MTT refers to multiple TT parallel, which are seven TT cores respectively. Corresponding to and processing the transactions of a downstream port in real time, MTT can provide full bandwidth for the access equipment of each downstream port and better support the concurrent transmission of large amounts of data across multiple ports.

Note:

USPORT Transceiver: Upstream port transceiver PHY;

DSPORT Transceiver: Downstream port transceiver PHY;

REPEATER: HUB repeater;

TT: Handle converters.

2. Feature

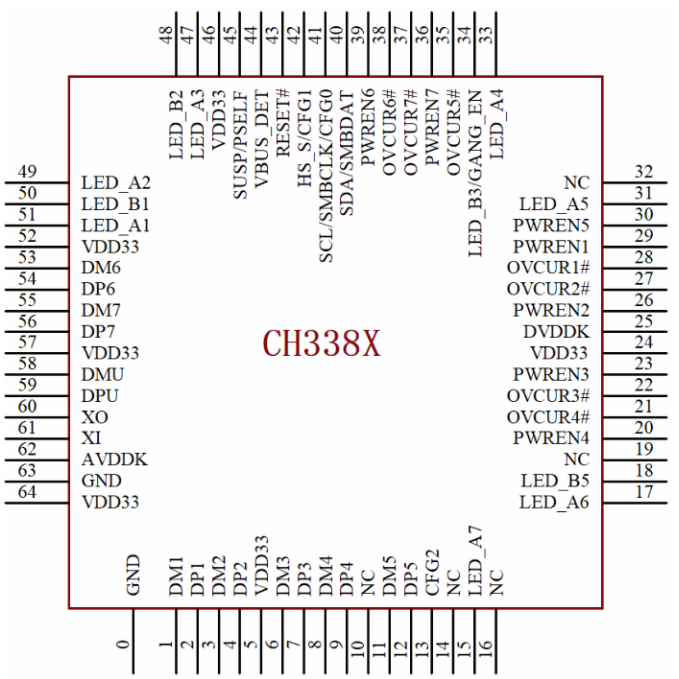
- 7-port USB HUB with 7 USB2.0 downstream ports, backward compatible with USB1.1 protocol specification
- Support independent power control for each port or GANG overall linkage power control
- Support independent over-current detection for each port or GANG overall over-current detection
- Support high-performance MTT mode, providing independent TT for each port to achieve full bandwidth concurrent transmission, the total bandwidth is 7 times that of STT
- Support port status LED indicator
- Whether to support composite devices, non-removable devices, custom VID, PID, port configuration and USB vender, product, serial number string descriptors, etc. can be configured through external EEPROM or internal EEPROM.
- Chip related parameters can be configured through the SMBus interface
- Built-in information memory, vender or product information and configuration can be customized in batches according to special needs of the industry
- Self-developed dedicated USBPHY, low-power consumption technology, supports self-power supply or bus power supply
- Functions such as self-powered or bus-powered modes can be configured through I/O pins
- Provide crystal oscillator, built-in capacitor, supports external clock input, built-in PLL provides 480MHz clock for USBPHY
- Some applications can support crystal-free mode, saving external crystals and capacitors.
- The upstream port has a built-in 1.5KΩ pull-up resistor, and the downstream port has a built-in pull-down resistor required by the USB Host, simplifying the peripherals.
- Some models have a built-in LDO linear step-down regulator, which can convert the USB bus power supply voltage into the chip's 3.3V working power supply.
- USB interface pins have 6KV Enhanced ESD Performance, Class 3A
- Industrial-grade temperature range: -40 to 85°C
- Available in QFN64, LQFP48, QFN32 and other small, low-cost, easy-to-process packages

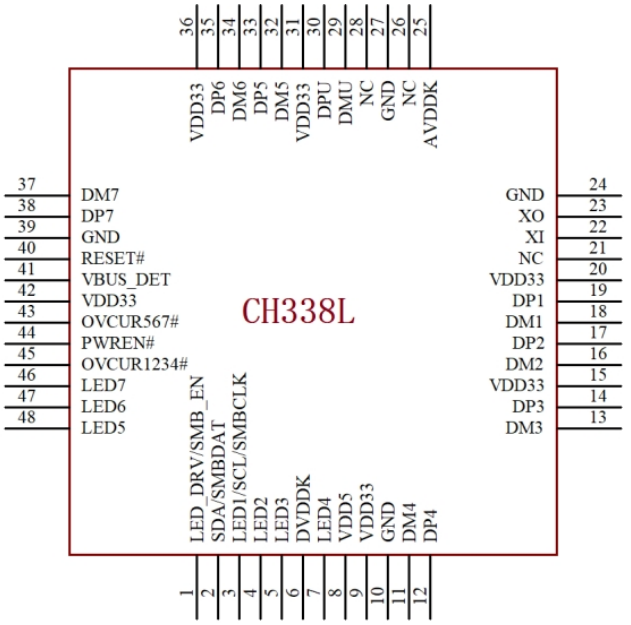
Table 1-1 Comparison of functions of models in the same cluster

Function \ Model	CH338X	CH338L	CH338F
TT mode	MTT	MTT	MTT
Overcurrent detection	Independent/GANG	GANG mode	GANG mode

Power control	Independent /GANG	GANG mode	GANG mode
LED	7+4	15	×
I/O pin configuration power supply mode	√	×	×
I/0 pin configuration non-removable device	√	√	×
External/internal EEPROM provide configuration information	√	√	√
SMBus interface configuration information	√	√	√
Custom configuration information	√	√	√
Upstream port switching function	×	×	√
Extension/isolation function	×	×	√
Type-C / PD	×	×	√
Chip power supply	Single 3.3V	Single 3.3V Or single 5V	Single 3.3V

3. Package





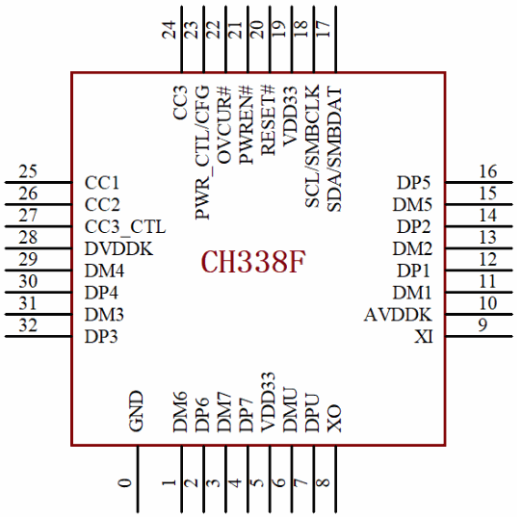


Table 3-1 Package description

Package form	Body size	Pin pitch		Package description	Order model
QFN64×9	9*9mm	0.5mm	19.7mil	Quad Flat No-Lead Package	CH338X
LQFP48	7*7mm	0.5mm	19.7mil	Low Profile Quad Flat Pack	CH338L
QFN32	4*4mm	0.4mm	15.7mil	Quad Flat No-Lead Package	CH338F

Note: CH338F is preferred for small size; CH338X and CH338L focus on PCB compatibility.

Pin 0# is the EPAD of the QFN package and is a required connection.

4. Pin

Table 4-1 Pin definition

Pin number (please refer to the pin with the same name)			Pin name	Type(1)	Function description
CH338X	CH338L	CH338F			
58	29	6	DMU	USB	Upstream port USB2.0 signal line D-
59	30	7	DPU	USB	Upstream port USB2.0 signal line D+
1	18	11	DM1	USB	1# Downstream port USB signal line D-
2	19	12	DP1	USB	1# Downstream port USB signal line D+
3	16	13	DM2	USB	2# Downstream port USB signal line D-
4	17	14	DP2	USB	2# Downstream port USB signal line D+
6	13	31	DM3	USB	3# Downstream port USB signal line D-
7	14	32	DP3	USB	3# Downstream port USB signal line D+
8	11	29	DM4	USB	4# Downstream port USB signal line D-
9	12	30	DP4	USB	4# Downstream port USB signal line D+
11	32	15	DM5	USB	5# Downstream port USB signal line D-
12	33	16	DP5	USB	5# Downstream port USB signal line D+
53	34	1	DM6	USB	6# Downstream port USB signal line D-
54	35	2	DP6	USB	6# Downstream port USB signal line D+
55	37	3	DM7	USB	7# Downstream port USB signal line D-
56	38	4	DP7	USB	7# Downstream port USB signal line D+
61	22	9	XI	I	Crystal oscillator input terminal, connected to one terminal of the external crystal
60	23	8	XO	O	The inverting output terminal of the crystal oscillator is connected to the other terminal of the external crystal.
43	40	20	RESET#	5I	External reset input, built-in pull-up resistor, active at low level, recommended to be left completely unconnected when not in use
-	8	-	V_{DD5}	P	LDO power input, 5V or 3.3V, external 1uF or larger capacitor
-	9	-	V_{DD33}	P	LDO power output, 3.3V, external 1uF or larger capacitor
5、57	20、36	5、19	V_{DD33}	P	Analog power input, 3.3V, external 1uF decoupling capacitor
52、64	15、31	-	V_{DD33}	P	Auxiliary power input, 3.3V, external 1uF or 0.1uF decoupling capacitor
24、46	42	-	V_{DD33}	P	I/O power input, 3.3V, external 1uF or 0.1uF decoupling capacitor
62	25	10	AV_{DDK}	P	1.2V core power, external 1uF or 0.1uF decoupling capacitor
25	6	28	DV_{DDK}	P	1.2V core power, external 0.1uF decoupling capacitor
0	10、24	0	GND	P	Common ground terminal, must be connected to GND
63	27、39	-	GND	P	Common ground, optional connection

28	-	-	OVCUR1#	5I	Downstream port 1 overcurrent detection input pin, low level overcurrent Overall mode downstream port overcurrent detection input pin, low level overcurrent
27	-	-	OVCUR2#	5I	Downstream port 2 overcurrent detection input pin, low level overcurrent
22	-	-	OVCUR3#	I	Downstream port 3 overcurrent detection input pin, low level overcurrent
21	-	-	OVCUR4#	I	Downstream port 4 overcurrent detection input pin, low level overcurrent
35	-	-	OVCUR5#	I	Downstream port 5 overcurrent detection input pin, low level overcurrent
38	-	-	OVCUR6#	I	Downstream port 6 overcurrent detection input pin, low level overcurrent
37	-	-	OVCUR7#	I	Downstream port 7 overcurrent detection input pin, low level overcurrent
-	-	22	OVCUR#	5I	Overall mode downstream port overcurrent detection input pin, low level overcurrent
-	45	-	OVCUR1234#	5I	Downstream port 1/2/3/4 overcurrent detection input pin, low level overcurrent
-	43	-	OVCUR567#	5I	Downstream port 5/6/7 overcurrent detection input pin, low level overcurrent
29	-	-	PWREN1	O	Downstream port 1 power output control pin, high level enabled Overall mode downstream port power output control pin, high level enabled
26	-	-	PWREN2	O	Downstream port 2 power output control pin, high level enabled
23	-	-	PWREN3	O	Downstream port 3 power output control pin, high level enabled
20	-	-	PWREN4	O	Downstream port 4 power output control pin, high level enabled
30	-	-	PWREN5	O	Downstream port 5 power output control pin, high level enabled
39	-	-	PWREN6	O	Downstream port 6 power output control pin, high level enabled
36	-	-	PWREN7	O	Downstream port 7 power output control pin, high level enabled
-	44	21	PWREN#	O	Overall mode downstream port power output control pin, low level enabled
51	3	-	LED_A1/ LED1	O	LED_A1: Downstream port 1 normal status indication signal LED1: Downstream port 1 status indication signal
49	4	-	LED_A2/	O	LED_A2: Downstream port 2 normal status indication

			LED2		signal LED2: Downstream port 2 status indication signal
47	5	-	LED_A3/ LED2	O	LED_A3: Downstream port 3 normal status indication signal LED3: Downstream port 3 status indication signal
33	7	-	LED_A4/ LED4	O	LED_A4: Downstream port 4 normal status indication signal LED4: Downstream port 4 status indication signal
31	48	-	LED_A5/ LED5	O	LED_A5: Downstream port 5 normal status indication signal LED5: Downstream port 5 status indication signal
17	47	-	LED_A6/ LED6	O	LED_A6: Downstream port 6 normal status indication signal LED6: Downstream port 6 status indication signal
15	46	-	LED_A7/ LED7	O	LED_A7: Downstream port 7 normal status indication signal LED7: Downstream port 7 status indication signal
-	1	-	LED_DRV/ SMB_EN	I/O	LED_DRV: LED indicator LED drive control signal SMB_EN: It is used as a configuration pin during reset to configure IIC mode or SMBus mode. Floating or high level is IIC mode, low level is SMBus mode, and it has a built-in pull-up resistor.
50	-	-	LED_B1	O	LED_B1: Downstream port 1 abnormal status indication signal
48	-	-	LED_B2	O	LED_B2: Downstream port 2 abnormal status indication signal
34	-	-	LED_B3/ GANG_EN	I/O	LED_B3: Downstream port 3 abnormal status indication signal GANG_EN: It is used as a configuration pin during reset to configure the overall mode or independent mode. The floating or high level is independent mode, and the low level is overall mode. It has a built-in pull-up resistor.
18	-	-	LED_B5	O	LED_B5: Downstream port 5 abnormal status indication signal
45	-	-	SUSP/ PSELF	I/O	SUSP: SUSPEND sleep state output pin, high level indicates sleep state, low level indicates normal state; PSELF: It is used as a configuration pin during reset to configure the power supply mode. The floating or high level is the self-power supply mode, and the low level is the bus power supply mode. It has a built-in pull-up resistor.
13			CFG2	I	CH338X chip function configuration pin 2
42			HS_S/	I/O	CH338X chip function configuration pin 1

			CFG1		HS_S: Upstream port speed status output pin, high level indicates USB high-speed, low level indicates USB full-speed; It serves as a configuration pin during reset and cooperates with CFG2 and CGF0 for functional configuration.
41			CFG0	I	CH338X chip function configuration pin 0
44	41	-	VBUS_DET	5I	USB bus V_{BUS} status detection input, built-in pull-down resistor
41	3	18	SCL/ SMBCLK	O	SCL: During reset the EEPROM clock signal line output SMBCLK: SMBus bus clock signal line
40	2	17	SDA/ SMBDAT	I/O	SDA: During reset the EEPROM bidirectional data signal line SMBDAT: SMBus bus data signal line
-	-	25	CC1	I/O	PD protocol communication pin CC1, used to connect the adapter
-	-	26	CC2	I/O	PD protocol communication pin CC2, used to connect the adapter
-	-	24	CC3	I/O	PD protocol communication pin CC3, used to connect cell phones/computers
-	-	27	CC3_CTL	O	CC3_CTL: PD protocol communication pin CC3 control pin
-	-	23	PWR_CTL/ CFG	I/O	PD protocol communication power control pin CFG: As a configuration pin during reset, different operating parameters are configured through different resistors.
10、14、16、19、32	21、26、28	-	NC		Empty pins or reserved pins are prohibited from being connected.

Note 1: Pin type abbreviation explanation:

I: 3.3V signal input. O: 3.3V signal output.

5I: Rated 3.3V signal input; Support 5V tolerant voltage.

P: Power or ground.

5. Function Description

5.1 Overcurrent Detection and Power Control

5.1.1 Overcurrent Detection

CH338X supports two overcurrent protection modes: independent overcurrent mode and overall overcurrent mode. CH338L and CH338F support overall overcurrent mode, as shown in Table 5-1.

Table 5-1 Overcurrent protection control instructions

Chip model	Overcurrent configuration	Overcurrent mode	Sampling pin for overcurrent detection	Reference figure
CH338X	EEPROM default allocation/ GANG_EN = high level	Independent overcurrent	OVCUR1#, OVCUR2#, OVCUR3#, OVCUR4#, OVCUR5#, OVCUR6#, OVCUR7#	Figure 5-1
	EEPROM non-default configuration/ GANG_EN = low level	Overall overcurrent	OVCUR1#	Figure 5-2
CH338L	-	Overall overcurrent	OVCUR1234#, OVCUR567#	Figure 5-2
CH338F	-	Overall overcurrent	OVCUR#	Figure 5-2

5.1.2 Power Supply

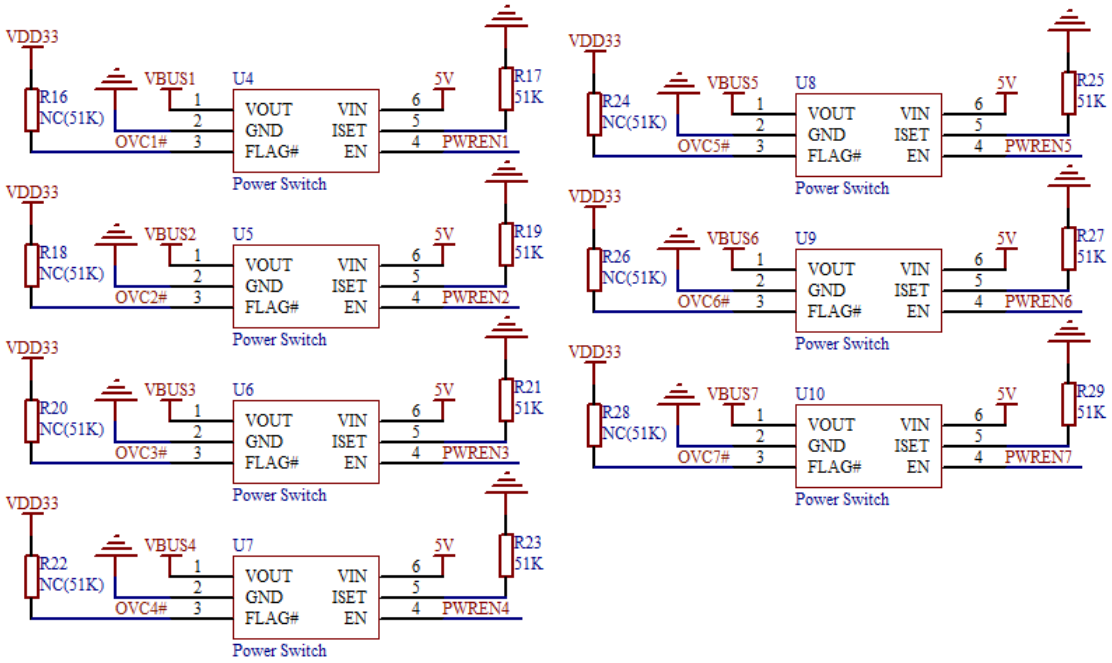
CH338X supports two power control modes: independent power control mode and overall power control mode. CH338L and CH338F support overall power control mode, as shown in Table 5-2.

Table 5-2 Power control instructions

Chip model	Power control configuration	Power control	Overcurrent power control pin	Reference figure
CH338X	EEPROM default allocation / GANG_EN = high level	Independent overcurrent	PWREN1, PWREN2, PWREN3, PWREN4, PWREN5, PWREN6, PWREN7 *Note: High level enabled*	Figure 5-1
	EEPROM non-default configuration / GANG_EN = low level	Overall overcurrent	PWREN1 *Note: High level enabled*	Figure 5-2
CH338L/ CH338F	-	Overall overcurrent	PWREN# *Note: High level enabled*	Figure 5-2

5.1.3 Independent Overcurrent Detection and Independent Power Supply Control

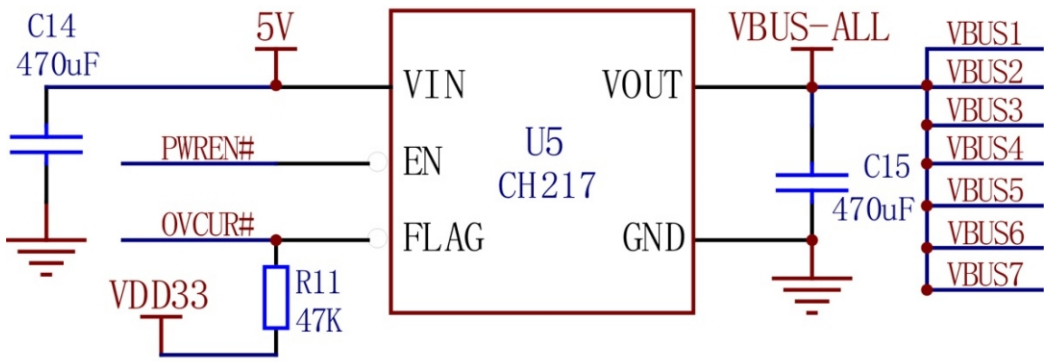
Figure 5-1 CH338X independent overcurrent detection and independent power supply control



In the figure above, V_{BUS1}-V_{BUS7} are connected to the V_{BUS} power pins of downstream ports 1-7 respectively. U4~U10 are USB current-limiting power distribution switch chips with integrated over-current detection for V_{BUS} power distribution management. In applications without external power supply of 5V, it is recommended to set the current limit below 1A or even 500mA through ISET external resistor. The FLAG pins of U4~U10 are open-drain outputs and need to be pulled up through resistors respectively. In the default configuration, OC_LEVEL=0, the OVCUR# pin of the CH338 chip provides a built-in weak pull-up current, so the resistors R16, R18, R20, R22, R24, R26 and R28 can be omitted. If the power switch chip control pin used is active high, the PWREN pin needs to be polarity swapped. The CH338X chip's overcurrent detection pin (OVCURx), downstream port power control pin (PWRENx), and indicator pins (LEDx) all support polarity configuration via configuration pins or EEPROM.

5.1.4 Overall Overcurrent Detection and Overall Power Supply Control

Figure 5-2 Overall overcurrent detection and independent power supply control



U5 is a USB current-limiting power switch chip, such as a CH217 chip or a chip with similar functions. R11 can be omitted in the default configuration. The capacity of C14 can be selected according to needs. $V_{BUS-ALL}$ is also connected to the V_{BUS} power pins of downstream ports 1-7. The current limit setting value of U5 needs to consider the 7 downstream ports and whether it is self-powered.

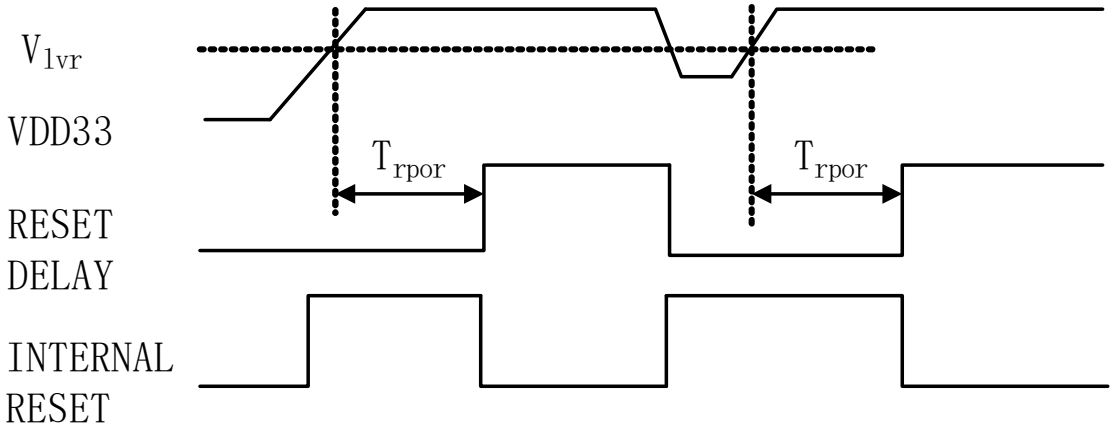
5.2 Reset

There is a power-on reset module embedded in the chip. Under normal circumstances, there is no need to provide an external reset signal. An external reset input pin RESET# is also provided, which has a built-in pull-up resistor.

5.2.1 Power on Reset

When the power supply is powered on, the chip's internal POR power-on reset module will generate a power-on reset sequence and delay Trpor for about 25mS to wait for the power supply to stabilize. During operation, when the power supply voltage is lower than V_{lvr}, the chip's internal LVR low-voltage reset module will generate a low-voltage reset until the voltage rises, and delays to wait for the power supply to stabilize. Figure 5-3 below shows the power-on reset process and low-voltage reset process.

Figure 5-3 Reset during power-on



5.2.2 External Reset

The external reset input pin RESET# has a built-in pull-up resistor of about 40KΩ. If the chip needs to be reset externally, then this pin can be driven low, the internal resistance of the driver is recommended to be no more than 1KΩ, and the low pulse width of the reset needs to be greater than 4uS.

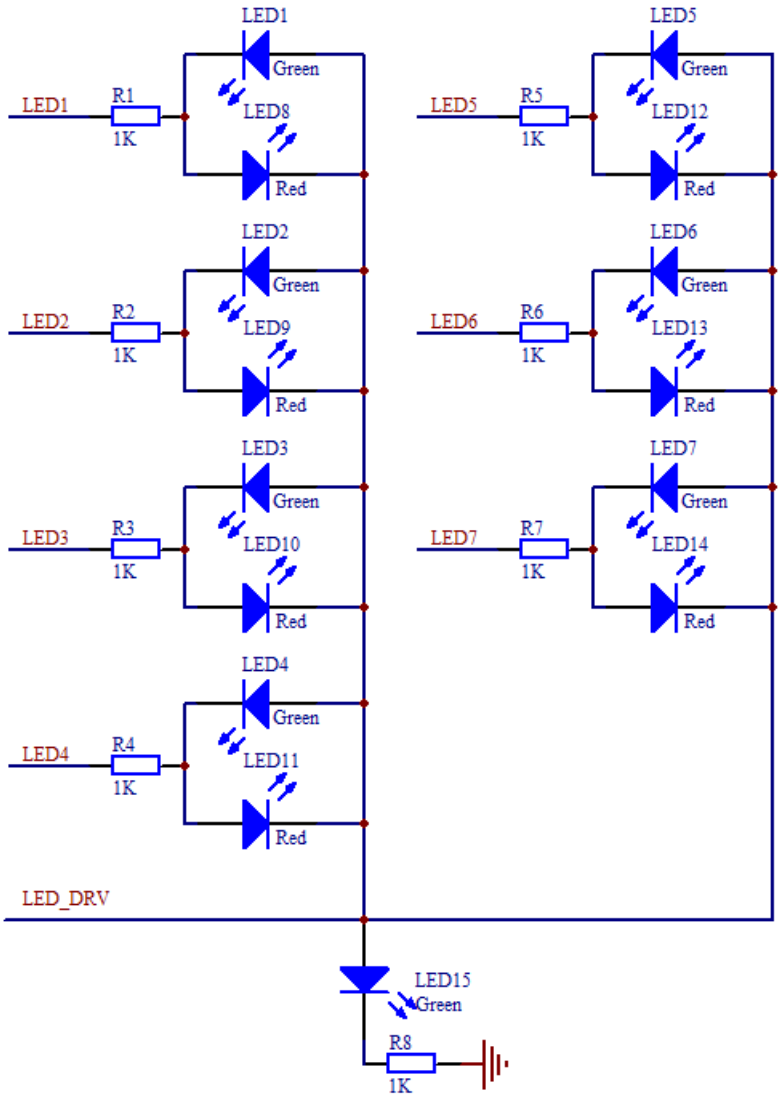
5.3 LED

According to the USB2.0 protocol specification, CH338 provides a downstream port status LED indicator control pin, the corresponding green LED of the port is on to indicate the port status is normal, the green LED is off to indicate that there is no device on the port or suspend, and the corresponding red LED of the port is on to indicate that the port is abnormal.

5.3.1 CH338L 15-LED Application

The figure below is a schematic diagram of the complete 15-LED mode application of CH338L, in which LED1-7 are the normal status indicators (Green LED) of ports 1-7 respectively. On indicates that a device is inserted into the port and the port is normal, and off indicates that there is no device on the port or suspend. LED8-14 are the abnormal status indicators (Red LED) of ports 1-7 respectively. When lit, it indicates that the port is abnormal, such as overcurrent. LED15 is the HUB working indicator LED. When it lights up, it indicates that the HUB is normal. When it goes out, it indicates that the HUB is suspended.

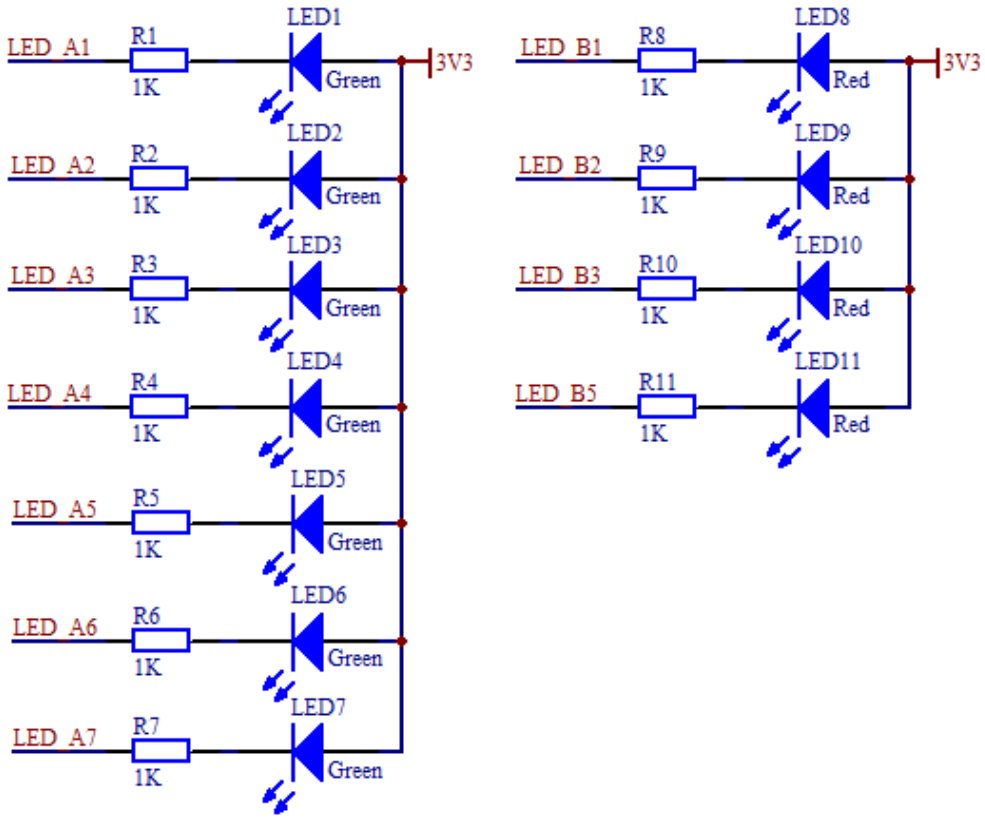
Figure 5-4 CH338L overall 15-LED mode application schematic



5.3.2 CH338X 11-LED Application

Figure 5-5 is a schematic diagram of the CH338X 11-LED mode application, in which LED1-7 are the normal status indicators (Green LED) of ports 1-7 respectively. On indicates that a device is inserted into the port and the port is normal, and off indicates that there is no device on the port or suspend. LED8-11 are the abnormal status indicators (Red LED) of ports 1, 2, 3 and 5 respectively. When lit, it indicates that the port is abnormal, such as overcurrent.

Figure 5-5 CH338X 11-LED mode application schematic



5.4 I/O Function Configuration

Some functions of CH338 can be configured in 3 ways: built-in or external EEPROM, SMBus interface and configuration pins. The parameter configuration function of EEPROM has a higher priority than the pin configuration function. Configuration pins are generally multiplexed pins that are used as configuration pins during reset. After the reset is completed, they are switched to the corresponding function pins.

Table 5-3 CH338X main configuration pin descriptions

Chip model	PIN13	PIN42	PIN41	Function description
	CFG2	CFG1	CFG0	
CH338X	0	0	0	Internal EEPROM configuration parameter function enabled Other function configuration pin enabled during reset HUB self-powered mode
	0	0	1	Internal EEPROM configuration parameter function enabled SMBus interface enabled Other function configuration pin disabled during reset HUB self-powered mode
	0	1	0	Internal EEPROM configuration parameter function enabled Other function configuration pin enabled during reset USB bus powered mode
	0	1	1	Internal EEPROM configuration parameter function enabled IIC interface enabled

				Other function configuration pin disabled during reset HUB self-powered mode
	1	0	0	Internal EEPROM configuration parameter function enabled
	1	0	1	Other function configuration pin disabled during reset
	1	1	0	HUB self-powered mode
	1	1	1	Internal EEPROM configuration parameter function enabled Other function configuration pin disabled during reset Overall power control, overall overcurrent detection HUB self-powered mode

Table 5-4 CH338X auxiliary configuration pin descriptions

Chip model	Function configuration	Pin status and function configuration description		
CH338X	Device removal function configuration	PIN40 SDA/SMBDAT	PIN45 SUSP/PSELF	Function description
		0	0	All ports are removable devices
		0	1	Port 1 is a non-removable device
		1	0	Port 1/2 is a non-removable device
		1	1	Ports 1/2/3 is non-removable devices
	Current overcurrent, power control mode configuration	PIN34 GANG_EN	Function description	
		0	Overall mode (Overall overcurrent, overall control)	
		1	Independent mode (Independent overcurrent, independent control)	
	Power control pin polarity configuration	PIN49 LED_A2	Function description	
		0	Active low	
		1	Active high	
	Overcurrent detection pin polarity configuration	PIN47 LED_A3	Function description	
		0	Active high (OC_LEVEL=1)	
		1	Active low (OC_LEVEL=0)	
	LED pin polarity configuration	PIN33 LED_A4	Function description	
		0	Active high	
		1	Active low	

Table 5-5 CH338L auxiliary configuration pin descriptions

Chip model	Function configuration	Pin status and function configuration description

<table>
<tr><td rowspan="13">CH338L</td><td rowspan="5">Downstream port enable configuration</td><td>PIN46
LED7</td><td>PIN47
LED6</td><td colspan="2">Function description</td></tr>
<tr><td>0</td><td>0</td><td colspan="2">Downstream ports 4, 3, 2, 1 enabled</td></tr>
<tr><td>1</td><td>0</td><td colspan="2">Downstream ports 5, 4, 3, 2, 1 enabled</td></tr>
<tr><td>0</td><td>1</td><td colspan="2">Downstream ports 6, 5, 4, 3, 2, 1 enabled</td></tr>
<tr><td>1</td><td>1</td><td colspan="2">Downstream ports 7, 6, 5, 4, 3, 2, 1 enabled</td></tr>
<tr><td rowspan="8">Device removal function configuration</td><td>PIN7
LED4</td><td>PIN5
LED3</td><td>PIN4
LED2</td><td>Function description</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>All ports are removable devices</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Port 2 is a non-removable device</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Ports 3 and 2 are non-removable devices</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Ports 3, 2, and 1 are non-removable devices</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Ports 4, 3, 2, and 1 are non-removable devices</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Ports 5, 4, 3, 2, and 1 are non-removable devices</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Ports 6, 5, 4, 3, 2, and 1 are non-removable devices</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Ports 7, 6, 5, 4, 3, 2, and 1 are non-removable devices</td></tr>
</table>

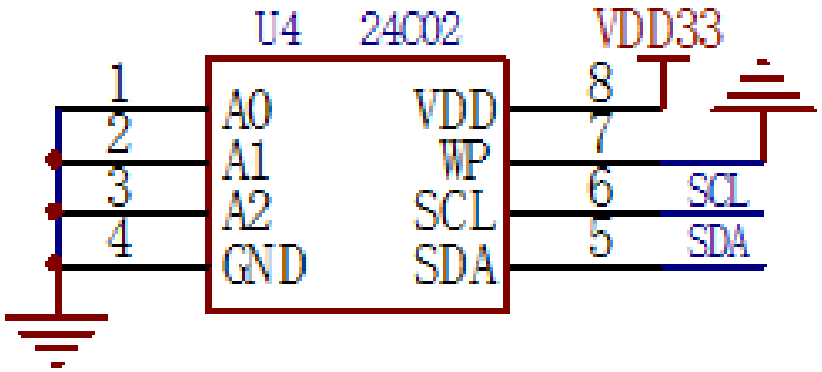
Table 5-6 CH338F configuration pin descriptions

<table>
<tr><th>Chip model</th><th>Function configuration</th><th colspan="2">Pin status and function configuration description</th></tr>
<tr><td rowspan="6">CH338F</td><td rowspan="6">Device removal function configuration</td><td>PIN23
PWR_CTL/CFG</td><td>Function description</td></tr>
<tr><td>15KΩ resistance to ground</td><td>Enable I2C interface, external EEPROM</td></tr>
<tr><td>9.1KΩ resistance to ground</td><td>Enable SMBus interface</td></tr>
<tr><td>3.9KΩ resistance to ground</td><td>Enable the exchange function between the upstream port and the downstream PORT1 port, and enable the SMBus interface. Write the register control with the offset address 0xFF through the SMBus interface. Write 0xCO to control switching. Writing 0x8O will not switch. Writing other values is invalid.</td></tr>
<tr><td>2KΩ resistance to ground</td><td>Enable the exchange function between the upstream port and the downstream PORT1 port, controlled by the SDA pin. There is no switching when it is left floating or pulled up. The input low level controls the switching.</td></tr>
<tr><td>820Ω resistance to ground</td><td>Enable 2-wire extension/isolation function</td></tr>
</table>

5.5 EEPROM Configuration Interface

CH338 provides a 2-wire I2C interface to communicate with an external EEPROM memory chip. The EEPROM chip address is 0. The EEPROM stores customized vender ID, product ID, USB string descriptor and functional configuration information. The SCL pin output clock frequency is about 100KHz, and the SDA pin has a built-in pull-up resistor to support open-drain bidirectional data communication without the need for an external pull-up resistor.

Figure 5-6 External EEPROM connection diagram



CH338 has built-in information memory, which can replace external EEPROM to mass-customize vender or product information and configuration according to the special needs of the industry, such as setting the number of downstream ports, setting the non-removable characteristics of the device of the downstream port, etc.

5.6 SMBus Configuration Interface

CH338 provides a 2-wire SMBus slave interface to communicate with the external master chip. The SMBus interface contains two pins, SMCLK and SMDAT. The communication address is 0x2C. It supports block read and block write operations, and each block is up to 32 bytes. The external master can read and write the EEPROM built into the chip through the SMBus interface. Figure 5-7 is a schematic diagram of block reading, and Figure 5-8 is a schematic diagram of block writing.

Figure 5-7 Block read schematic diagram

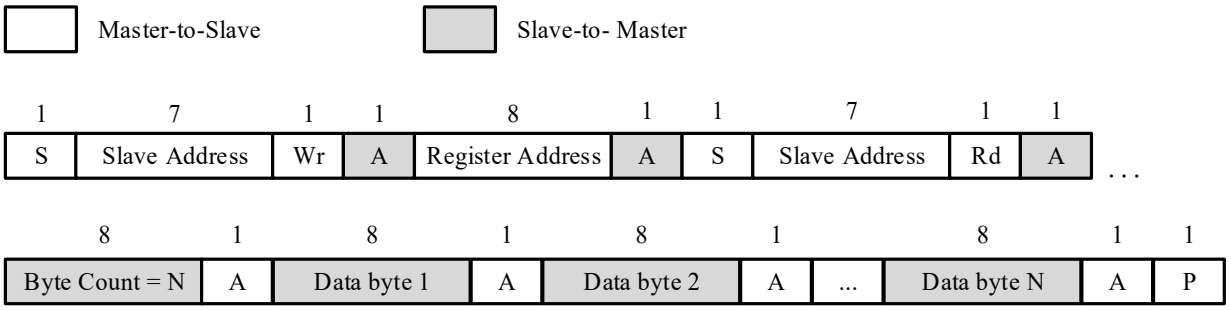
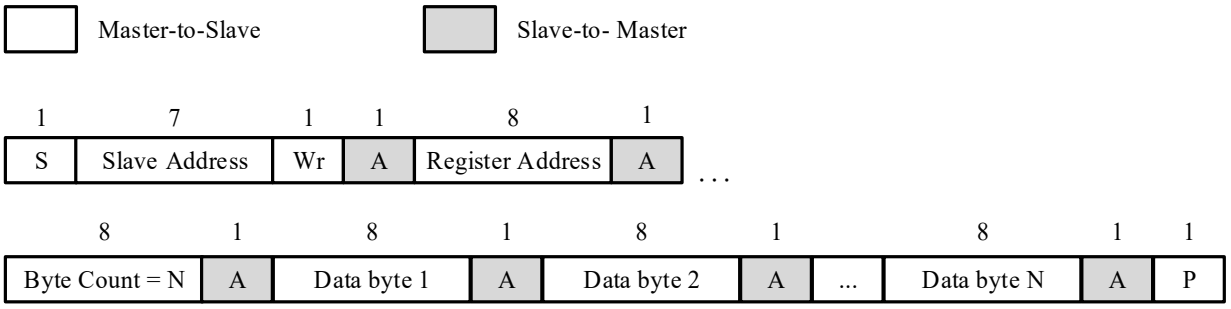


Figure 5-8 Block write schematic diagram



5.7 EEPROM Configuration

CH338 supports loading configuration information such as vender identification code VID, product identification code PID, USB string descriptor and function configuration from external or internal EEPROM. If the information in the EEPROM is invalid, the default configuration information will be automatically loaded. Table 5-7 describes the specific configuration information of EEPROM.

Table 5-7 Internal/External EEPROM configuration information

Offset address	Parameter abbreviation	Parameter description	Default value
00h	VID_L	The low byte of the vender identification code VID	86h
01h	VID_H	The high byte of the vender identification code VID	1Ah
02h	PID_L	The low byte of the product identification code PID CH338 series are 9Eh, CH339 series are 9Fh	9Eh or 9Fh
03h	PID_H	The high byte of the product identification code PID	80h
04h	bcdDevice_L	bcdDevice low byte, used for indicating chip package model Fixed, cannot modified	Follow model
05h	bcdDevice_H	bcdDevice high byte, used for indicating chip version Fixed, cannot modified	Follow model
06h	Fun_Cfg1	Functional configuration byte 1 Bit7: Power supply mode selection; 0: Bus powered mode (Default); 1: Self-powered mode; Bit6: Reserved; Bit5: High-speed mode prohibition control; 0: High-speed mode enabled (Default); 1: High speed mode disabled; Bit4: STT and MTT mode selection; 0: STT mode; 1: MTT mode (Default); Bit3: Reserved; Bit2-1: Port overcurrent function control; 00: Overall overcurrent control;	Follow model

		01: Independent overcurrent control; 1x: Does not support overcurrent control; Bit0: Port power control; 0: Overall power control; 1: Independent power control;	
07h	Fun_Cfg2	Functional configuration byte 2 Bit7: Reserved; Bit6: Reserved; Bit5: Reserved; Bit4: Reserved; Bit3: Whether HUB is Compound Device; 0: No; 1: Yes; Bit2-0: Reserved;	20h
08h	Fun_Cfg3	Functional configuration byte 3 Bit7-4: Reserved; Bit3: Port remapping function control; 0: Disabled (Default); 1: Enabled; Bit2-1: Reserved; Bit0: String descriptor enable control; 0: Disabled (Default); 1: Enabled;	00h
09h	Dev_ Removable	Whether the downstream port device can be removed is controlled Bit7-1: Is the device on downstream port 7-1 removable? 0: Removable (Default); 1: Not removable; Bit0: Reserved, must be 0;	00h
0Ah	Port_Dis_Sp	Port disabled in self-powered mode Bit7-1: Is downstream port 7-1 prohibited? 0: Disabled (Default); 1: Enabled; Bit0: Reserved, must be 0;	00h
0Bh	Port_Dis_Bp	Port disabled in bus powered mode Bit7-1: Is downstream port 7-1 prohibited? 0: Disabled (Default); 1: Enabled; Bit0: Reserved, must be 0;	00h
0Ch	MaxPwr_Sp	Maximum operating current in self-power mode, unit is 2mA	01h
0Dh	MaxPwr_Bp	Maximum operating current in bus power supply mode, unit is 2mA	64h

0Eh	HubCurrent_Sp	Maximum current required by HUB in self-power mode	01h
0Fh	HubCurrent_Bp	Maximum current required by HUB in bus power mode	64h
10h	Pwr_OnTime	Delay time from when the downstream port is powered on to when the power supply becomes valid	32h
11h	LanguageID_H	Language ID high byte	00h
12h	LanguageID_L	Language ID low byte	00h
13h	Vendor_StrLen	Vendor string descriptor length	00h
14h	Product_StrLen	Product string descriptor length	00h
15h	SN_StrLen	Serial number string descriptor length	00h
16h-53h	Vendor String	Vendor string descriptor Vendor string descriptor in Unicode format	00h
54h-91h	Product String	Product string descriptor Product string descriptor in Unicode format	00h
92h-CFh	Serial Number String	Serial number string descriptor Serial number string descriptor in Unicode format	00h
D0h	PortNum	Number of downstream ports, valid range: 1-7	Follow model
D1h	bcdUSB_L	USB version low byte bcdUSB_L=0x00, USB2.00 bcdUSB_L=0x01, USB2.01 bcdUSB_L=0x10, USB2.10	00h
D2h	Fun_Cfg4	Functional configuration byte 4 Bit7-2: Reserved, must be 0; Bit1: Force the downstream port to full-speed mode; 0: High speed mode (Default); 1: Full-speed mode; Bit0: Indicator function enable configuration; 0: Disabled (Default); 1: Enabled;	00h
D3h	Fun_Cfg5	Functional configuration byte 5 Bit7: LED indicator polarity configuration; 0: Active low (Default); 1: Active high; Bit6: Port overcurrent detection polarity configuration; 0: Active low (Default); 1: Active high; Bit5: Port power control polarity configuration; 0: Active low (Default); 1: Active high; Bit4-0: Reserved;	00h
D4-FAh	Reserved	Reserved	00h
FBh	Port_Remap12	Downstream port 1-2 remapping configuration Bit7-4: Physical port 2 remapping 0000: Physical port 2 prohibits remapping;	00h

		0001: Physical port 2 is mapped to logical port 1; 0010: Physical port 2 is mapped to logical port 2; 0011: Physical port 2 is mapped to logical port 3; 0100: Physical port 2 is mapped to logical port 4; 0101: Physical port 2 is mapped to logical port 5; 0110: Physical port 2 is mapped to logical port 6; 0111: Physical port 2 is mapped to logical port 7; 1000-1111: Invalid; Bit3-0: Physical port 1 remapping 0000: Physical port 1 prohibits remapping; 0001: Physical port 1 is mapped to logical port 1; 0010: Physical port 1 is mapped to logical port 2; 0011: Physical port 1 is mapped to logical port 3; 0100: Physical port 1 is mapped to logical port 4; 0101: Physical port 1 is mapped to logical port 5; 0110: Physical port 1 is mapped to logical port 6; 0111: Physical port 1 is mapped to logical port 7; 1000-1111: Invalid;	
FCh	Port_Remap34	Downstream port 3-4 remapping configuration Bit7-4: Physical port 4 remapping 0000: Physical port 4 prohibits remapping; 0001: Physical port 4 is mapped to logical port 1; 0010: Physical port 4 is mapped to logical port 2; 0011: Physical port 4 is mapped to logical port 3; 0100: Physical port 4 is mapped to logical port 4; 0101: Physical port 4 is mapped to logical port 5; 0110: Physical port 4 is mapped to logical port 6; 0111: Physical port 4 is mapped to logical port 7; 1000-1111: Invalid; Bit3-0: Physical port 3 remapping 0000: Physical port 3 prohibits remapping; 0001: Physical port 3 is mapped to logical port 1; 0010: Physical port 3 is mapped to logical port 2; 0011: Physical port 3 is mapped to logical port 3; 0100: Physical port 3 is mapped to logical port 4; 0101: Physical port 3 is mapped to logical port 5; 0110: Physical port 3 is mapped to logical port 6; 0111: Physical port 3 is mapped to logical port 7; 1000-1111: Invalid;	00h
FDh	Port_Remap56	Downstream port 5-6 remapping configuration Bit7-4: Physical port 6 remapping 0000: Physical port 6 prohibits remapping; 0001: Physical port 6 is mapped to logical port 1; 0010: Physical port 6 is mapped to logical port 2;	00h

		0011: Physical port 6 is mapped to logical port 3; 0100: Physical port 6 is mapped to logical port 4; 0101: Physical port 6 is mapped to logical port 5; 0110: Physical port 6 is mapped to logical port 6; 0111: Physical port 6 is mapped to logical port 7; 1000-1111: Invalid; Bit3-0: Physical port 5 remapping 0000: Physical port 5 prohibits remapping; 0001: Physical port 5 is mapped to logical port 1; 0010: Physical port 5 is mapped to logical port 2; 0011: Physical port 5 is mapped to logical port 3; 0100: Physical port 5 is mapped to logical port 4; 0101: Physical port 5 is mapped to logical port 5; 0110: Physical port 5 is mapped to logical port 6; 0111: Physical port 5 is mapped to logical port 7; 1000-1111: Invalid;	
FEh	Port_Remap7	Downstream port 7 remapping configuration Bit7-4: Physical port 7 remapping 0000: Physical port 7 prohibits remapping; 0001: Physical port 7 is mapped to logical port 1; 0010: Physical port 7 is mapped to logical port 2; 0011: Physical port 7 is mapped to logical port 3; 0100: Physical port 7 is mapped to logical port 4; 0101: Physical port 7 is mapped to logical port 5; 0110: Physical port 7 is mapped to logical port 6; 0111: Physical port 7 is mapped to logical port 7; 1000-1111: Invalid; Bit3-0: Reserved;	00h
FFh	Reserved	Reserved	00h

5.8 Bus Powered and Self-powered

CH338 supports USB bus power supply mode and self-power supply mode. The bus power supply comes from the USB upstream port, and the power supply capacity is 500mA, 900mA, 1.5A and other standards. The internal resistance loss of the USB cable and the consumption of the HUB itself will reduce the power supply capacity to the downstream port, and the voltage of the downstream port may be low. Self-powered usually comes from an external power port and depends on the external power supply capability.

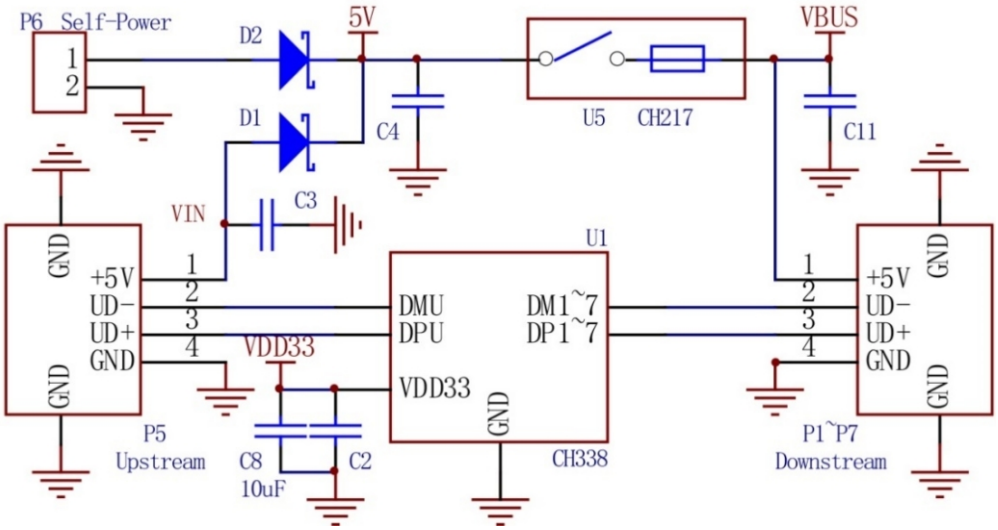
Since the voltages of self-power supply and bus power supply are difficult to be completely equal, the HUB needs to avoid direct short-circuiting between the two to generate large currents. In addition, when the USB upstream port is powered off, the HUB must also prevent the self-powered external power supply from injecting current into the USB bus and USB host.

5.8.1 Bidirectional Isolation Schematic

Diodes D1 and D2 are used to bidirectionally isolate the V_{BUS} bus power supply and the P6 port external power

supply to prevent the two power supplies from flowing back to each other. High-power Schottky diodes are used to reduce their own voltage drop. The downstream port V_{BUS} gets a voltage of 4.7V or even lower, only to indicate.

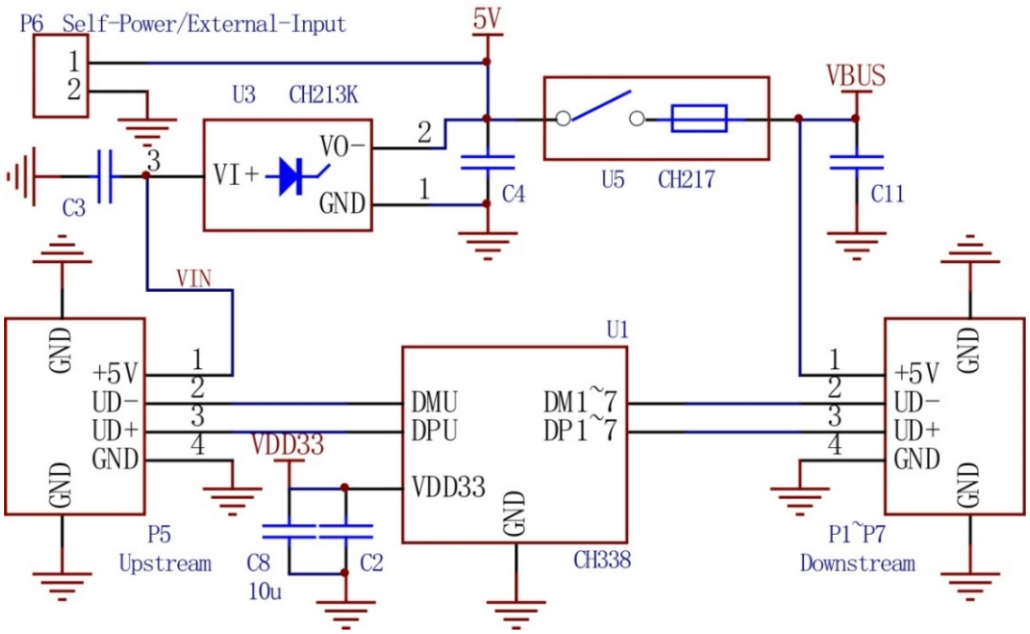
Figure 5-9 Schematic diagram of Schottky diode bidirectional isolation of V_{BUS} and external power supply



5.8.2 Practical Single Isolation Solution

The function of an ideal diode is to conduct one-way conduction with low voltage drop. U3 is used to prevent the external power supply of the P6 port from flowing back to the upstream port V_{BUS}. At 500mA current, the voltage drop of U3 is about one-third of the voltage drop of the Schottky diode. Downstream Port V_{BUS} can get 4.9V voltage.

Figure 5-10 Schematic diagram of ideal diode isolating V_{BUS} and external power supply



6. Parameter

6.1 Absolute Maximum Value

(Critical or exceeding the absolute maximum value may cause the chip to work abnormally or even be damaged)

Name	Parameter description	Min.	Max.	Unit
T_A	Ambient temperature during operation	-40	85	℃
T_J	Junction temperature range	-40	100	℃
T_S	Ambient temperature during storage	-55	150	℃
V_{DD5}	LDO input power supply voltage (V_{DD5} pin is connected to power supply, GND pin is connected to ground)	-0.4	5.8	V
V_{DD33}	Working power supply voltage (V_{DD33} pin is connected to power supply, GND pin is connected to ground)	-0.4	4.0	V
V_{5I}	5V tolerant voltage on input pin	-0.4	5.3	V
V_{USB}	Voltage on USB signal pin	-0.4	V_{DD33}+0.4	V
V_{GPIO}	The voltage on other (3.3V) input or output pins	-0.4	V_{DD33}+0.4	V
V_{ESDUSB}	HBM mannequin ESD tolerant voltage on USB signal pins	6K		V
V_{ESDIO}	HBM mannequin ESD tolerant voltage on other pins	2K		V

6.2 Electrical Parameters

(Test Conditions: T_A=25℃, V_{DD5}=5V or V_{DD33}=3.3V)

Name	Parameter description			Min.	Typ.	Max.	Unit
V_{DD5}	LDO input supply voltage @V_{DD5}		Enable internal LDO	3.8	5.0	5.5	V
V_{DD33}	LDO output voltage @V_{DD33}		Enable internal LDO	3.2	3.3	3.4	V
	External 3.3V voltage @V_{DD33}		No need for internal LDO	3.2	3.3	3.4	
I_{LDO}	Internal power regulator LDO external 3.3V load capability					100	mA
I_{CC}	Working current	Upstream high-speed	7 downstream high-speed		140		mA
		Upstream high-speed	1 downstream high-speed		65		mA
		Upstream high-speed	7 downstream full-speed		50		mA
		Upstream high-speed	1 downstream full-speed		49		mA
		Upstream full-speed	7 downstream full-speed		34		mA
		Upstream full-speed	1 downstream full-speed		33		mA

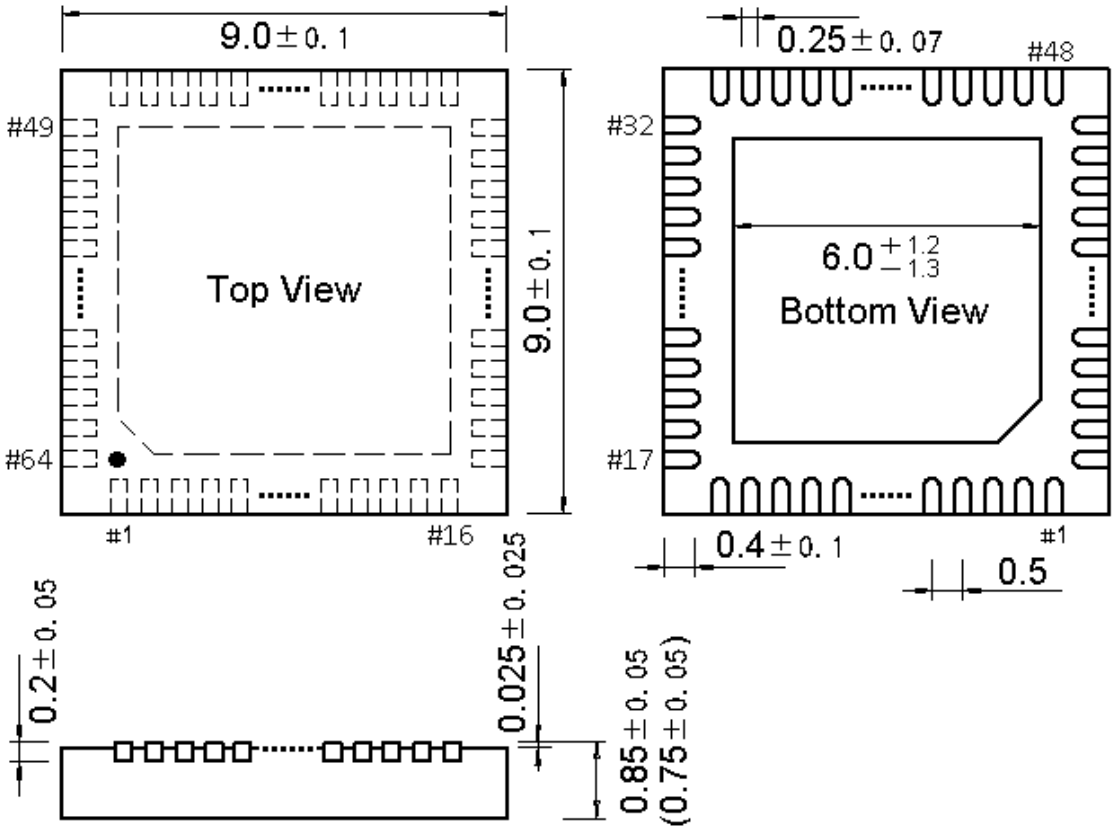
		Upstream high-speed Upstream full-speed	Downstream no device contains 1.5KΩ pull-up		0.5		mA
I_{SLP}	Deep sleep supply current (Excluding 1.5KΩ pull-up) Or: Own sleep power current (Not connected to USB host)				0.28		mA
V_{IL}	low level input voltage		Standard I/O pin	0		0.8	V
			5I pin	0		0.8	V
V_{IH}	High level input voltage		Standard I/O pin	2.0		V_{DD33}	V
			5I pin	2.0		5.0	V
V_{ILRST}	Low level input voltage of RESET# pin			0		0.8	V
V_{OL}	Low level output voltage		Sink current 5mA		0.4	0.6	V
V_{OH}	High level output voltage		Source current 5mA	V_{DD33}-0.6	V_{DD33}-0.4		V
R_{PU}	Pull-up equivalent resistance			30	40	55	kΩ
R_{PD}	Pull-down equivalent resistance			30	40	55	kΩ
V_{lvr}	Voltage threshold for power low voltage reset			2.4	2.9	3.2	V

7. Package

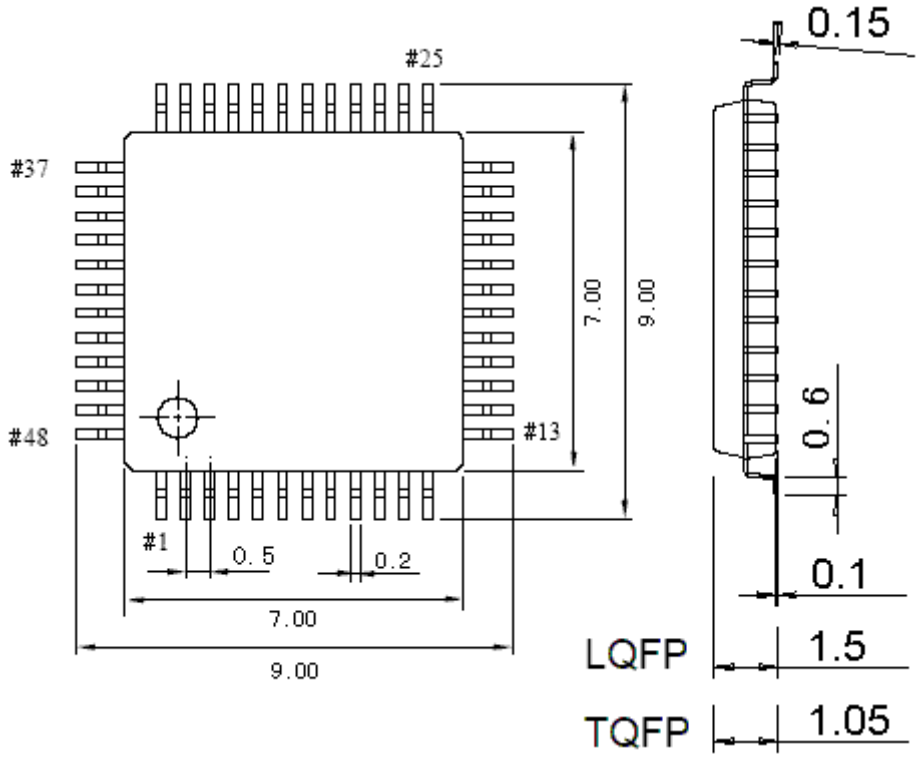
Note: The unit of dimensioning is mm (Millimeter).

The pin center spacing is the nominal value without error, and the dimensional error other than that is no more than ±0.2mm.

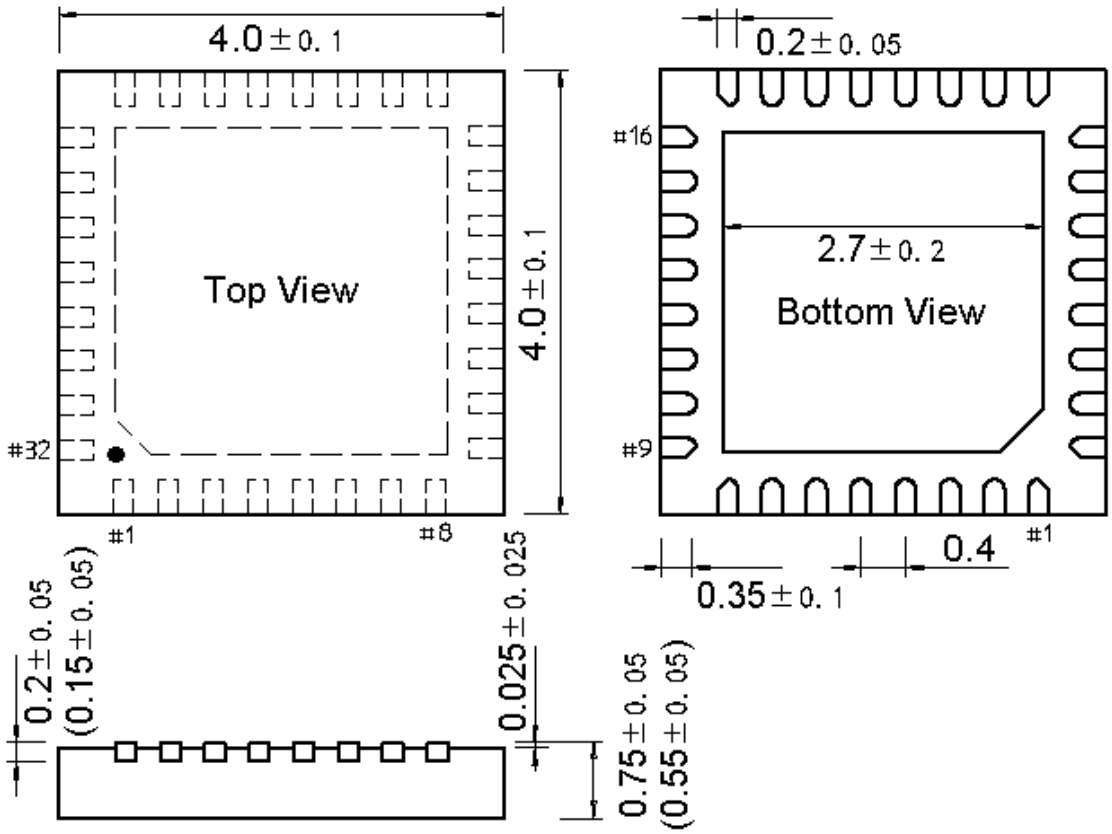
7.1 QFN64×9



7.2 LQFN48



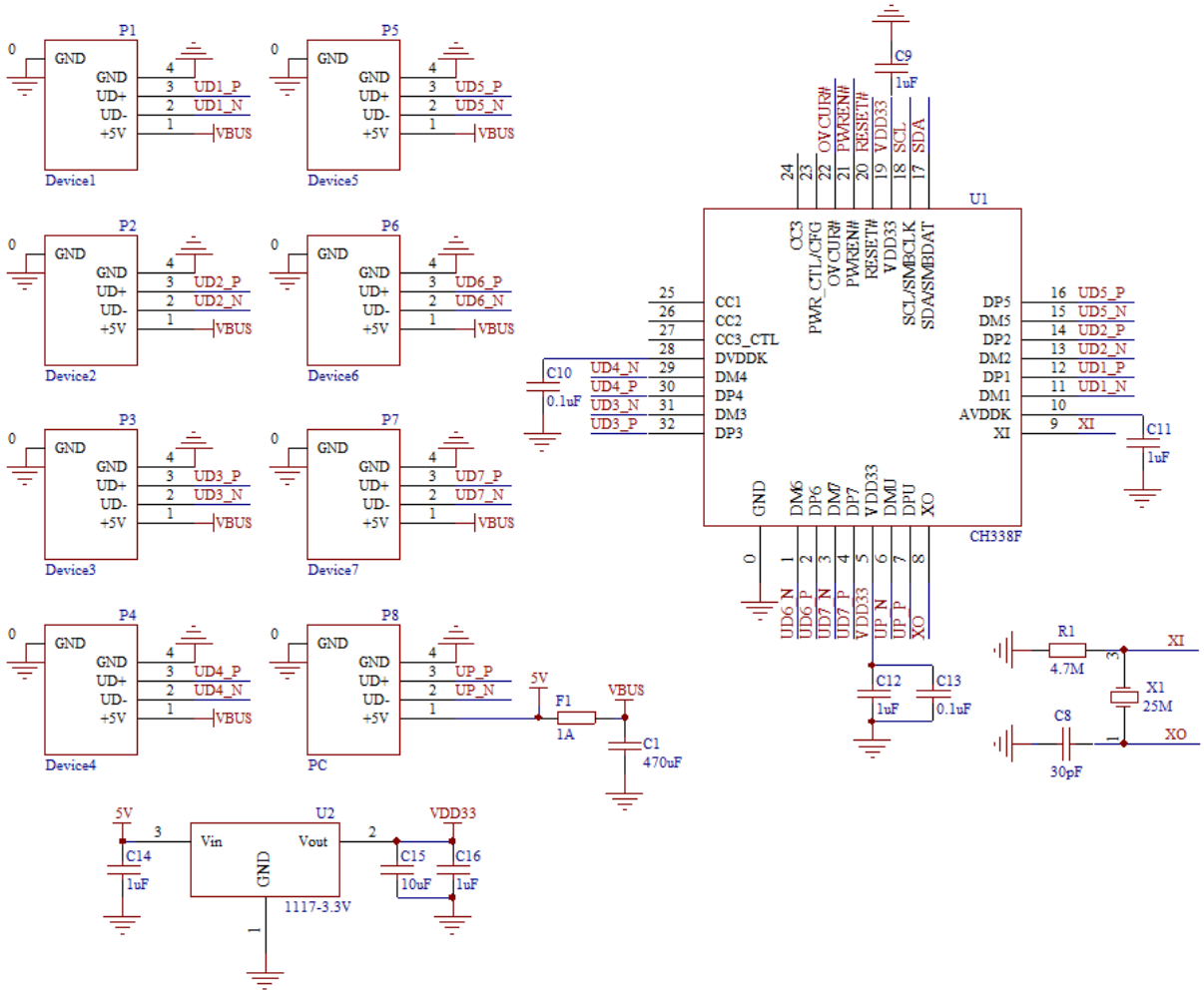
7.3 QFN32



8. Application

8.1 Simplified Application, Bus Powered

Figure 8-1 CH338F bus power supply simplified schematic

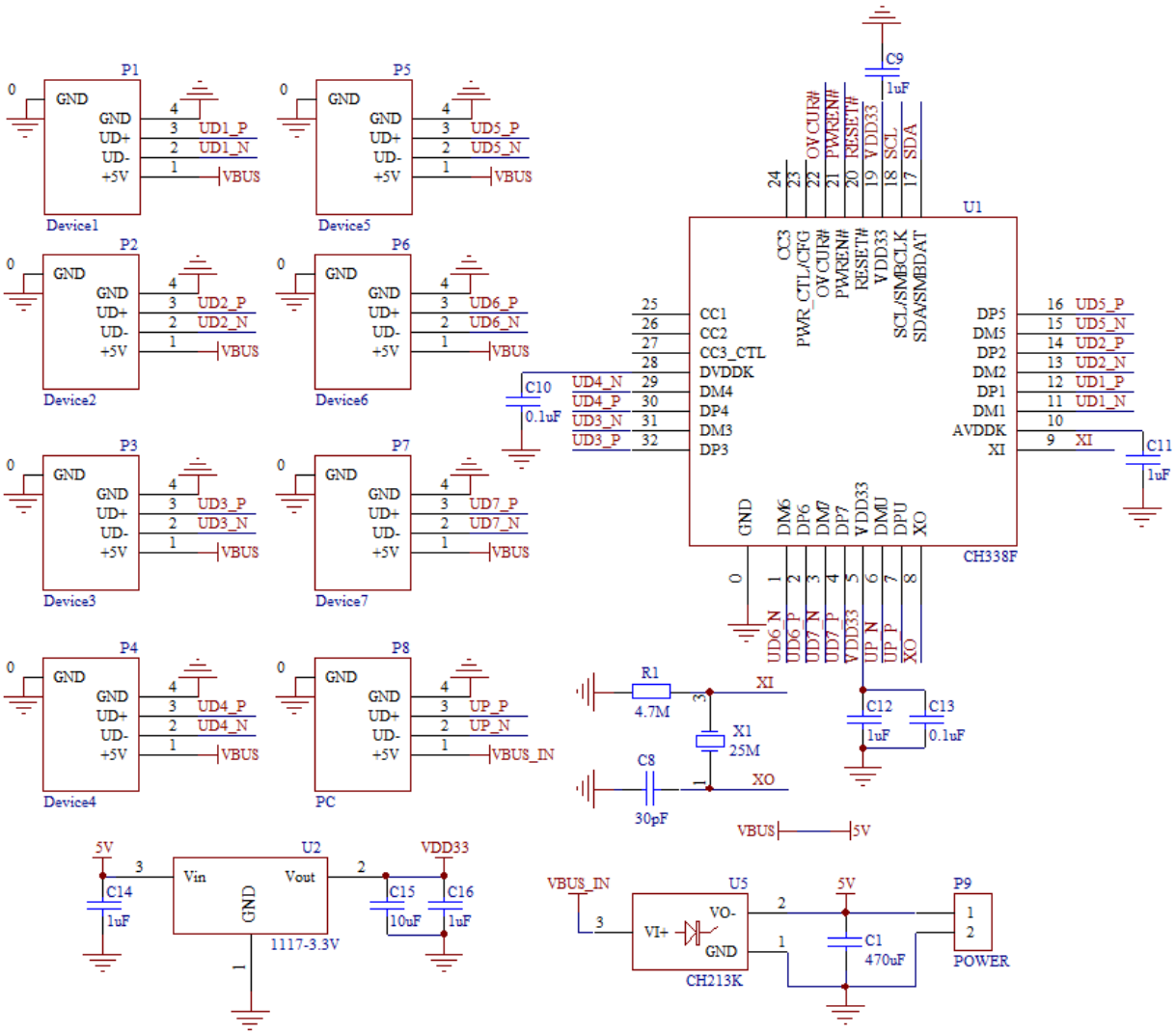


In the figure above, P1-P7 are the seven downstream USB ports of the HUB, and P8 is the upstream USB port of the HUB. The fuse resistor Fuse between 5V and V_{BUS} can be replaced with a USB current-limiting power switch chip, which will provide faster protection response and better effect. Note that the fuse resistor and USB power switch chip may not support high temperatures.

At the moment when the USB device on the downstream port is hot-swapped, the dynamic load may cause the V_{BUS} and 5V voltages to drop instantaneously, which may cause an LVR low-voltage reset, causing the entire HUB to be disconnected and reconnected. Improvement methods: ① Increase the electrolytic capacitor of the 5V power supply within the scope allowed by the specification (Increase the capacity of C1 in the illustration) to alleviate the drop; ② Increase the capacitance at the power input end of the HUB chip (Increase the capacity of C12 in the illustration, for example 22uF); ③ Enhance the 5V power supply capability or change it to self-power supply. In addition, improving the quality of the USB cable will also improve the power supply capability.

8.2 Simplified Application, Bus Powered

Figure 8-2 CH338F self-powered simplified schematic diagram



The main difference from Figure 8-1 is that it has an external power supply port P9. U5 is a low-voltage ideal diode CH213, which is used to prevent the external power supply of P9 from flowing back to the V_{BUS_IN} of the upstream port P8, especially when the upstream port, such as the computer, is shut down and P9 is still powered externally. Case. Theoretically U5 can be replaced with a Schottky diode, but you need to choose a device with a lower voltage drop of its own, otherwise it will reduce the output voltage of the downstream port V_{BUS}. At 300mA load current, the voltage drop of the Schottky diode is about 0.3V, and that of the ideal diode is about 0.05V.

Since P9 itself and the external power supply usually have no load, the backflow from P8 to P9 is generally not considered.

The low-voltage drop diode CH213 has simple overcurrent and short-circuit protection functions, and the protection response is faster, which can replace and eliminate the fuse resistor Fuse between 5V and V_{BUS} in Figure 8-1. The external power supply connected to P9 needs to have overcurrent and short-circuit protection capabilities. Otherwise, a fuse resistor needs to be added between P9 and 5V, or a USB current-limiting power switch chip needs to be added between 5V and V_{BUS}.

8.3 Independent Overcurrent Detection Application

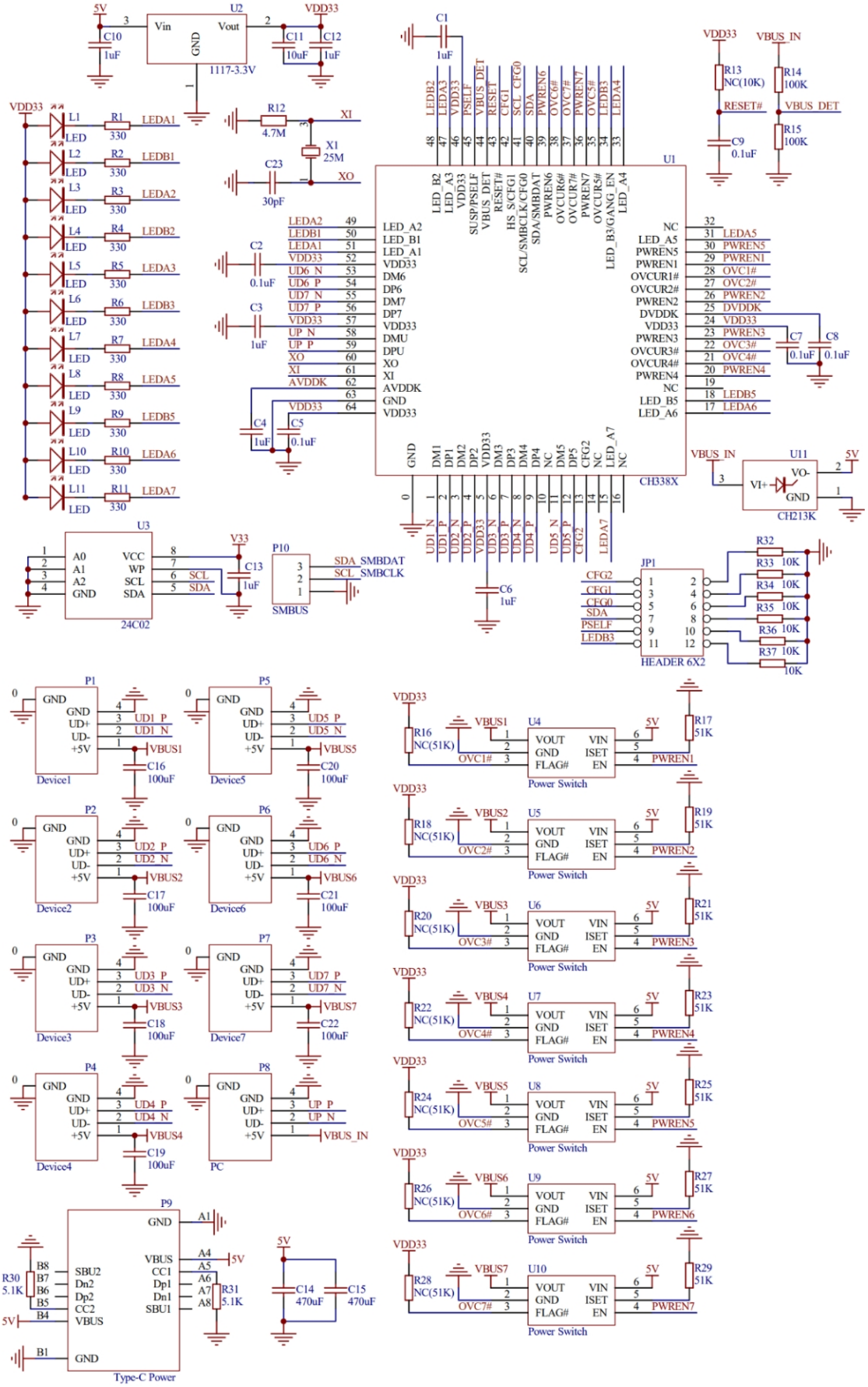
The figure below is an application reference diagram of independent power distribution control and independent over-current detection for each HUB port, which can be used for computers and HUB hubs. In the figure, R17, R19, R21, R23, R25, R27 and R29 set the current limiting threshold according to the power supply capacity. The FLAG# pin of the USB current limiting power switch chip can generate an overcurrent or overtemperature alarm signal to notify the HUB controller and computer, the OVCUR# pin of CH338 has a built-in pull-up resistor (Default OC_LEVEL=0).

P9 is an external self-powered input port. In the current picture of the Type-C interface, the ideal diode U11 is used to prevent the external power supply from flowing back to the upstream port USB power. If there is no P9 or no backflow prevention is considered, then U11 is not needed.

When designing the PCB, it is necessary to consider the actual operating current carrying capacity, V_{BUS_IN}, 5V, V_{BUS*} and P9 and each port GND alignment path PCB as wide as possible, if there is an over-hole it is recommended that more than one parallel connection.

It is recommended to add an overvoltage protection device for 5V and an ESD protection device for all USB signals, e.g. CH412K, whose V_{CC} should be connected to 3.3V.

Figure 8-3 CH338X independent overcurrent detection application diagram



8.4 Overall Overcurrent Detection Application

The figure below is the application reference diagram of GANG power distribution control and overall overcurrent detection for all ports of the HUB. CH217 is a USB power distribution switch chip that supports overcurrent protection.

Figure 8-4 CH338F overall overcurrent detection application diagram