7-Port Multi-function USB HUB Controller Chip CH339

Datasheet

Version: V1.0

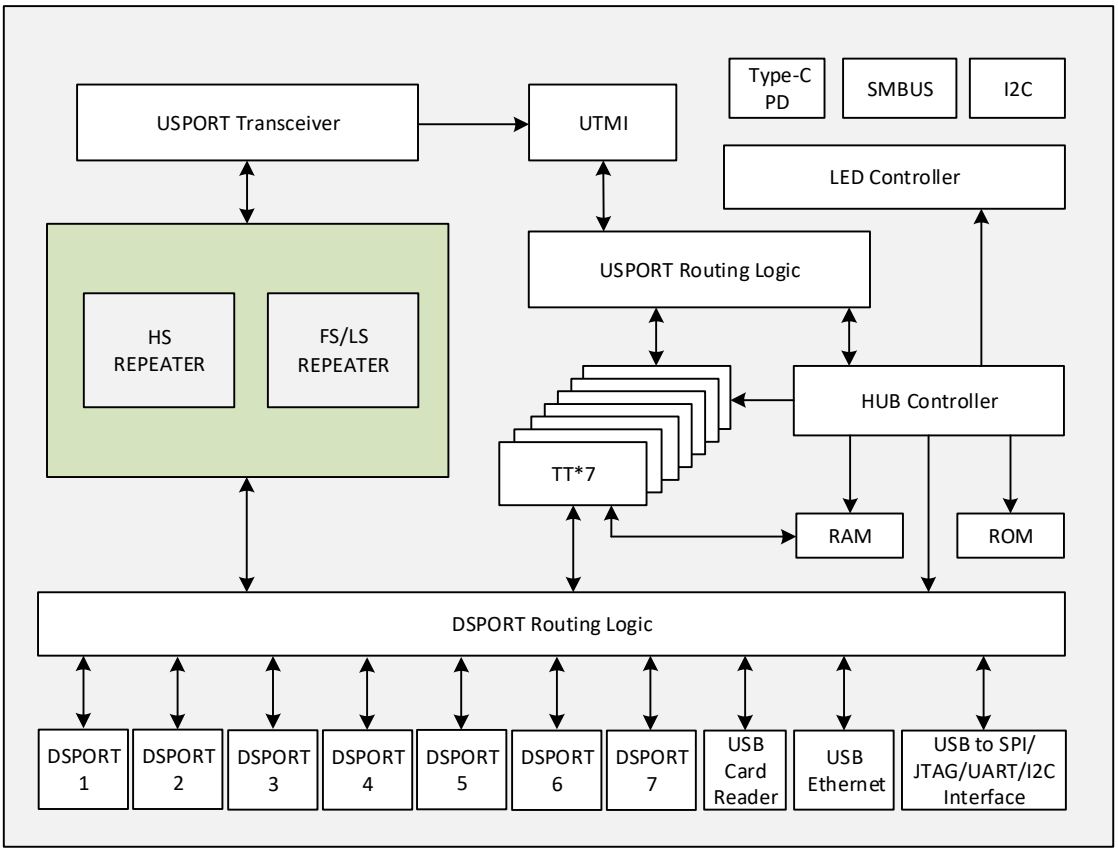
https://wch-ic.com

1. Overview

CH339 is a 7-port multi-function USB HUB controller chip compliant with USB2.0 protocol specification. It integrates 7-port USB HUB, USB 100 Gigabit Ethernet, USB high-speed SD card reader, USB PD, and USB to SPI, USB to JTAG, USB to UART, and USB to I2C interfaces in a single chip. The CH339 upstream port supports USB2.0 high-speed and full-speed, while the downstream port supports USB2.0 high-speed 480Mbps, full-speed 12Mbps and low-speed 1.5Mbps, as well as several internal direct channels such as USB NIC, USB high-speed card reader, USB to JTAG and so on. CH339 supports high-performance concurrent processing MTT mode, adopts industrial design and streamlined peripherals, and can be used in computer and industrial computer motherboards, docking stations, peripherals, embedded systems and other scenarios.

The following figure is the system block diagram of CH339.

Figure 1-1 System block diagram



The above figure is the internal structure block diagram of the HUB controller system. The HUB controller mainly consists of three modules: Repeater, TT and controller. The controller is similar to the MCU processor and is used for global management and control. When the upstream port is at the same speed as the downstream port, the routing logic connects the port to Repeater, and when the upstream port is inconsistent with the downstream port, the routing logic connects the port to TT.

TT is divided into single TT and multiple TT, that is, STT and MTT, STT are a single TT core time-sharing

scheduling to handle transactions sent by USB hosts to all downstream ports, and MTT refers to multiple TT parallel, where seven TT cores correspond to one downstream port transaction in real time, so MTT can provide full bandwidth for access devices of each downstream port and better support concurrent transmission of multi-port and large amount of data.

Note:

USPORT Transceiver: Upstream port transceiver PHY;

DSPORT 1-7: Downstream port transceiver PHY;

REPEATER: HUB Repeater;

TT: Transaction translator.

2. Features

(1) USB HUB

- 7-port USB HUB, provide 7 USB2.0 downstream port, downwards compatible with USB1.1 protocol specifications
- Support each port independent power control or GANG overall linkage power control
- Support each port independent overcurrent detection or GANG overall overcurrent detection
- Support high-performance MTT mode, and provides independent TT for each port to achieve full-bandwidth concurrent transmission. The total bandwidth is 7 times that of STT.
- Self-developed dedicated USBPHY, low-power consumption technology, supporting self-power supply or bus power supply
- Functions such as self-power supply or bus power supply mode can be configured through the I/O pin.
- Provide crystal oscillator, support external clock input, built-in PLL provides 480MHz clock for USBPHY
- Non-Ethernet applications can support crystal-free mode, saving external crystals and capacitors
- The upstream port has built-in 1.5KΩ pull-up resistor, and the downstream port has built-in pull-down resistance required by the USB Host, streamlining the periphery.

(2) USB to Ethernet and USB High-speed Card Reader

- Built-in self-developed 10M/100M Ethernet MAC+PHY, compatible with IEEE 802.3 10BASE-T/100BASE-TX
- Support CDC-ECM protocol and CDC-NCM protocol, free-install driver program or optional vendor driver program
- 10M/100M auto-negotiation, support UTP CAT5E, CAT6 twisted pair, support Auto-MDIX, automatic identification of positive and negative signal lines
- Support hibernation mode and low-power sleep mode, support network low-power configuration and dynamic power management
- Support remote wake-up through events such as magic packets and network wake-up packets
- Support IPv4/IPv6 packet verification, IPv4 TCP/UDP/HEAD and IPv6 TCP/UDP packet verification generation and inspection
- Support SD and MMC cards and convert them to standard USB mass storage devices
- Provide SDIO interface, compatible with SD card specification 2.0, compatible with MMC specification 4.5

(3) USB to SPI Interface

- As Host/Master mode, providing four signal lines: SCS line, SCK/CLK line, MISO/SDI line, MOSI/SDO
- Support 8-bit data structure, support MSB or LSB transmission
- Support SPI mode 0/1/2/3, support transmission frequency configuration, up to 60MHz, support hardware DMA to transmit and receive
- With the cooperation of computer API, 4-wire interface devices such as FLASH, MCU and sensors can be operated flexibly.

(4) USB to JTAG Interface

- As Host/Master mode
- JTAG interface provides TMS line, TCK line, TDI line, TDO line, TRST line (optional) and SRST line (optional).
- Support high-speed USB data transmission

- Through the cooperation of computer API, it can operate CPU, DSP, FPGA, CPLD, MCU and other devices flexibly.

(5) USB to UART Interface

- Emulate the standard serial port, which can be used to upgrade the original serial port peripherals or add additional serial ports through USB
- The serial port applications under the computer-side Windows operating system are fully compatible and do not need to be modified.
- Hardware full-duplex serial port, built-in independent transceiver buffer, communication baud rate support 2400bps~6Mbps
- Serial port supports 8 data bits, supports parity, parity and no parity, and supports 1 or 2 stop bits.
- Support CTS and RTS hardware automatic flow control
- Through external level conversion devices, support RS232, RS485, RS422 and other interfaces

(6) USB to I2C Interface

- As Host/Master mode
- Provide two signal lines, SCL and SDA, and support 5 transmission speeds
- Through the cooperation of computer API, it can flexibly operate the devices with 2-wire interface, such as A/D, D/A, EEPROM and sensors.

(7) Other Interfaces

- Whether the HUB chip supports composite devices, non-removable devices, custom VID, PID, port configuration and USB vendors, products, serial number string descriptors, etc., can be configured through external EEPROM or internal HUB.
- Built-in information memory, mass customization of manufacturer or product information and configuration according to the special needs of the industry
- Processor core, high-speed USB, Ethernet and other controllers and physical layer transceiver IP are fully self-developed, with close cooperation of each module, high efficiency and low cost, and exemption from IP authorization fee.
- USB interface pin with 6kV enhanced ESD performance, Class 3A
- Industrial-grade temperature range: -40~85℃
- Provide QFN68, QFN32 and other packaging forms

Figure 1-1 Functional comparison

Function \ Model	CH339W	CH339F
TT mode	MTT	MTT
USB port number	7	4
Overcurrent detection	Independent or GANG	GANG mode
Power control	Independent or GANG	GANG mode
I/0 pin configuration power supply	√	×
External/internal EEPROM	√	√

Provide configuration information		
Custom configuration information	√	√
Upstream switching function	√	×
Isolation / extension function	√	√
USB NIC function	√	√
USB card reader function	√	√
USB to JTAG function	√	×
USB to SPI function	√	×
USB to UART function	√	×
USB to I2C function	√	×
USB to SMBus function	√	×
Type-C / PD	√	×
Chip power supply	Single 3.3V	Single 3.3V

3. Package

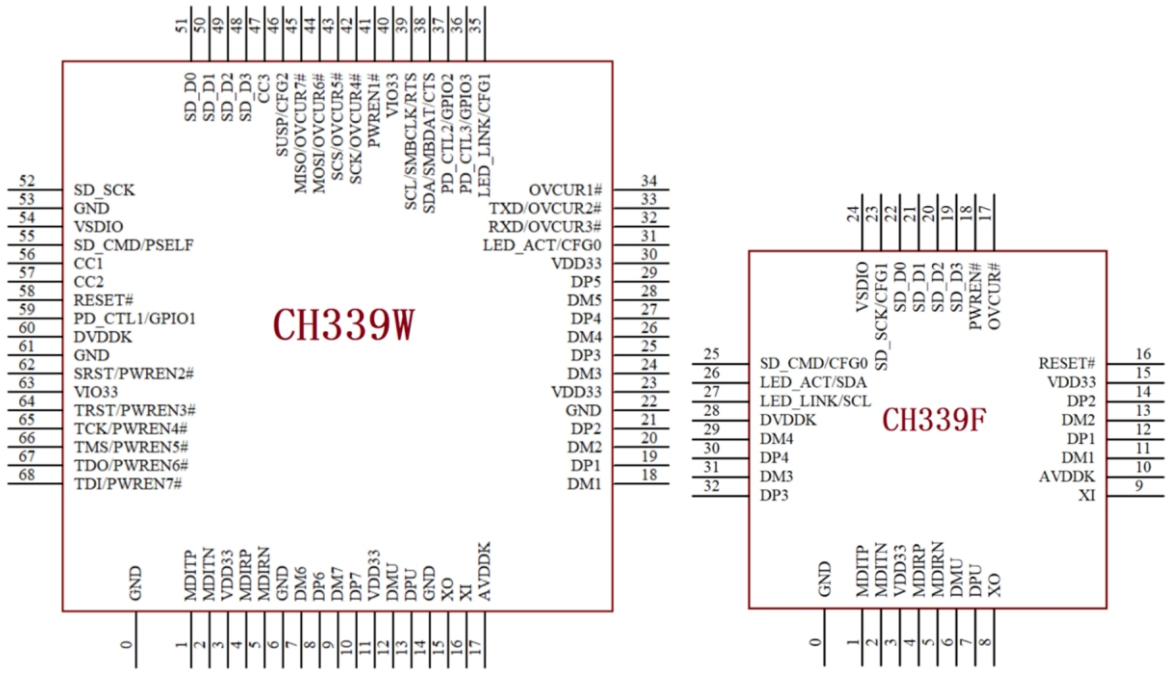


Table 3-1 Package description

Package form	Body size	Pin pitch		Package description	Order model
QFN68	8*8mm	0.4mm	15.7mil	Quad Flat No-leads Package	CH339W
QFN32	4*4mm	0.4mm	15.7mil	Quad Flat No-leads Package	CH339F

Note:

CH339F is preferred, which is small in size; CH339W has many pins and focuses on complete functions.

The 0# pin is the EPAD of the QFN package and is a necessary connection.

4. Pins

Table 4-1 Pin definition

Pin number (Pin of the same name can be referenced)		Pin name	Type(1)	Function description
CH339W	CH339F			
12	6	DMU	USB	Upstream port USB2.0 signal line D-
13	7	DPU	USB	Upstream port USB2.0 signal line D+
18	11	DM1	USB	1#Downstream port USB signal line D-
19	12	DP1	USB	1# Downstream port USB signal line D+
20	13	DM2	USB	2# Downstream port USB signal line D-
21	14	DP2	USB	2# Downstream port USB signal line D+
24	31	DM3	USB	3# Downstream port USB signal line D-
25	32	DP3	USB	3# Downstream port USB signal line D+
26	29	DM4	USB	4# Downstream port USB signal line D-
27	30	DP4	USB	4# Downstream port USB signal line D+
28	-	DM5	USB	5# Downstream port USB signal line D-
29	-	DP5	USB	5# Downstream port USB signal line D+
7	-	DM6	USB	6# Downstream port USB signal line D-
8	-	DP6	USB	6# Downstream port USB signal line D+
9	-	DM7	USB	7# Downstream port USB signal line D-
10	-	DP7	USB	7# Downstream port USB signal line D+
16	9	XI	I	The input end of the crystal oscillator is connected to one end of the external crystal
15	8	XO	O	The inverted output end of the crystal oscillator is connected to the other end of the external crystal
58	16	RESET#	5I	External reset input, built-in pull-up resistor, low level effective, can be suspended when not in use, short V_{IO33} is recommended to prevent interference
3、23	3、15	V_{DD33}	P	Analog power input, external supply 3.3V, external 1uF capacitor
11、30	-	V_{DD33}	P	Auxiliary power input, external supply 3.3V, external 0.1uF or 1uF capacitor
40、63	-	V_{IO33}	P	Pin power input, external supply 3.3V, external 0.1uF or 1uF capacitor
54	24	V_{SDIO}	P	Decoupling end of internal power supply of SDIO pin, external 0.1uF decoupling capacitor
17	10	AV_{DDK}	P	Analog core power supply, external 1uF decoupling capacitor
60	28	DV_{DDK}	P	Digital core power supply, external 0.1uF decoupling capacitor
0	0	GND	P	Common ground terminal, must be connected to GND
6、14、22、	-	GND	P	Public ground terminal, optional, GND connection is

53、61				recommended
34	17	OVCUR1# OVCUR#	5I	Downstream port 1 overcurrent detection input pin, low level overcurrent; Overall mode downstream port overcurrent detection input pin, low level overcurrent
33	-	OVCUR2#	5I	Downstream port 2 overcurrent detection input pin, low level overcurrent
32	-	OVCUR3#	5I	Downstream port 3 overcurrent detection input pin, low level overcurrent
42	-	OVCUR4#	5I	Downstream port 4 overcurrent detection input pin, low level overcurrent
43	-	OVCUR5#	5I	Downstream port 5 overcurrent detection input pin, low level overcurrent
44	-	OVCUR6#	5I	Downstream port 6 overcurrent detection input pin, low level overcurrent
45	-	OVCUR7#	5I	Downstream port 7 overcurrent detection input pin, low level overcurrent
41	18	PWREN1# PWREN#	O	Downstream port 1 power output control pin, low level on; Whole mode downstream port power output control pin, low level on.
62	-	PWREN2#	O	Downstream port 2 power output control pin, low level on
64	-	PWREN3#	O	Downstream port 3 power output control pin, low level on
65	-	PWREN4#	O	Downstream port 4 power output control pin, low level on
66	-	PWREN5#	O	Downstream port 5 power output control pin, low level on
67	-	PWREN6#	O	Downstream port 6 power output control pin, low level on
68	-	PWREN7#	O	Downstream port 7 power output control pin, low level on
51	22	SD_D0	I/O	SDIO interface data pin 0
50	21	SD_D1	I/O	SDIO interface data pin 1
49	20	SD_D2	I/O	SDIO interface data pin 2
48	19	SD_D3	I/O	SDIO interface data pin 3
52	23	SD_SCK	O	SDIO interface clock pin
55	25	SD_CMD	O	SDIO interface command pin;
1	1	MDITP	ETH	Differential transmitter for 10BASE-T/100BASE-TX in MDI mode; Differential receiver for 10BASE-T/100BASE-TX in MDIX mode
2	2	MDITN	ETH	
4	4	MDIRP	ETH	Differential receiver for 10BASE-T/100BASE-TX in MDI mode; Differential transmitter for 10BASE-T/100BASE-TX in MDIX mode
5	5	MDIRN	ETH	
31	26	LED_ACT	O	ETH port status LED 0
-	26	SCL	O	SCL: Output for EEPROM clock signal line during reset
35	27	LED_LINK	O	ETH port status LED 1
-	27	SDA	I/O	SDA: Bidirectional data signal line for EEPROM during reset

46	-	CFG2/ SUSP	5I/O	CFG2: Chip function configuration pin 2 SUSP: SUSPEND sleep state output pin, high level indicates sleep state, low level indicates normal state
35	23	CFG1	I	Chip function configuration pin 1
31	25	CFG0	5I	Chip function configuration pin 0
55	-	PSELF	I	PSELF: CH339W acts as a power mode configuration pin during reset, suspended or high for self-powered mode, low for bus-powered mode, with built-in pull-up resistor.
68	-	TDI	O	Data output of JTAG interface
67	-	TDO	I	Data input of JTAG interface, built-in pull-up resistor
65	-	TCK	O	Clock output of JTAG interface
66	-	TMS	O	Mode selection of JTAG Interface
64	-	TRST	O	Reset output of JTAG interface
62	-	SRST	O	System reset output of JTAG interface
43	-	SCS	O	Chip selection output of 4-wire serial port
42	-	SCK	O	Clock output of 4-wire serial port, alias DCK
45	-	MISO	I	Data input of 4-wire serial port, alias SDI/DIN, built-in pull-up resistor
44	-	MOSI	O	Data output of 4-wire serial port, alias SDO/DOUT
33	-	TXD	O	Serial data output of UART, idle state is high level
32	-	RXD	5I	Serial data input of UART, built-in pull-up resistor
39	-	RTS	O	UART MODEM output signal, request transmission, low efficiency
38	-	CTS	I	UART MODEM input signal, clear transmission, low efficiency
39	-	SCL/ SMBCLK	O	SCL: Clock output of 2-wire serial interface SMBCLK: SMBus bus clock signal line
38	-	SDA/ SMBDAT	I/O	SDA: Data input and output of 2-wire serial interface SMBDAT: SMBus bus data signal line
56	-	CC1	5I/O	PD protocol communication pin CC1, used to connect adapter
57	-	CC2	5I/O	PD protocol communication pin CC2, used to connect adapter
47	-	CC3	I/O	PD protocol communication pin CC3, used to connect mobile phone / computer
59	-	PD_CTL1	O	PD protocol communication control pin 1
37	-	PD_CTL2	O	PD protocol communication control pin 2
36	-	PD_CTL3	I/O	PD protocol communication control pin 3 When the upstream switching function is enabled, the pin is a switching control pin, suspended or pulled up does not switch, input low-level control switching

Note 1: Pin type abbreviations:

USB = USB signal input;

ETH = Ethernet signal input;

I = 3.3V signal input;

O = 3.3V signal output;

5I = Rated 3.3V signal input, support 5V tolerant voltage;

P = Power or ground.

5. Function Description

5.1 Overcurrent Detection and Power Control

5.1.1 Overcurrent Detection

CH339W supports two overcurrent protection modes: Independent overcurrent mode and global overcurrent mode, while CH339F supports global overcurrent mode, as shown in Table 5-1.

Table 5-1 Description of overcurrent protection control

Chip model	Overcurrent configuration	Overcurrent mode	Sampling pin of overcurrent detection	Reference diagram
CH339W	EEPROM non-default configuration / CFG2-0 pin configuration	Independent overcurrent	OVCUR1#, OVCUR2#, OVCUR3#, OVCUR4#, OVCUR5#, OVCUR6#, OVCUR7#	Figure 5-1
	EEPROM default configuration / CFG2-0 pin configuration	Overall overcurrent	OVCUR1#	Figure 5-2
CH339F	-	Overall overcurrent	OVCUR#	Figure 5-2

5.1.2 Power Control

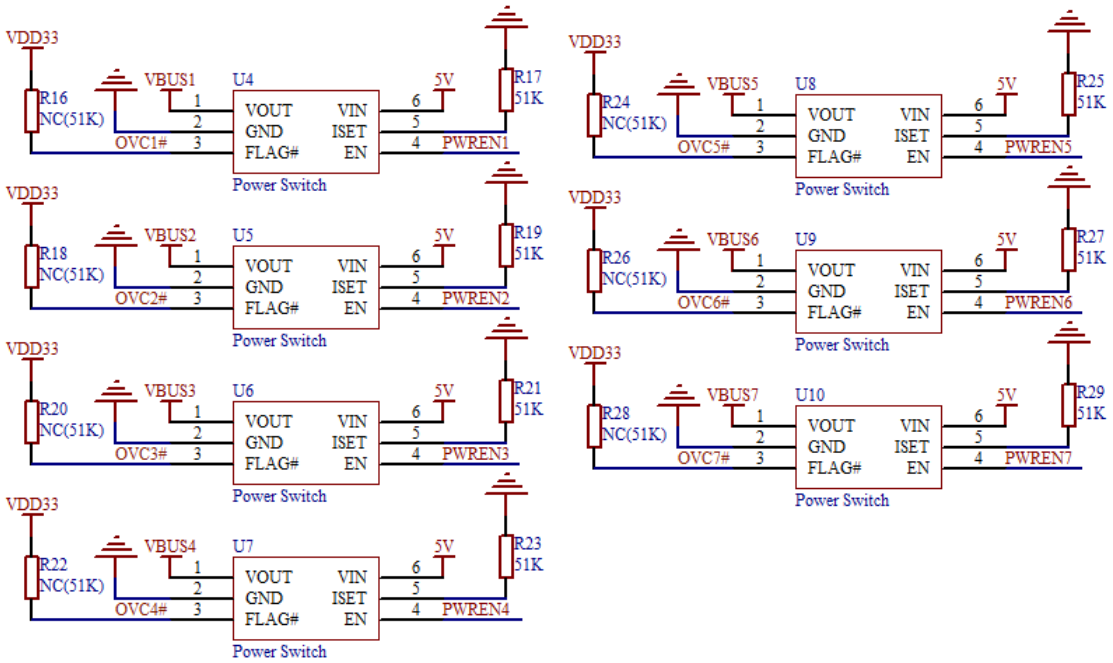
CH339W supports two power control modes: Independent power control mode and overall power control mode, while CH339F supports overall power control mode, as shown in Table 5-2.

Table 5-2 Description of power control

Chip model	Power control configuration	Power control	Control pin of overcurrent power supply	Reference diagram
CH339W	EEPROM non-default configuration / CFG2-0 pin configuration	Independent control	PWREN1#, PWREN2#, PWREN3#, PWREN4#, PWREN5#, PWREN6#, PWREN7# *Note: High level on*	Figure 5-1
	EEPROM default configuration / CFG2-0 pin configuration	Overall control	PWREN1#	Figure 5-2
CH339F	-	Overall control	PWREN#	Figure 5-2

5.1.3 Independent Overcurrent Detection and Independent Power Control

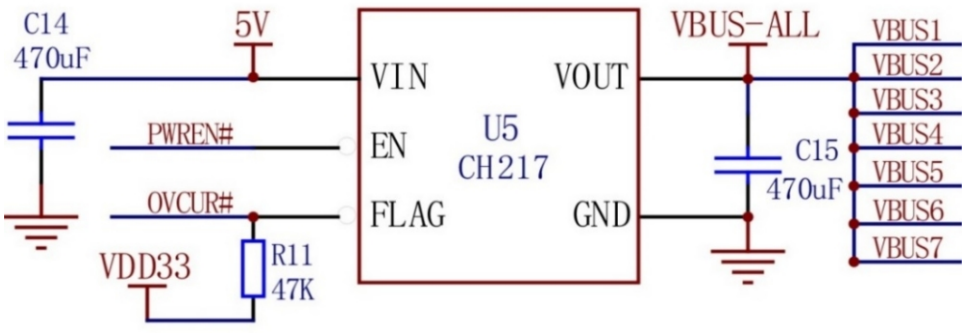
Figure 5-1 CH339W independent overcurrent detection and independent power control



In the above figure, V_{BUS1}-V_{BUS7} are connected to the V_{BUS} power supply pins of downstream ports 1-7 respectively. U4~U10 are USB current-limiting power distribution switching chips with internal integrated over-current detection for V_{BUS} power distribution management. In 5V applications without external power supply, it is recommended to set the current limit below 1A or even 500mA by ISET external resistor. The FLAG pin of U4~U10 is open-drain output, which needs to be pulled up by resistor respectively. The OVCUR# pin of CH339W chip provides built-in weak pull-up current, so resistors R16, R18, R20, R22, R24 can be omitted, R26 and R28. The output of the PWRENx# pin of the CH339 chip is low when the power supply is turned on, so if the control pin of the power switch chip used is active high, the polarity of the PWREN pin needs to be configured.

5.1.4 Overall Overcurrent Detection and Overall Power Control

Figure 5-2 overall overcurrent detection and independent power control



U5 is a USB current limiting power switch chip, such as a CH217 chip or a chip with similar functions. R11 can be omitted by default configuration. The capacity of C14 can be selected as needed. The $V_{BUS-ALL}$ also connects the V_{BUS} power pins of downstream ports 1-7. The current limit setting value of U5 needs to consider 7 downstream ports and whether it is self-powered or not.

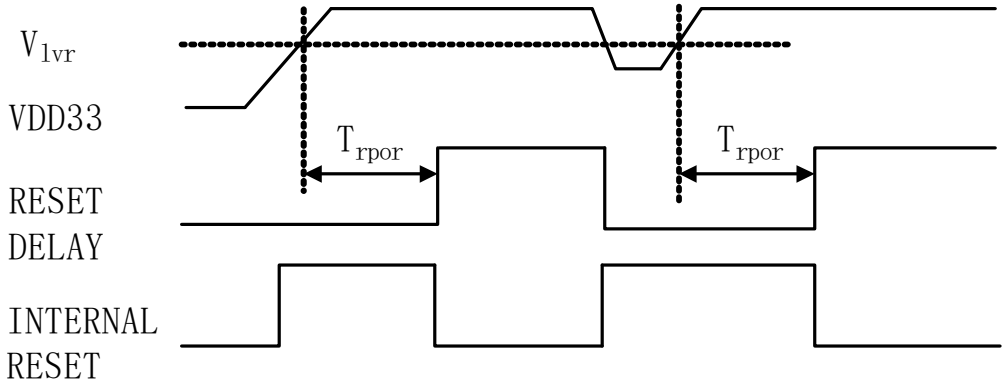
5.2 Reset

The chip is embedded with a power-on reset module, and in general, there is no need to provide an external reset signal. It also provides an external reset input pin RESET#, which has a built-in pull-up resistor.

5.2.1 Power-on Reset

When the power supply is powered on, the POR power-on reset module in the chip will produce a power-on reset sequence and delay the Trpor about 25mS to wait for the power supply to stabilize. In the process of operation, when the power supply voltage is lower than Vlvr, the LVR low voltage reset module in the chip will produce a low voltage reset until the voltage picks up, and delay to wait for the power supply to stabilize. The following figure shows the power-on reset process and the low-voltage reset process.

Figure 5-3 Reset during Power-on



5.2.2 External Reset

The external reset input pin RESET# has a built-in 40kΩ pull-up resistor. If the chip needs to be reset externally, the pin can be driven to a low level, the drive internal resistance is recommended to be no more than 1kΩ, and the reset low level pulse width needs to be greater than 4uS.

5.3 I/O Function Configuration

Some of the functions of the CH339 chip can be configured in 3 ways: internal EEPROM, external EEPROM and configuration pins. The parameter configuration function of external EEPROM has higher priority than the parameter configuration function of internal EEPROM, and the parameter configuration function of internal EEPROM has higher priority than the pin configuration function. Configuration pins are generally multiplexed pins that act as configuration pins during reset and then switch to the corresponding function pins after reset is complete. The CH339W chip has built-in 7-port HUB function, USB NIC function, USB card reader function, PD function, USB to JTAG function, USB to SPI function, USB to UART function, USB to GPIO function and USB to I2C function, supporting overall / independent overcurrent detection and overall / independent power control. Except for the main functions such as 7-port HUB, USB extended Ethernet, USB card reader and PD, other functions can be selected through configuration pins as needed, as shown in the table below.

Table 5-3 CH339W main configuration pin description

Configuration pin			Function enable / Disable description									
PIN46	PIN35	PIN31	Overall overcurrent detection	Independent overcurrent detection	Overall power control	Independent power	USB to JTAG	USB to SPI	USB to UART	USB to I2C/ SMBUS	Upstream port exchange function	Extension isolation function
CFG2	CFG1	CFG0										
0	0	0	Reserved									
0	0	1	√	×	√	×	√	√	√	√	√	×
0	1	0	√	×	√	×	√	√	√	√	×	√
0	1	1	×	√	×	√	×	×	×	√	×	×
1	0	0	×	√	√	×	√	×	×	√	×	×
1	0	1	√	×	×	√	×	√	√	√	×	×
1	1	0	√	×	√	×	√	√	(√)	×	×	×
1	1	1	√	×	√	×	√	√	√	√	×	×

Note 2: √ indicates that the function is enabled, × indicates that the function is disabled, and (√) indicates that the USB-to-serial port function supports hardware flow control.

Note 3: When the upstream switching function is enabled, the PD_CTL3 pin is used as the switching control pin, the suspension or pull-up does not switch, and the input low-level control switch.

The CH339F chip has built-in 4-port HUB function, USB card reader function and USB 100Gb NIC function, which supports overall overcurrent detection and overall power control. The USB card reader function, USB extended Ethernet function and upstream switching function can be configured through configuration pins.

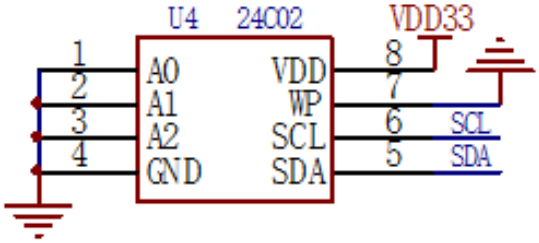
Table 5-4 CH339F configuration pin description

Configuration pin		Function enable / Disable description		
PIN42	PIN41	USB card reader function	USB to Ethernet function	Extension / isolation function
CFG1	CFG0			
0	0	×	√	√
0	1	×	√	×
1	0	√	×	×
1	1	√	√	×

5.4 EEPROM Configuration Interface

CH339F provides 2-wire I2C interface to communicate with the external EEPROM memory chip. The address of the EEPROM chip is 0. The EEPROM chip stores information such as custom vendor ID, product ID, number of downstream ports, device unremovable characteristics of downstream ports, USB string descriptors and function configuration.

Figure 5-4 Schematic diagram of external EEPROM connection



CH339 built-in information memory, according to the special needs of the industry can replace the external EEPROM lot customization of vendor or product information and configuration, such as setting the number of downstream ports, setting downstream ports of the device cannot be removed features.

5.5 EEPROM Configuration

CH339 supports loading configuration information such as vendor identification number VID, product identification number PID, USB string descriptor and feature configuration from external or internal EEPROM. If the information in EEPROM is invalid, the default configuration information is automatically loaded. Table 5-5 describes the specific configuration information of EEPROM.

Table 5-5 Internal / external EEPROM configuration information

Offset address	Parameter abbreviation	Parameter description	Default value
00h	VID_L	The low byte of the vendor identification code VID	86h
01h	VID_H	The high byte of the vendor identification code VID	1Ah
02h	PID_L	The low byte of the product identification number PID. Default is 9Fh.	9Fh
03h	PID_H	High byte of product identification number PID	80h

04h	bcdDevice_L	BcdDevice low byte, used to indicate the chip package model Fixed, unmodifiable	Follow model
05h	bcdDevice_H	BcdDevice high byte, used to indicate the chip version Fixed, unmodifiable	Follow model
06h	Fun_Cfg1	Functional configuration byte 1 Bit7: Power supply mode selection 0: Bus power mode (default); 1: Self-power mode Bit6: Reserved; Bit5: High-speed mode forbidden control 0: High-speed mode enabled (default); 1: High-speed mode disabled. Bit4: STT and MTT mode selection; 0: STT mode; 1: MTT mode (default); Bit3: Reserved; Bit2-1: Port overcurrent function control; 00: Overall overcurrent control; 01: Independent overcurrent control; 1x: Overcurrent control is not supported Bit0: Port power control; 0: Overall power control; 1: Independent power control.	Follow model
07h	Fun_Cfg2	Functional configuration byte 2 Bit7: Reserved; Bit6: Reserved; Bit5: Reserved; Bit4: Reserved; Bit3: HUB is Compound Device or not; 0: No; 1: Yes; Bit2-0: Reserved.	20h
08h	Fun_Cfg3	Functional configuration byte 3 Bit7-4: Reserved; Bit3: Port remapping function control 0: Disable (default); 1: Enable Bit2-1: Reserved; Bit0: String descriptor enables control; 0: Disable (default); 1: Enable	00h
09h	Dev_ Removable	Whether the downstream port device can remove the control	Follow model

		Bit7-1: Whether the device of downstream port 7-1 can be removed 0: Removable (default); 1: Not removable; Bit0: Reserved, must be 0;	
0Ah	Port_Dis_Sp	Port disabled in self-powered mode Bit7-1: Whether downstream port 7-1 is disabled or not 0: Enable (default); 1: Disable; Bit0: Reserved, must be 0;	00h
0Bh	Port_Dis_Bp	Port disabled in Bus Power Mode Bit7-1: Whether downstream port 7-1 is disabled or not 0: Enable (default); 1: Disable; Bit0: Reserved, must be 0;	00h
0Ch	MaxPwr_Sp	Maximum working current in self-powered mode, in 2mA	01h
0Dh	MaxPwr_Bp	Maximum working current in bus power supply mode, in 2mA	64h
0Eh	HubCurrent_Sp	Maximum current required by HUB in self-powered mode	01h
0Fh	HubCurrent_Bp	Maximum current required by HUB in bus power supply mode	64h
10h	Pwr_OnTime	Effective delay time from power to power on the downstream port	32h
11h	LanguageID_H	Language ID high byte	00h
12h	LanguageID_L	Language ID low byte	00h
13h	Vendor_StrLen	Vendor string descriptor length	00h
14h	Product_StrLen	Product string descriptor length	00h
15h	SN_StrLen	Serial number string descriptor length	00h
16h-53h	Vendor String	Vendor string descriptor Vendor's string descriptor in Unicode format	00h
54h-91h	Product String	Product string descriptor Product string descriptor in Unicode format	00h
92h-CFh	Serial Number String	Serial number string descriptor Serial number string descriptor in Unicode format	00h
D0h	PortNum	Number of downstream ports. Valid range: 1-7	Follow model
D1h	bcdUSB_L	USB version low byte bcdUSB_L=0x00, USB2.00 bcdUSB_L=0x01, USB2.01 bcdUSB_L=0x10, USB2.10	00h
D2h	Fun_Cfg4	Functional configuration byte 4 Bit7-2: Reserved, must write 0 Bit1: Force downstream port to full speed mode;	00h

		0: High-speed mode (default); 1: Full-speed mode; Bit0: Indicator function enable configuration; 0: Disable (default); 1: Enable.	
D3h	Fun_Cfg5	Functional configuration byte 5 Bit7: LED indicator polarity configuration; 0: Active low (default); 1: High level valid; Bit6: Port overcurrent detection polarity configuration; 0: Low level valid (default); 1: High level valid; Bit5: Port power control polarity configuration; 0: Active low (default); 1: High level valid; Bit4-0: Reserved.	00h
D4-FAh	Reserved	Reserved	00h
FBh	Port_Remap12	Downstream port 1-2 remapping configuration Bit7-4: Physical port 2 remapping 0000: Physical port 2 is prohibited from remapping; 0001: Physical port 2 mapped as logical port 1; 0010: Physical port 2 mapped as logical port 2; 0011: Physical port 2 mapped as logical port 3; 0100: Physical port 2 mapped as logical port 4; 0101: Physical port 2 mapped as logical port 5; 0110: Physical port 2 mapped as logical port 6; 0111: Physical port 2 mapped as logical port 7; 1000-1111: Invalid; Bit3-0: Physical port 1 remapping 0000: Physical port 1 is prohibited from remapping; 0001: Physical port 1 mapped as logical port 1; 0010: Physical port 1 mapped as logical port 2; 0011: Physical port 1 mapped as logical port 3; 0100: Physical port 1 mapped as logical port 4; 0101: Physical port 1 mapped as logical port 5; 0110: Physical port 1 mapped as logical port 6; 0111: Physical port 1 mapped as logical port 7; 1000-1111: Invalid.	00h
FCh	Port_Remap34	Downstream port 3-4 remapping configuration Bit7-4: Physical port 4 remapping 0000: Physical port 4 is prohibited from remapping;	00h

		0001: Physical port 4 mapped as logical port 1; 0010: Physical port 4 mapped as logical port 2; 0011: Physical port 4 mapped as logical port 3; 0100: Physical port 4 mapped as logical port 4; 0101: Physical port 4 mapped as logical port 5; 0110: Physical port 4 mapped as logical port 6; 0111: Physical port 4 mapped as logical port 7; 1000-1111: Invalid. Bit3-0: Physical port 3 remapping 0000: Physical port 3 is prohibited from remapping; 0001: Physical port 3 mapped as logical port 1; 0010: Physical port 3 mapped as logical port 2; 0011: Physical port 3 mapped as logical port 3; 0100: Physical port 3 mapped as logical port 4; 0101: Physical port 3 mapped as logical port 5; 0110: Physical port 3 mapped as logical port 6; 0111: Physical port 3 mapped as logical port 7; 1000-1111: Invalid.	
FDh	Port_Remap56	Downstream port 5-6 remapping configuration Bit7-4: Physical port 6 remapping 0000: Physical port 6 is prohibited from remapping; 0001: Physical port 6 mapped as logical port 1; 0010: Physical port 6 mapped as logical port 2; 0011: Physical port 6 mapped as logical port 3; 0100: Physical port 6 mapped as logical port 4; 0101: Physical port 6 mapped as logical port 5; 0110: Physical port 6 mapped as logical port 6; 0111: Physical port 6 mapped as logical port 7; 1000-1111: Invalid. Bit3-0: Physical port 5 remapping 0000: Physical port 5 is prohibited from remapping; 0001: Physical port 5 mapped as logical port 1; 0010: Physical port 5 mapped as logical port 2; 0011: Physical port 5 mapped as logical port 3; 0100: Physical port 5 mapped as logical port 4; 0101: Physical port 5 mapped as logical port 5; 0110: Physical port 5 mapped as logical port 6; 0111: Physical port 5 mapped as logical port 7; 1000-1111: Invalid.	00h
FEh	Port_Remap7	Downstream port 7 remapping configuration Bit7-4: Physical port 7 remapping	00h

		0000: Physical port 7 is prohibited from remapping; 0001: Physical port 7 mapped as logical port 1; 0010: Physical port 7 mapped as logical port 2; 0011: Physical port 7 mapped as logical port 3; 0100: Physical port 7 mapped as logical port 4; 0101: Physical port 7 mapped as logical port 5; 0110: Physical port 7 mapped as logical port 6; 0111: Physical port 7 mapped as logical port 7; 1000-1111: Invalid. Bit3-0: Reserved.	
FFh	Reserved	Reserved	00h

5.6 Bus Power Supply and Self-power Supply

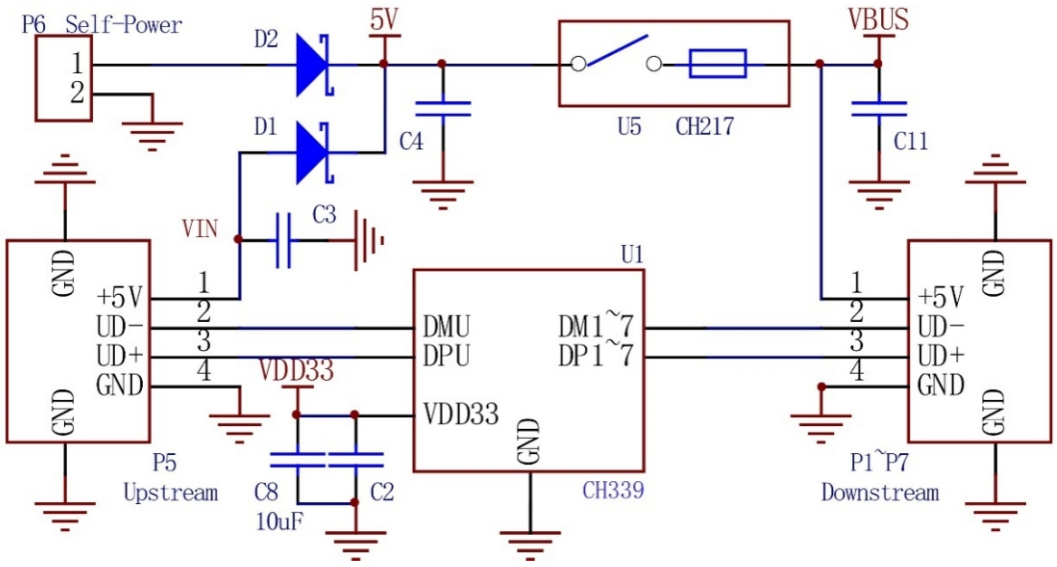
CH339 supports USB bus power mode and self-power mode. The bus power supply comes from the upstream port of USB, and the power supply capacity is 500mA or 900mA, 1.5A and other standards. The internal resistance loss of USB wire and the consumption of HUB itself will reduce the power supply capacity of the downstream port, and the voltage of the downstream port may be on the low side. Self-power supply usually comes from an external power port, depending on the power supply capacity of the external power supply.

Because the voltages of self-power supply and bus power supply are difficult to be completely equal, HUB needs to avoid the large current caused by the direct short connection between them. In addition, when the USB upstream port is powered off, the HUB should also avoid recharging current to the USB bus and USB host from the self-powered external power supply.

5.6.1 Bidirectional Isolation Schematic

The diodes D1 and D2 are used to bidirectionally isolate the V_{BUS} bus power supply and the P6 port external power supply, preventing the two power supplies from pouring back into each other, using high-power Schottky barrier diodes to reduce their own voltage drop, and the downstream port V_{BUS} gets 4.7V voltage or even lower, just as a sign.

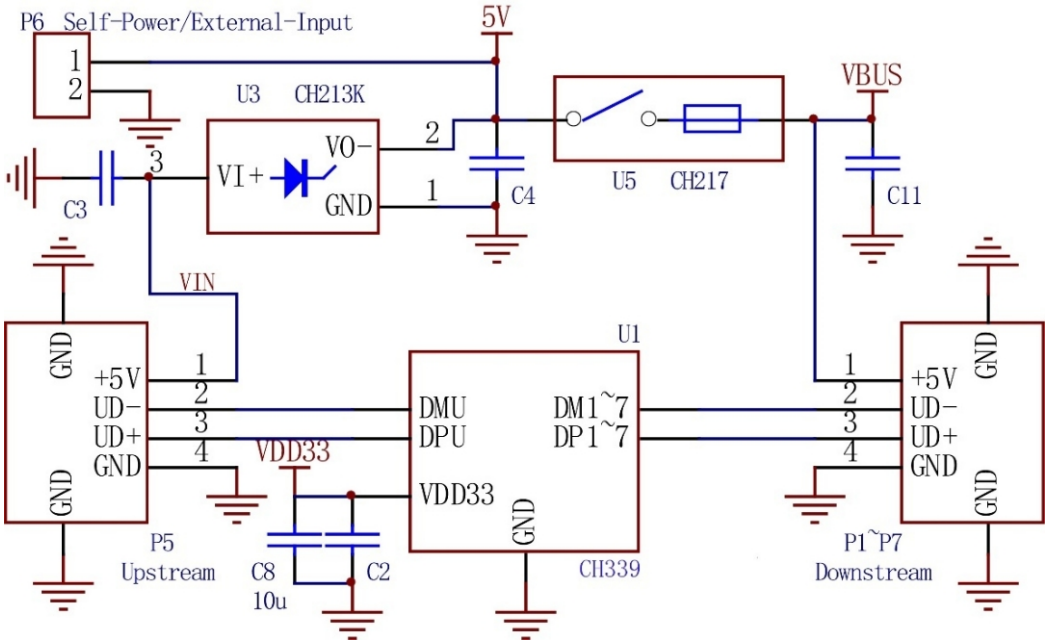
Figure 5-5 Schematic diagram of Schottky barrier diode bidirectional isolation V_{BUS} and external power supply



5.6.2 Practical Single Isolation Scheme

The function of the ideal diode is the one-way conduction of the low voltage drop. The U3 is used to prevent the upstream port V_{BUS} of the P6 port from pouring back. at the 500mA current, the voltage drop of the U3 is about 1/3 of the Schottky barrier diode voltage drop, and the downstream port V_{BUS} can get 4.9V voltage.

Figure 5-6 Schematic diagram of ideal diode isolating V_{BUS} and external power supply



5.7 USB to Ethernet Function

The CH339 chip integrates USB to 100Gb Ethernet function, integrated 10M/100M Fast Ethernet MAC controller and 100Gb transceiver PHY, which is compatible with IEEE 802.3 10Base-T, 100Base-TX protocol standards. Supports auto-negotiation and Auto-MDIX, providing the necessary features required for transmission over CAT5 network cables and CAT6 network cables. Built-in 50Ω impedance matching resistor with streamlined peripheral circuitry.

ETH related feature pins are as follows:

Table 5-6 Description of Ethernet function pins

Pin name	Type	Function description
MDITP	ETH	Differential transmitter for 10BASE-T/100BASE-TX in MDI mode
MDITN	ETH	Differential receiver for 10BASE-T/100BASE-TX in MDIX mode
MDIRP	ETH	Differential receiver for 10BASE-T/100BASE-TX in MDI mode
MDIRN	ETH	Differential transmitter for 10BASE-T/100BASE-TX in MDIX mode
LED_ACT	O	ETH port status LED 0
LED_LINK	O	ETH port status LED 1

The Ethernet controller supports IPv4/IPv6 packet check, IPv4TCP/UDP/HEAD and IPv6TCP/UDP packet check generation and inspection. Support IEEE802.3x-compliant flow control and half-duplex collision pressure fallback flow control. VLAN tags that conform to the IEEE802.3Q standard are supported. Support Magic packet Wake up, optional low power consumption in hibernation mode, automatic power management, can save power consumption in no-load or light load, and support 10Base-T energy saving mode.

The chip supports CDC-ECM mode by default, and custom firmware can support vendor drivers and CDC-NCM. The firmware will select and enable the corresponding mode according to the configuration requirements of the user and the commands issued by the host computer of PC. Support to configure relevant parameters through built-in EEPROM, including MAC address, MAC filter configuration, USB vendor ID, product ID, USB power configuration and vendor custom string and other information.

5.8 USB to High-speed Card Reader Function

The CH339 chip integrates the function of USB to high-speed card reader and supports SD card and MMC card. Realize the conversion of storage media such as SD card or MMC card into standard USB mass storage devices. The related feature pins are as follows:

Table 5-7 Description of the card reader function pins

Pin name	Type	Function description
SD_D0	I/O	SDIO interface data pin 0
SD_D1	I/O	SDIO interface data pin 1
SD_D2	I/O	SDIO interface data pin 2
SD_D3	I/O	SDIO interface data pin 3
SD_SCK	O	SDIO interface clock pin
SD_CMD	O	SDIO interface command pin

5.9 USB to Common Interface Function

CH339W chip integrates interface functions such as USB to SPI/JTAG/UART/I2C. The enabling or disabling of each interface function can be configured through the configuration pin CFG2-0 as needed.

5.9.1 USB to SPI Interface

The 4-wire SPI synchronous serial interface works in Host/Master host mode, including SCSx, SCK (CLK), MISO (SDI/DIN) and MOSI (SDO/DOUT) four signal lines. Support for 8-bit data structures, support for MSB and LSB transmission, support for the SPI mode 0/1/2/3, support for transmission frequency configuration, etc. Built-in hardware DMA, which can send and read batch data quickly. Through the cooperation of computer API, 4-wire interface FLASH, MCU, sensors and other devices can be operated flexibly.

5.9.2 USB to JTAG Interface

The JTAG interface works in Host/Master host mode, including six signal lines: TMS, TCK, TDI, TDO, TRST and SRST. TRST and SRST are optional signal lines. Support the fast mode and bit-bang mode of custom protocol, and the transmission rate can reach 30Mbit/S. Provide computer-side USB high-speed driver and USB to JTAG TAP function library, support secondary development, for the construction of custom USB to high-speed JTAG debugger, FPGA downloader, CPU programmer and other products.

5.9.3 USB to UART Interface

The UART interface works in full duplex mode, including four signal lines: TXD, RXD, CTS and RTS. When the serial input is idle, the RXD is high, and when the serial output is idle, the TXD is high.

Serial data includes 1 low level start bit, 8 data bits, 1 / 2 high level stop bits, supports no parity / odd parity / even parity. Support common communication baud rate: 2400, 3600, 4800, 9600, 14400, 19200, 28800, 33600, 38400, 56000, 57600, 76800, 115200, 128000, 153600, 230400, 460800, 921600, 1M, 1.5M, 2M 3M, 4M, 5M, 6M and so on.

The asynchronous serial port of CH339W chip supports CTS and RTS hardware automatic flow control, which is not enabled by default and can be enabled by VCP (Virtual COM Port) vendor driver control. If enabled, the serial port will continue to send the next packet of data only when the CTS pin input is detected as valid (active low), otherwise the serial port will pause sending; when the receive buffer is empty, the serial port will automatically validate the RTS pin (active low) until the receive buffer is fuller of data, then the serial port will automatically invalidate the RTS pin, and validate the RTS pin again when the buffer is empty. Using hardware automatic rate control, you can connect your side's CTS pin to the other side's RTS pin, and connect your side's RTS pin to the other side's CTS pin.

Under the Windows operating system on the computer side, after installing the high-speed VCP vendor driver, it is able to emulate a standard serial port, so the vast majority of serial port applications are fully compatible and usually do not require any modification. USB to UART interface function can be used to upgrade the original serial peripheral devices or to add additional serial ports to the computer via the USB bus. Through the addition of level shifters, further interfaces such as RS232, RS485, RS422, etc. can be provided.

5.9.4 USB to I2C / SMBus Interface

The I2C/SMBus interface operates in Host/Master host mode and consists of two signal lines, SCL and SDA. SCL is used for unidirectional output of the synchronization clock with open-drain output, and SDA is used for bi-directional data input and output with open-drain output and input.

The basic operating elements of the I2C interface include: Start bit, stop bit, bit output, and bit input. the I2C interface supports five transmission speeds, and can be used to flexibly operate 2-wire interface devices such as A/D, D/A, EEPROM, and sensors through the cooperation of a computer API.

6. Parameters

6.1 Absolute Maximum Value (Critical or exceeding the absolute maximum value will probably cause the chip to work improperly or even be damaged)

Name	Parameter Description	Min.	Max.	Unit
T_A	Ambient temperature during operation	-40	85	℃
T_J	Junction temperature range	-40	100	℃
T_S	Ambient temperature during storage	-55	150	℃
V_{DD33}	Working power supply voltage (V_{DD33} pin connected to power, GND pin grounded)	-0.4	4.0	V
V_{IO33}	Pin power supply voltage (V_{IO33} pin connected to power, GND pin grounded)	-0.4	4.0	V
V_{5I}	Voltage on 5V tolerant voltage input pin	-0.4	5.3	V
V_{USB}	Voltage on USB signal pin	-0.4	V_{DD33}+0.4	V
V_{GPIO}	Voltage on other (3.3V) input or output pins	-0.4	V_{IO33}+0.4	V
V_{ESDUSB}	HBM ESD tolerant voltage on USB signal pin	6K		V
V_{ESDIO}	HBM ESD on other pins tolerant voltage	2K		V

6.2 Electrical Parameters (Test conditions: T_A=25℃, V_{DD33}=3.3V)

Name	Parameter Description			Min.	Typ.	Max.	Unit
V_{DD33}	External 3.3V voltage@V_{DD33}			3.2	3.3	3.4	V
V_{IO33}	Pin power voltage				V_{DD33}		V
I_{CC}	Working current	Upstream high-speed	7 downstream high-speed + ETH + SDIO + USB transfer		200		mA
		Upstream high-speed	4 downstream high-speed +ETH+SDIO		156		mA
		Upstream high-speed	4 downstream high-speed +ETH		154		mA
		Upstream high-speed	4 downstream high-speed +SDIO		106		mA
		Upstream high-speed	7 downstream high-speed		140		mA
		Upstream high-speed	4 downstream high-speed		100		mA
		Upstream high-speed	1 downstream high-speed		65		mA
		Upstream high-speed	7 downstream full-speed		50		mA
		Upstream full-speed	7 downstream full-speed		34		mA

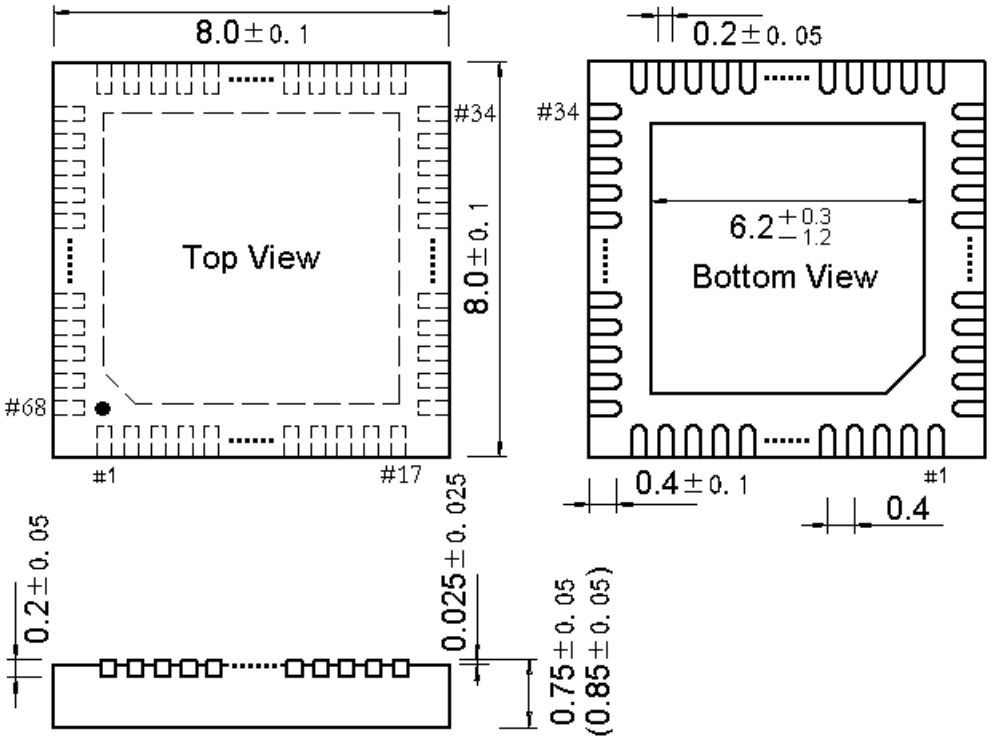
		Upstream high-speed Upstream full-speed	Downstream no device With 1.5KΩ pull-up		0.5		mA
I_{SLP}	Deep sleep power supply current (excluding 1.5K Ω pull-up) Or: Own sleep power supply current (without USB host)						mA
V_{IL}	Low level input voltage		Standard I/O pin	0		0.8	V
			5I pin	0		0.8	V
V_{IH}	High level input voltage		Standard I/O pin	2.0		V_{IO33}	V
			5I pin	2.0		5.0	V
V_{ILRST}	Low-level input voltage of RESET# pin			0		0.8	V
V_{OL}	Low level output voltage		Sink current 5mA		0.4	0.6	V
V_{OH}	High level output voltage		Source current 5mA	V_{IO33}-0.6	V_{IO33}-0.4		V
R_{PU}	Pull-up equivalent resistance			30	40	55	kΩ
R_{PD}	Pull-down equivalent resistance			30	40	55	kΩ
V_{lvr}	Voltage threshold for low voltage reset of power supply			2.4	2.9	3.2	V

7. Package

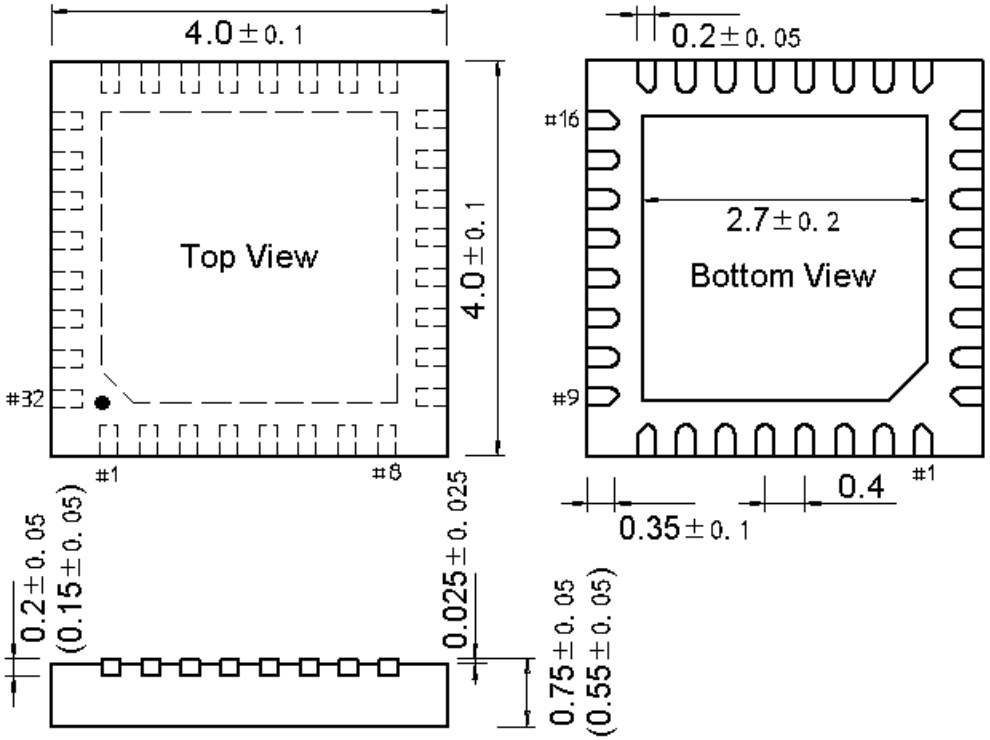
Note: All dimensions are in mm (millimeters).

The pin center spacing values are nominal values, with no error. Other than that, the dimensional error is not greater than the greater of ±0.2mm.

7.1 QFN68



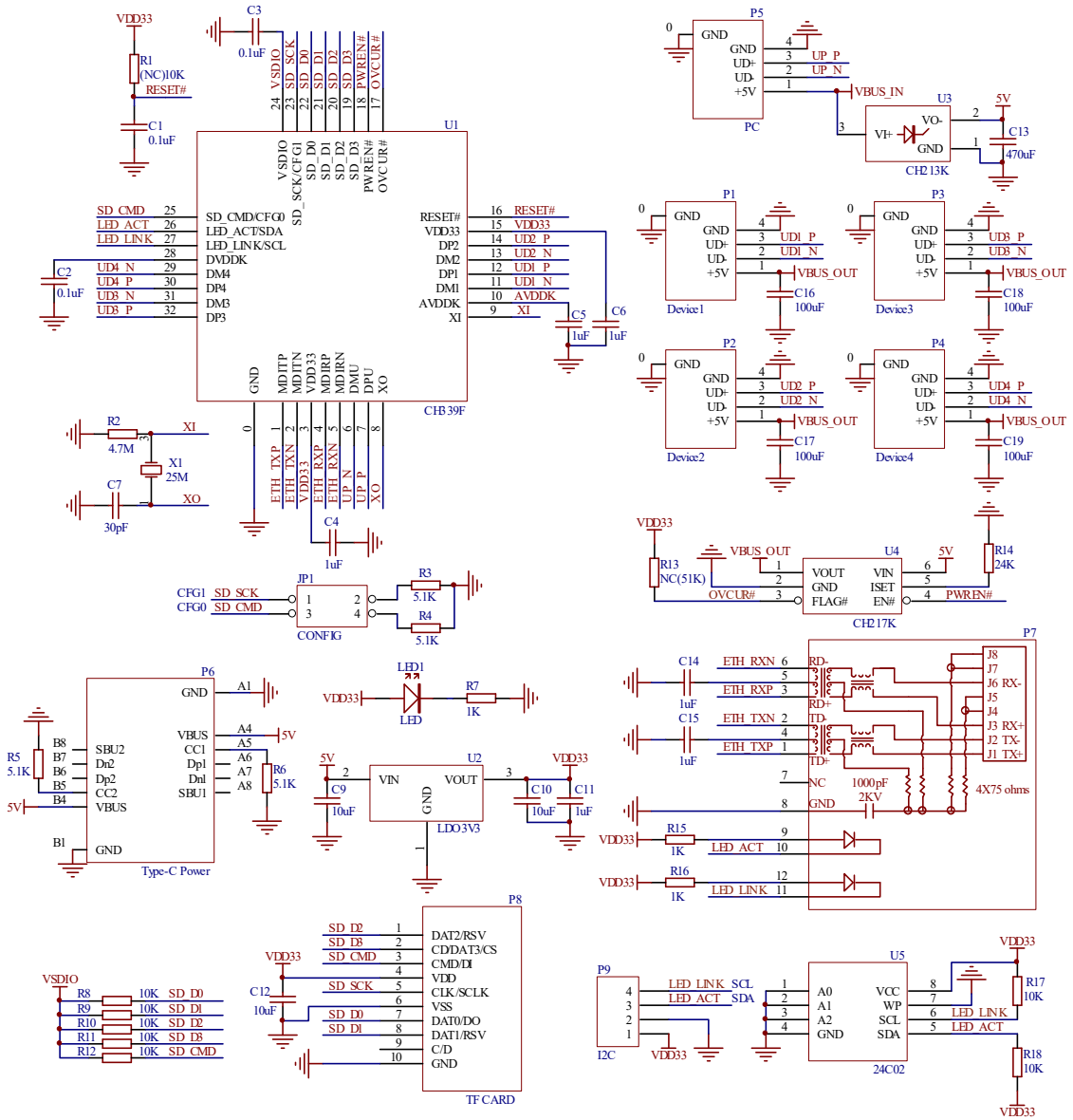
7.2 QFN32


4.0±0.1
Top View
4.0±0.1
#32
#1
#8
0.2±0.05
(0.15±0.05)
0.025±0.025
0.75±0.05
(0.55±0.05)
0.2±0.05
#16
2.7±0.2
Bottom View
#9
#1
0.4
0.35±0.1

8. Application

8.1 HUB + USB Card Reader + USB NIC

Figure 8-1 Reference circuit diagram for CH339F application



In the figure above, P1-P4 is the four downstream USB interfaces of HUB, P5 is the upstream USB interface of HUB, P6 is the external power supply interface, P7 is the RJ45 interface of built-in network transformer, and P8 is the SD card interface.

The U5 in the figure is an optional EEPROM, CH339 Ethernet LED pin that is also used to connect the EEPROM during a reset.

U2 is a 5V to 3.3V Low Dropout Regulator (LDO). Try to choose a wide range of input and low dropout models. It is recommended that the load capacity of the 500mA is not lower than that of the U2 and has a heat dissipation mechanism, so as to ensure a stable output at 3.3V. U3 is an ideal low-voltage drop diode CH213, with simple over-

current and short-circuit protection, and faster protection response, used to avoid V_{BUS_IN} backflow of the P6 external power supply upstream port P5, especially when the upstream port such as the computer is turned off and the external power supply of the P6 is still supplied. Theoretically, U3 can be replaced by Schottky barrier diode, but it is necessary to choose devices with low voltage drop, otherwise the output voltage of downstream port V_{BUS} will be reduced. When 300mA load current, the voltage drop of Schottky barrier diode is about 0.3V, and that of ideal diode is about 0.05V.

The power supply of all ports of HUB in current application is overall power control and overall overcurrent detection, U4 is USB current limit power switch chip CH217K which supports overcurrent protection, compared with the fuse resistor, the protection response is faster and more effective. Note that the fuse resistor and USB power switch chip may not support high temperature. R14 in the figure can set the current limit threshold according to the power supply capacity, the FLAG# pin of the USB current limit power switch chip can generate an over-current or over-temperature alarm signal to notify the HUB controller and the computer, and the OVCUR# pin of the CH339 chip has a built-in pull-up resistor.

At the moment when the USB device in the downstream port is hot-plugged, the dynamic load may instantly drop the V_{BUS} and 5V voltage, which may lead to the low-voltage reset LVR, resulting in the disconnection and reconnection of the whole HUB. Improvement methods: (1) Increase the electrolytic capacitor of the 5V power supply (Increase the capacity of the graphic C13) within the allowable range of the specification, alleviate the drop; (2) Increase the capacitance of the power input of the HUB chip (Increase the capacity of the graphic C10, such as 22uF); (3) Enhance the 5V power supply capacity or change to self-power supply, in addition, improving the quality of USB wire will also improve the power supply capacity.

The actual working current carrying capacity should be taken into account when designing PCB. The PCB of V_{BUS_IN}, 5V, V_{BUS_OUT}, P6 and each port GND routing path is as wide as possible. If there are holes, multiple parallel connections are recommended. The D+ and D- signal lines of the USB port are arranged in parallel according to the high-speed USB specification to ensure the characteristic impedance and provide ground wires or copper cladding on both sides as far as possible to reduce the signal interference from the outside.

5V overvoltage protection is recommended, and ESD protection is recommended for all USB signals, e.g. CH412K, whose VCC should be connected to 3.3V.

8.2 HUB + USB Card Reader+ USB NIC + USB to Multiple Interfaces

In the figure below, P1-P7 is the seven downstream USB interfaces of HUB, P8 is the upstream USB interface of HUB, P9 is the external power supply interface, P11 is the SD card interface, P12 is the RJ45 interface of built-in network transformer, P13 is the USB-to-I2C interface, P14 is the USB-to-JTAG interface, P15 is the USB-to-UART and SPI interface, and P16 is the extended interface controlled by PD.

Figure 8-2 Reference circuit diagram for CH339W application