CH32V004 Datasheet

V1.5

Overview

CH32V004 is a general-purpose microcontroller designed based on QingKe RISC-V core, supporting 48MHz system main frequency, with wide voltage, low-power consumption, 1-wire SDI and other features. Its pins and functions are compatible with CH32V003. CH32V004 has a built-in 12-bit ADC, with a sampling rate of up to 3Msps; it provides rich peripheral resources, such as 7-channel DMA controller, multi-group timer, USART, I2C, SPI and so on.

Features

- **Core**
  - QingKe 32-bit RISC-V core, RV32EmC instruction set
  - Fast programmable interrupt controller + hardware interrupt stack
  - Support 2-level interrupt nesting
  - Support system main frequency 48MHz
- **Memory**
  - 6KB volatile data storage area SRAM
  - 32KB program memory CodeFlash
  - 3328B BootLoader
  - 256B non-volatile system configuration memory
  - 256B user-defined memory
- **Power management and low-power consumption**
  - System power supply V_{DD}: 2.7~5V
  - Low-power mode: Sleep, Standby
- **Clock & Reset**
  - Built-in factory-trimmed 24MHz RC oscillator
  - Built-in 128KHz RC oscillator
  - High-speed external 3~25MHz oscillator
  - Built-in system clock monitoring (SCM) module
  - Power on/down reset, programmable voltage detector
- **7-channel general-purpose DMA controller**
  - 7 channels, support ring buffer
  - Support TIMx/ADC/USART/I2C/SPI
- **12-bit ADC**
  - Analog input range: V_{SS}~V_{DD}
  - 8 external signals + 3 internal signals
  - Support 3M sampling rate
- **Multiple timers**
  - 16-bit advanced-control timer, with dead zone control and emergency brake; can offer PWM complementary output for motor control
  - 16-bit general-purpose timer, provide input capture/output comparison/PWM/pulse counting/incremental encoder input
  - 2 watchdog timers (independent watchdog and window watchdog)
  - SysTick: 32-bit counter
- **1 set of USART**
  - Support LIN, support multiple pin mapping
- **I2C interface**
- **SPI interface**
- **GPIO port**
  - 3 sets of GPIO ports, 18 I/O ports
  - Mapping 1 external interrupt
- **Security features: Chip unique ID**
- **Debug mode: 1-wire serial debug interface (SDI)**
- **Package: QFN, TSSOP**

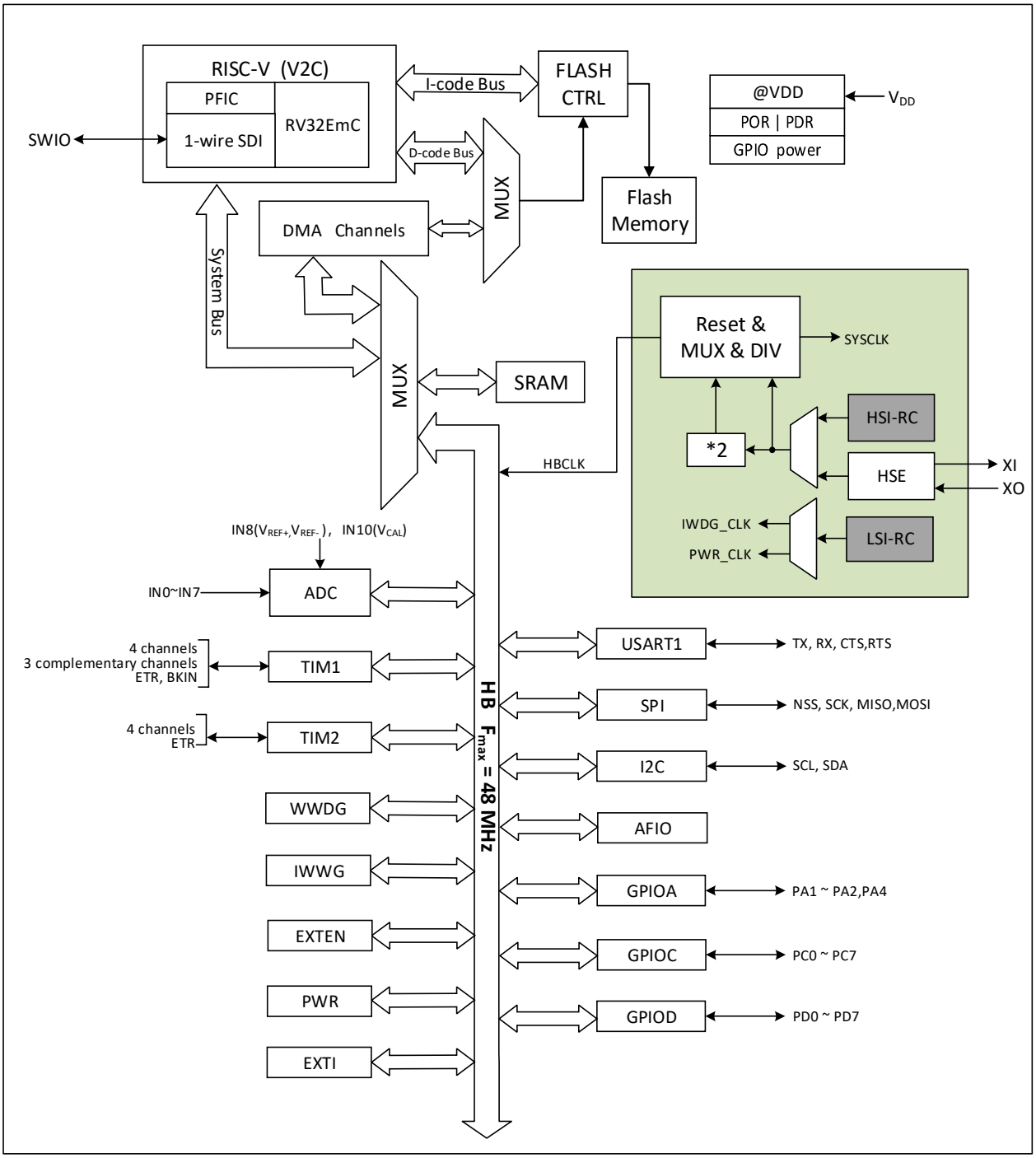
Model	Code FLASH	RAM	GPIO	ADTM	GPTM	Watchdog	ADC	Serial port	I2C	SPI	Package form
CH32V004F6P1	32K	6K	18	1	1	2	8+3	1	1	1	TSSOP20
CH32V004F6U1	32K	6K	18	1	1	2	8+3	1	1	1	QFN20

Chapter 1 Specification Information

1.1 System Structure

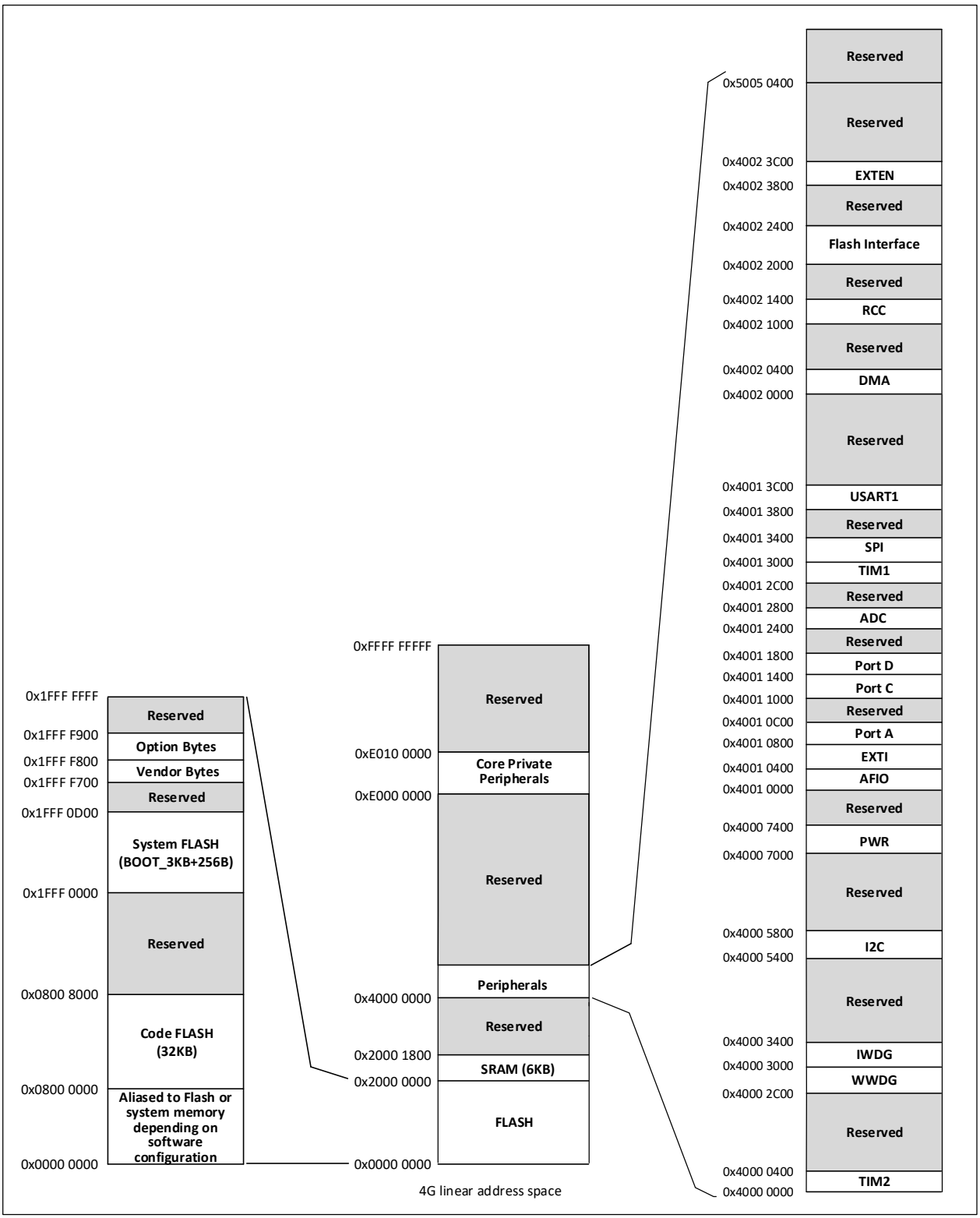
The microcontroller is based on the RISC-V instruction set design, its architecture will be QingKe microprocessor core, arbitration unit, DMA module, SRAM storage and other components through multiple buses to achieve interaction. The design integrates a general-purpose DMA controller to reduce the burden on the CPU, improve access efficiency. Multi-level clock management mechanism is applied to reduce the power consumption of peripherals, while both data protection mechanisms, automatic clock switching protection and other measures to increase system stability. The following diagram shows the overall architecture.

Figure 1-1 System block diagram



1.2 Memory Map

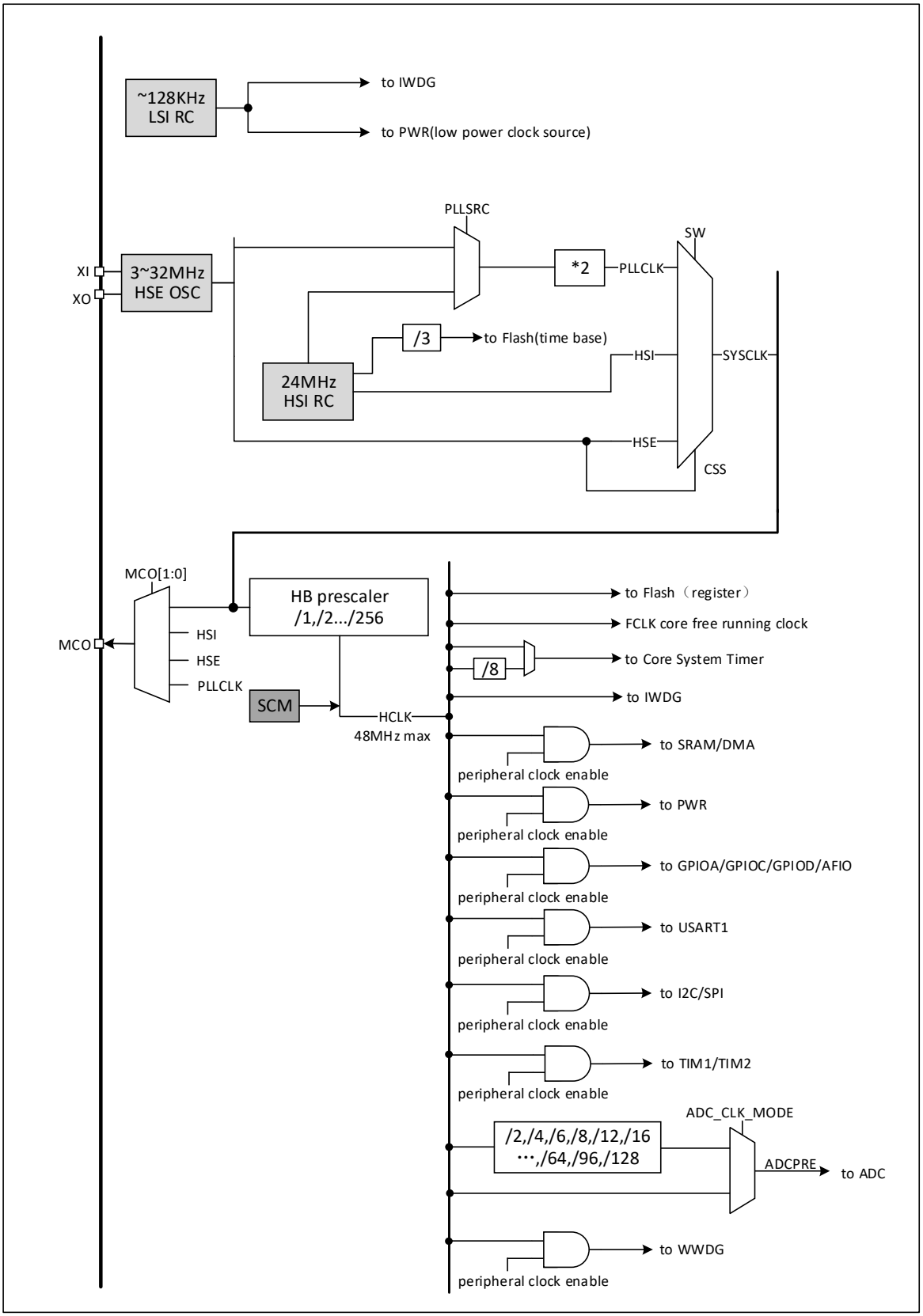
Figure 1-2 Memory address map



1.3 Clock Tree

3 sets of clock sources are introduced into the system: Internal high-frequency RC oscillator (HSI), internal low-frequency RC oscillator (LSI) and external high-frequency oscillator (HSE). Among them, the low-frequency clock source provides a clock reference for the IWDG, and the high-frequency clock source is directly or indirectly output as the system bus clock (SYSCLK) through a 2x multiplier, and the system clock is then provided by the pre-scaler for the HB domain peripheral control clock and sampling or interface output clock. Part of the module working need to be provided by PLL clock directly.

Figure 1-3 Clock tree block diagram



1.4 Functional Description

1.4.1 QingKe RISC-V2A Processor

RISC-V2C supports RISC-V instruction set EmC[(1)] subset. The processor is internally managed in a modular fashion and contains units such as a programmable fast interrupt controller (PFIC), extended instruction support, and so on. The bus is connected to external unit modules to enable interaction between external function modules and the core. QingKe processor with its minimalist instruction set, a variety of operating modes, modular customization and expansion features can be flexibly applied to different scenarios MCU design, such as small area low-power embedded scenarios.

- Support machine mode
- Fast Programmable Interrupt Controller (PFIC)
- 2-level hardware interrupt stack
- Support 1-wire /2-wire serial debug interface (SDI)
- Custom extension instructions

Note: 1. The "m" extension in EmC implements the multiplication subset of the M extension.

1.4.2 On-chip Memory

Built-in 6K-byte SRAM area, which is used to store data, which is lost after power loss.

Built-in 32K-byte program flash memory area (Code FLASH), that is, the user area, is used for users' applications and constant data storage.

Built-in 3328-byte system storage area (System FLASH), that is, BOOT area, is used for system boot program storage (factory-solidified bootloader).

Built-in 256-byte system non-volatile configuration information storage area, used for manufacturer configuration word storage, solidified before leaving the factory, users can not be modified.

Built-in 256-byte user-defined information store for user option byte storage.

1.4.3 Power Supply Scheme

V_{DD} = 2.7 ~ 5.5V: Supplies power to the I/O pins as well as the internal regulator.

1.4.4 Power Supply Monitor

The power-on reset (POR) / power-down reset (PDR) circuit is integrated inside the chip, which is always in the operating state to ensure that the system works when the power supply exceeds the set threshold ($V_{POR/PDR}$); when the V_{HV} is lower than the set threshold ($V_{POR/PDR}$), the device is placed in the reset state without the need to use an external reset circuit.

Refer to Chapter 3 for the values of $V_{POR/PDR}$.

1.4.5 System Voltage Regulator LDO

After resetting, the system voltage regulator is automatically switched on. There are two modes of operation depending on the application mode.

- On mode: Normal running operation, providing stable core power.
- Low-power mode: Low-power operation of the regulator when the CPU is in Standby mode.

1.4.6 Low-power Mode

The system supports two low-power modes, which can achieve the best balance under the conditions of low-power consumption, short start-up time and multiple wake-up events.

- Sleep mode (SLEEP)

In sleep mode, only the CPU clock stops, but all peripheral clocks are powered normally and the peripherals are in working state. This mode is the shallowest low-power mode, but can achieve the fastest wake-up.

Exit condition: Any interruption or wake-up event.

- Standby mode (STANDBY)

A peripheral clock control mechanism is combined with the SLEEPDEEP of the core and allows the voltage regulator to operate in a lower power state. The high-frequency clock (HSI/HSE/PLL) domain is turned off, SRAM and register contents are maintained, and I/O pin states are maintained. The system can continue to run after this mode wakes up, with HSI as the default system clock.

Exit conditions: Any external interrupt / event (EXTI signal), external reset signal on NRST, IWDG reset, in which EXTI signal includes one of 18 external I/O ports, PVD output, automatic wake-up, etc.

1.4.7 Programmable Fast Interrupt Controller (PFIC)

The chip has a built-in Programmable Fast Interrupt Controller (PFIC) that supports up to 255 interrupt vectors, providing flexible interrupt management with minimal interrupt latency. Currently the chip manages 4 core private interrupts and 25 peripheral interrupt management, with other interrupt sources reserved. the PFIC registers are all accessible in both user and machine privileged modes.

- 2 individually maskable interrupts
- Provide one non-maskable interrupt NMI
- Support Hardware Prologue/Epilogue (HPE) without instruction overhead
- Provide 2 Vector Table Free (VTF) for faster access to interrupt service routines
- Vector table support address or instruction mode
- Interrupt nesting depth can be configured up to 2 levels
- Support interrupt tail linking

1.4.8 External Interrupt/Event Controller (EXTI)

The external interrupt/event controller contains a total of 10 edge detectors for generating interrupt/event requests. Each interrupt line can be configured independently of its trigger event (rising or falling edge or double edge) and can be individually masked; a pending register maintains the status of all interrupt requests. EXTI can detect clock cycles with pulse widths less than the internal HB. Up to 18 general-purpose I/O ports are optionally connected to the same external interrupt line.

1.4.9 General-purpose DMA Controller

The system has built-in general-purpose DMA controller, manages 7 channels, flexibly handles high-speed data transmission from memory to memory, peripheral to memory and memory to peripheral devices, and supports ring buffer mode. Each channel has special hardware DMA request logic, which supports one or more peripheral access requests to memory. Access priority, transmission length, source address and destination address of transmission can be configured.

DMA for the main peripherals include: general / advanced timer TIMx, ADC, USART, I2C, SPI.

Note: DMA and CPU access the system SRAM after arbitration by the arbitrator.

1.4.10 Clock and Boot

The system clock source HSI is on by default. After no clock is configured or reset, the RC oscillator of the internal 24MHz is used as the default CPU clock, and then the external 3~25MHz clock or PLL clock can be selected. When clock safe mode is turned on, if HSE is used as the system clock (directly or indirectly), if an external clock failure

is detected, the system clock will automatically switch to the internal RC oscillator, while HSE and PLL will automatically turn off; for low-power mode with clock off, the system will also automatically switch to the internal RC oscillator after waking up. If the clock interrupt is enabled, the software can receive the corresponding interrupt. In addition, in order to improve the reliability of the system, System Clock Monitor (SCM) module is added. When the enable bit is turned on, if the system clock fails, a brake signal will be generated to the advanced timer TIM1, and the system clock failure interrupt flag will be set. If the enable is interrupted in advance, the interrupt will be entered.

1.4.11 Analog-to-digital Converter (ADC)

The chip has a built-in 12-bit ADC that provides up to 8 external channels and 3 internal channels for sampling at sampling rates up to 3Msps, providing programmable channel sampling time for single, continuous, scan or intermittent conversion. The analog watchdog function allows very accurate monitoring of one or more selected channels for monitoring the channel signal voltage, and when the voltage exceeds a set threshold, the system can be configured to generate a reset and protect the system.

The internal channel of ADC is ADC_IN8~ADC_IN10. The internal reference voltage V_{REF} is connected to the IN8 input channel; the OPA internal output channel is connected to the IN9 input channel for converting the output of the OPA into digital values; and the internal calibration voltage VCAL is connected to the IN10 input channel, which is half of the system power supply voltage V_{DD}.

1.4.12 Timer and Watchdog

- Advanced-control Timer (TIM1)

The advanced-control timer is a 16-bit automatic load increment / decrement counter with a 16-bit programmable prescaler. In addition to the complete general timer function, it can be regarded as a three-phase PWM generator assigned to 6 channels, with a complementary PWM output function with dead-zone insertion, allowing the timer to be updated after a specified number of counter cycles for repeated counting cycles, braking functions, etc. Advanced control timers have the same functions as general timers and have the same internal structure, so advanced control timers can cooperate with other TIM timers through timer linking function to provide synchronization or event linking functions.

- General-purpose timer (TIM2)

The general-purpose timer is a 16-bit auto-load add / subtract counter with a programmable 16-bit prescaler and 4 independent channels, each of which supports input capture, output comparison, PWM generation and monopulse mode output. By alternate channels 3 and 4, channels 1 and 2 also have complementary PWM output with dead-time insertion. In addition, it can work with the advanced-control timer TIM1 through the timer linking function to provide synchronization or event linking functions. In debug mode, counters can be frozen and any general-purpose timer can be used to generate PWM output.

- Independent Watchdog (IWDG)

Independent watchdog is a free-running 12-bit decreasing counter that supports 7 frequency division coefficients. The clock is provided by an internally independent RC oscillator (LSI) of about 128KHz; the LSI is independent of the master clock and can operate in standby mode. IWDG works completely independently of the main program, so it is used to reset the entire system in the event of a problem, or to provide timeout management for applications as a free timer. The option byte can be configured as a software or hardware startup watchdog. Counters can be frozen in debug mode.

- Window Watchdog (WWDG)

Window watchdog is a 7-bit decrement counter and can be set to run freely. Can be used to reset the entire system when a problem occurs. It is driven by the main clock and has the function of early warning interrupt; in debug mode, the counter can be frozen.

- SysTick Timer (SysTick)

QingKe microprocessor core comes with a 32-bit incremental counter for generating SYSTICK exceptions (exception number: 15), which can be specially used in real-time operating systems to provide "heartbeat" rhythm for the system, and can also be used as a standard 32-bit counter. It has automatic reload function and programmable clock source.

1.4.13 Universal Synchronous/Asynchronous Receiver Transmitter (USART)

The chip provides 1 set of USART. Support full-duplex asynchronous serial communication and half-duplex single-wire communication, also support LIN (Local Internet), compatible with IrDA SIR ENDEC transmission codec specification, and modem (CTS/RTS hardware flow control) operation, but also support multiprocessor communication. It adopts fractional baud rate generator system and supports continuous communication of DMA operation.

1.4.14 Serial Peripheral Interface (SPI)

The chip provides a serial peripheral SPI interface, which supports master or slave operation and dynamic switching. Support multi-master mode, full-duplex or half-duplex synchronous transmission, support basic SD card and MMC mode. Programmable clock polarity and phase, data bit width provides 8- or 16-bit choice, reliable communication hardware CRC generation / check, support DMA operation continuous communication.

1.4.15 I2C Bus

The chip provides an I2C bus interface, which can work in multi-host mode or slave mode, and complete all I2C bus specific timing, protocol, arbitration and so on. Both standard and fast communication speeds are supported.
The I2C interface provides 7-bit or 10-bit addressing and supports double-slave address addressing in 7-bit slave mode. Built-in hardware CRC generator / verifier.

1.4.16 General-purpose Input and Output (GPIO)

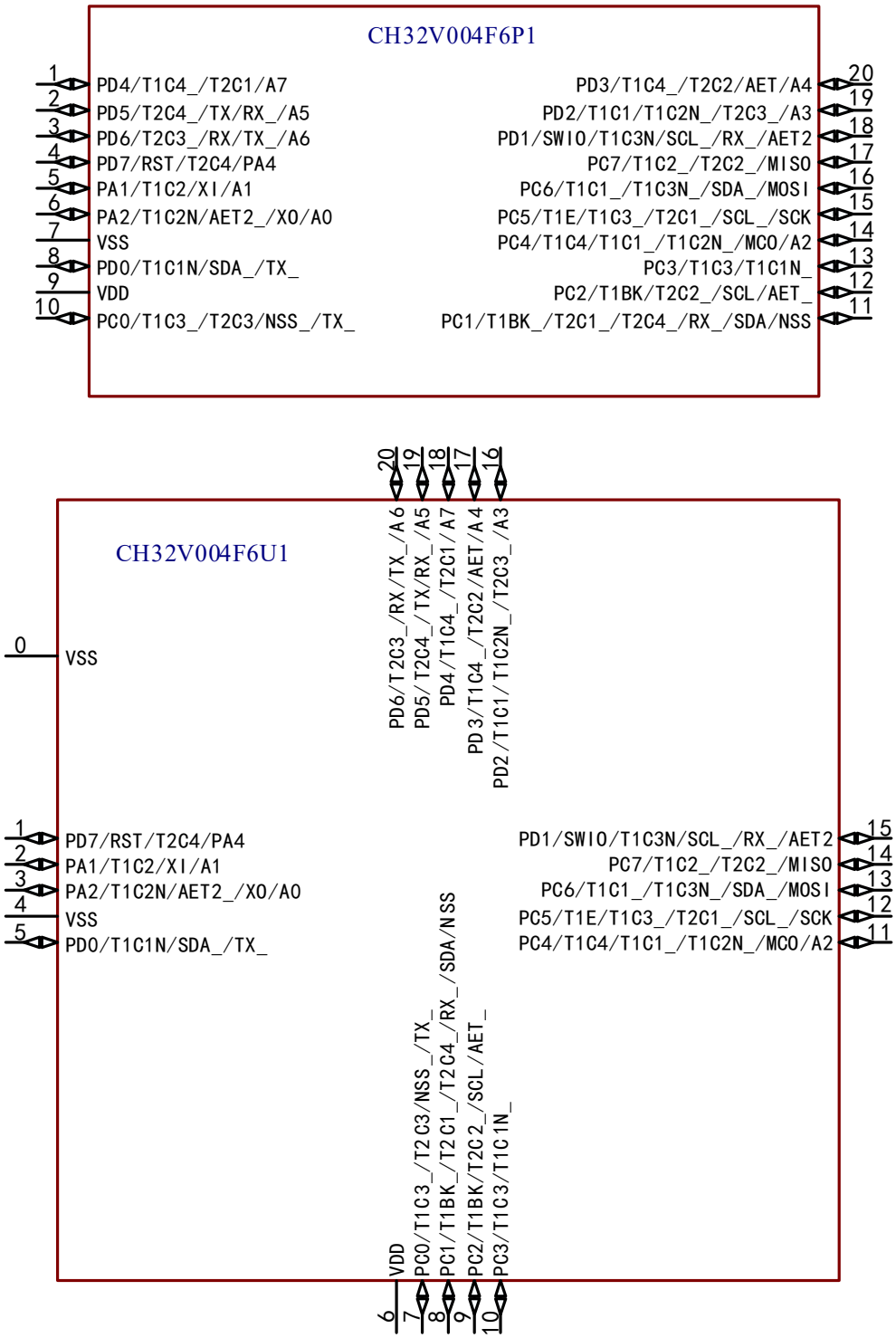
The system provides 3 sets of GPIO ports (PA0~PA7, PB0~PB6, PC0~PC7, PD0~PD7) with a total of 18 GPIO pins. Most pins can be configured by software to output (push-pull or open-drain), input (with or without pull-up or pull-down), or alternate peripheral function ports.
When PA1 and PA2 are crystal pins, i.e., PA1PA2_RM = 1, PA1 and PA2 cannot be used for GPIO functions.
All GPIO pins support controllable pull-up and pull-down resistors. When PD7 is used as reset pins, the pull-up resistor is turned on and the pull-down resistor is turned off by default.
All GPIO pins are shared with digital or analog alternate peripherals. All GPIO pins have a large current drive capability. A locking mechanism is provided to freeze the I/O configuration to avoid accidental writing to the I/O register.
The power supply of all the I/O pins in the system is provided by the V_{DD}. By changing the V_{DD} power supply, the output level of the I/O pin will be changed to adapt to the external communication interface level. Please refer to the pin description for the specific pin.

1.4.17 1-wire Serial Debug Interface (SDI)

The core comes with 1-wire SDI Serial Debug Interface, which corresponds to SWIO pin (Single Wire Input Output). The debug interface pin function is turned on by default after the system is powered on or reset, and the SDI can be turned off according to the need after the main program is running. The HSI clock must be turned on when using the 1-wire emulation debug interface.

Chapter 2 Pinouts and Pin Definition

2.1 Pinouts



Note: The multiplexed functions in the pin diagram are abbreviated.

Example: A: ADC_ (A1: ADC_IN1, AET: ADC_RETR, AET2: ADC_IETR)

T1: TIM1_ (T1C1: TIM1_CH1、T1C1N: TIM1_CH1N, T1BK: TIM1_BKIN, T1E: TIM1_ETR)

T2: TIM2_ (T2C1: TIM2_CH1_ETR, T2C2: TIM2_CH2)
USART1_ (RX: USART1_RX, TX: USART1_TX)
I2C_ (SDA: I2C_SDA, SCL: I2C_SCL)
SPI_ (SCK: SPI_SCK, NSS: SPI_NSS, MISO: SPI_MISO, MOSI: SPI_MOSI)

2.2 Pin Description

Note: The pin function descriptions in the table below are for all functions and do not relate to specific model products. Peripheral resources may vary between models, so please check the availability of this function according to the product model resource table before viewing.

Table 2-1 CH32V004 Pin definitions

Pin No.		Pin name	Pin type(1)	Main function (after reset)	Default alternate function	Remapping function(2)
QFN20	TSSOP20					
0	-	V_{SS}	P	V_{SS}		
18	1	PD4	I/O/A	PD4	ADC_IN7/TIM2_CH1_ETR	TIM1_CH4_3/TIM1_ETR_1/ TIM1_ETR_4/TIM1_ETR_5/ TIM1_ETR_6/TIM2_CH2_7/ USART1_RTS_9/SPI_SCK_4
19	2	PD5	I/O/A	PD5	ADC_IN5/USART1_TX	TIM2_CH4_3/USART1_RX_1/ USART1_CTS_9/SPI_MISO_4
20	3	PD6	I/O/A	PD6	ADC_IN6/USART1_RX	TIM2_CH3_3/USART1_TX_1/ SPI_MOSI_4
1	4	PD7(3)	I/O	PD7	TIM2_CH4/RST	TIM2_CH4_1/USART1_CTS_4/ USART1_CTS_5
		PA4(3)	I/O	PA4		
2	5	PA1	I/O/A	PA1	ADC_IN1/TIM1_CH2	XI/TIM1_CH2_1/TIM1_CH2_9/ TIM2_CH2_5/TIM2_CH2_6/ USART1_RX_8/SPI_SCK_5
3	6	PA2	I/O/A	PA2	ADC_IN0/TIM1_CH2N	X0/TIM1_CH3_9/TIM1_CH2N_1/ TIM1_CH2N_4/TIM1_CH2N_5/ TIM1_CH2N_6/TIM2_CH3_5/ TIM2_CH3_6/TIM2_CH3_7/ SPI_MOSI_5/ADC_IETR_1
4	7	V_{SS}	P	V_{SS}		

Pin No.		Pin name	Pin type(1)	Main function (after reset)	Default alternate function	Remapping function(2)
QFN20	TSSOP20					
5	8	PD0	I/O	PD0	TIM1_CH1N	TIM1_CH1N_1/TIM1_CH3N_4/ TIM1_CH3N_5/TIM1_CH3N_6/ USART1_TX_2/I2C_SDA_1
6	9	V_{DD}	P	V_{DD}		
7	10	PC0	I/O	PC0	TIM2_CH3	TIM1_CH3_2/TIM1_CH1N_7/ TIM1_CH1N_9/TIM2_CH1_ETR_4/ TIM2_CH3_1/USART1_TX_3/ SPI_NSS_1/SPI_MOSI_3
8	11	PC1	I/O	PC1	I2C_SDA/SPI_NSS	TIM1_CH2N_7/TIM1_CH2N_9/ TIM1_BKIN_2/TIM1_BKIN_3/ TIM2_CH1_ETR_1/TIM2_CH2_4/ TIM2_CH1_ETR_3/TIM2_CH4_2/ USART1_RX_3/SPI_NSS_5
9	12	PC2	I/O	PC2	TIM1_BKIN/USART1_RTS/ I2C_SCL	TIM1_CH3N_7/TIM1_CH3N_9/ TIM2_CH2_2/USART1_RTS_2/ TIM1_BKIN_1/TIM1_ETR_3/ ADC_RETR_1
10	13	PC3	I/O	PC3	TIM1_CH3	TIM1_CH3_1/TIM1_CH3_5/ TIM1_CH1N_2/TIM1_CH1N_3/ TIM2_CH3_4/USART1_CTS_2
11	14	PC4	I/O	PC4	ADC_IN2/TIM1_CH4/MCO	TIM1_CH1_3/TIM1_CH1_7/ TIM1_CH1_8/TIM1_CH4_1/ TIM1_CH2N_2/USART1_RX_9/ SPI_NSS_2/SPI_NSS_6/
12	15	PC5	I/O	PC5	TIM1_ETR/SPI_SCK	TIM1_CH2_7/TIM1_CH2_8/

Pin No.		Pin name	Pin type(1)	Main function (after reset)	Default alternate function	Remapping function(2)
QFN20	TSSOP20					
						TIM1_CH3_3/TIM1_ETR_2/ TIM2_CH1_ETR_2/USART1_TX_6/ I2C_SCL_2/SPI_SCK_1
13	16	PC6	I/O	PC6	SPI_MOSI	TIM1_CH1_2/TIM1_CH3_7/ TIM1_CH3_8/TIM1_CH3N_3/ USART1_RX_6/USART1_CTS_1/ USART1_CTS_3/SPI_MOSI_1/ I2C_SDA_2
14	17	PC7	I/O	PC7	SPI_MISO	TIM1_CH2_2/TIM1_CH2_3/ TIM1_CH4_7/TIM1_CH4_8/ TIM2_CH2_3/USART1_CTS_6/ USART1_CTS_7/USART1_RTS_1/ USART1_RTS_3/SPI_MISO_1/ SPI_MISO_6
15	18	PD1	I/O/A	PD1	TIM1_CH3N/SWIO/ ADC_IETR	TIM1_CH4_4/TIM1_CH4_5/ TIM1_CH3N_1/TIM1_CH3N_2/ USART1_TX_4/USART1_RX_2/ USART1_RX_5/I2C_SCL_1/ I2C_SDA_4
16	19	PD2	I/O/A	PD2	ADC_IN3/TIM1_CH1	TIM1_CH1_1/TIM1_CH2N_3/ TIM2_CH3_2/USART1_CTS_8/ SPI_SCK_2
17	20	PD3	I/O/A	PD3	ADC_IN4/TIM2_CH2/ USART1_CTS/ADC_RETR	TIM1_CH4_2/TIM2_CH1_ETR_7/ TIM2_CH2_1/USART1_RTS_8/ SPI_NSS_4/SPI_MOSI_2

Note 1: Explanation of table abbreviations:

I = TTL/CMOS level Schmitt input; O = CMOS level tri-state output.

A = Analog signal input or output; P = Power supply.

Note 2: The underlined value of the remapping function indicates the configuration value of the corresponding bit in the AFIO register. For example, TIM1_CH4_3 indicates that the corresponding bit in the AFIO register is configured as 011b.

Note 3: For the CH32V004 chip, the PA4 and PD7 pins are shorted inside the chip to prevent both I/Os from being configured as output functions.

2.3 Pin Alternate Functions

Note: The pin function descriptions in the table below are for all functions and do not relate to specific model products. Peripheral resources may vary between models, so please check the availability of this function according to the product model resource table before viewing.

Table 2-3 Pin alternate and remapping functions

Alternate / Pin	ADC	TIM1	TIM2	USART	SYS	I2C	SPI
PA1	ADC_IN1	TIM1_CH2 TIM1_CH2_1 TIM1_CH2_9	TIM2_CH2_5 TIM2_CH2_6	USART1_RX_8	XI		SPI_SCK_5
PA2	ADC_IN0 ADC_IETR_1	TIM1_CH3_9 TIM1_CH2N TIM1_CH2N_1 TIM1_CH2N_4 TIM1_CH2N_5 TIM1_CH2N_6	TIM2_CH3_5 TIM2_CH3_6 TIM2_CH3_7		XO		SPI_MOSI_5
PC0		TIM1_CH3_2 TIM1_CH1N_7 TIM1_CH1N_9	TIM2_CH1_ETR_4 TIM2_CH3 TIM2_CH3_1	USART1_TX_3			SPI_NSS_1 SPI_MOSI_3
PC1		TIM1_CH2N_7 TIM1_CH2N_9 TIM1_BKIN_2 TIM1_BKIN_3	TIM2_CH1_ETR_1 TIM2_CH1_ETR_3 TIM2_CH2_4 TIM2_CH4_2	USART1_RX_3		I2C_SDA	SPI_NSS SPI_NSS_5
PC2	ADC_RETR_1	TIM1_CH3N_7 TIM1_CH3N_9 TIM1_BKIN TIM1_BKIN_1 TIM1_ETR_3	TIM2_CH2_2	USART1_RTS USART1_RTS_2		I2C_SCL	
PC3		TIM1_CH3 TIM1_CH3_1 TIM1_CH3_5 TIM1_CH1N_2 TIM1_CH1N_3	TIM2_CH3_4	USART1_CTS_2			
PC4	ADC_IN2	TIM1_CH1_3 TIM1_CH1_7 TIM1_CH1_8 TIM1_CH4 TIM1_CH4_1 TIM1_CH2N_2		USART1_RX_9	MCO		SPI_NSS_2 SPI_NSS_6
PC5		TIM1_CH2_7 TIM1_CH2_8 TIM1_CH3_3	TIM2_CH1_ETR_2	USART1_TX_6		I2C_SCL_2	SPI_SCK SPI_SCK_1

Alternate / Pin	ADC	TIM1	TIM2	USART	SYS	I2C	SPI
		TIM1_ETR TIM1_ETR_2					
PC6		TIM1_CH1_2 TIM1_CH3_7 TIM1_CH3_8 TIM1_CH3N_3		USART1_RX_6 USART1_CTS_1 USART1_CTS_3		I2C_SDA_2	SPI_MOSI SPI_MOSI_1
PC7		TIM1_CH2_2 TIM1_CH2_3 TIM1_CH4_7 TIM1_CH4_8	TIM2_CH2_3	USART1_CTS_6 USART1_CTS_7 USART1_RTS_1 USART1_RTS_3			SPI_MISO SPI_MISO_1 SPI_MISO_6
PD0		TIM1_CH1N TIM1_CH1N_1 TIM1_CH3N_4 TIM1_CH3N_5 TIM1_CH3N_6		USART1_TX_2		I2C_SDA_1	
PD1	ADC_IETR	TIM1_CH4_4 TIM1_CH4_5 TIM1_CH3N TIM1_CH3N_1 TIM1_CH3N_2		USART1_TX_4 USART1_RX_2 USART1_RX_5	SWIO SWDIO	I2C_SCL_1 I2C_SDA_4	
PD2	ADC_IN3	TIM1_CH1 TIM1_CH1_1 TIM1_CH2N_3	TIM2_CH3_2	USART1_CTS_8			SPI_SCK_2
PD3	ADC_IN4 ADC_RETR	TIM1_CH4_2	TIM2_CH1_ETR_7 TIM2_CH2 TIM2_CH2_1	USART1_CTS USART1_RTS_8			SPI_NSS_4 SPI_MOSI_2
PD4	ADC_IN7	TIM1_CH4_3 TIM1_ETR_1 TIM1_ETR_4 TIM1_ETR_5 TIM1_ETR_6	TIM2_CH1_ETR TIM2_CH2_7	USART1_RTS_9			SPI_SCK_4
PD5	ADC_IN5		TIM2_CH4_3	USART1_TX USART1_RX_1 USART1_CTS_9			SPI_MISO_4
PD6	ADC_IN6		TIM2_CH3_3	USART1_TX_1 USART1_RX			SPI_MOSI_4
PD7			TIM2_CH4 TIM2_CH4_1	USART1_CTS_4 USART1_CTS_5	RST		

Chapter 3 Electrical Characteristics

3.1 Test Condition

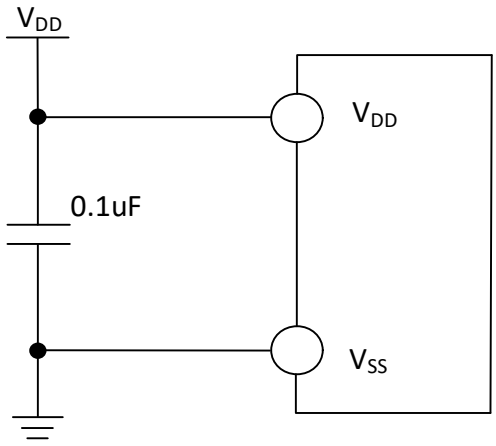
Unless otherwise specified and marked, all voltages are based on V_{SS}.

All minimum and maximum values will be guaranteed under the worst ambient temperature, supply voltage and clock frequency. Typical values are based on room temperature 25℃ and V_{DD}=3.3V or 5V for design guidance.

Data obtained through comprehensive evaluation, design simulation or process characteristics will not be tested on the production line. On the basis of comprehensive evaluation, the minimum and maximum values are obtained through sample testing. Unless the special instructions are measured, the characteristic parameters are guaranteed by comprehensive evaluation or design.

Power supply scheme:

Figure 3-1 Typical circuit for conventional power supply



3.2 Absolute Maximum Ratings

Stresses at or above the absolute maximum ratings listed in the table below may cause permanent damage to the device.

Table 3-1 Absolute maximum ratings

Symbol	Description	Min.	Max.	Unit
T_A	Ambient temperature during operation	-10	70	℃
T_S	Ambient temperature during storage	-40	125	℃
V_{DD}-V_{SS}	External main supply voltage (V_{DD})	-0.3	5.5	V
V_{IN}	Input voltage on the I/O pin	V_{SS}-0.3	V_{DD}+0.3	V
$\|\triangle V_{DD\_x}\|$	Variations between different main power supply pins		50	mV
$\|\triangle V_{SS\_x}\|$	Variations between different ground pins		50	mV
$V_{ESD(HBM)}$	Electrostatic discharge voltage (HBM) of ordinary I/O pin	4K		V

I_{VDD}	Total current of all V_{DD} main power pins		100	mA
I_{VSS}	Total current of all V_{SS} common ground pins		200	mA
I_{IO}	Sink current on any I/O and control pin		30	mA
	Output current on any I/O and control pin		-30	
$I_{INJ(PIN)}$	XI pin of HSE		+/-4	
	Injected current on other pins		+/-4	
$\sum I_{INJ(PIN)}$	Total injected current on all I/Os and control pins		+/-20	

3.3 Electrical Characteristics

3.3.1 Operating Conditions

Table 3-2 General operating conditions

Symbol	Parameter	Condition	Min.	Max.	Unit
F_{HCLK} or F_{SYS}	Internal system bus frequency Or microprocessor main frequency			48	MHz
V_{DD}	Standard operating voltage		2.7	5.5	V
T_A	Ambient temperature		-10	70	℃
T_J	Junction temperature range		0	100	℃

Table 3-3 Power-on and power-down conditions

Symbol	Parameter	Condition	Min.	Max.	Unit
t_{VDD}	V_{DD} rising rate		0	20000	us/V
	V_{DD} falling rate		40	20000	

3.3.2 Embedded Reset and Power Control Block Characteristics

Table 3-4 Reset and voltage monitor (For PDR, select high threshold gear)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$V_{POR/PDR}$	Power-on / power-down reset threshold	Rising edge	1.7	1.85	2.0	V
		Falling edge	1.6	1.75	1.9	V
$V_{PDRhyst}$	PDR hysteresis		60	80	100	mV

$t_{RSTTEMPO}$	Power-on reset	RST_MODE[1:0] = 11		2		ms
	Other reset			300		us

Note: 1. Normal temperature test value.

3.3.3 Embedded Reference Voltage

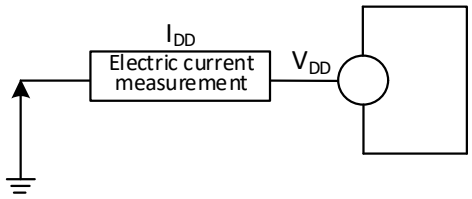
Table 3-5 Embedded reference voltage

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{REFINT}	Internal reference voltage	T_A = -10℃~70℃	1.18	1.2	1.22	V
$T_{S\_vrefint}$	ADC sampling time when reading the internal reference voltage	Slow sampling is recommended.	3		240	$1/f_{ADC}$

3.3.4 Supply Current Characteristics

Current consumption is a comprehensive index of a variety of parameters and factors. These parameters and factors include operating voltage, ambient temperature, I/O pin load, the software configuration of the product, the operating frequency, flip rate of the I/O pin, the location of the program in memory and the executed code, etc. The current consumption measurement method is as follows:

Figure 3-2 Current consumption measurement



The microcontroller is in the following conditions:

In the case of room temperature V_{DD} = 3.3V or 5V, during the test: all I/O ports are configured with pull-down input, HSI = 24MHz (calibrated), and the bit LDO_MODE of register PWR_CTLR is 10. Enable or disable the power consumption of all peripheral clocks.

Table 3-6 Typical current consumption in Run mode, data processing code runs from the internal Flash

Symbol	Parameter	Condition			Typ.		Unit
		HSI/HSE	HSI_LP	F_{HCLK}	All peripherals enabled	All peripherals disabled	
I_{DD}(1)	Supply current in Run mode	Runs on the high-speed external clock	X	F_{HCLK} = 48MHz	4.3	3.4	mA
				F_{HCLK} =	3.3	2.8	

		(HSE) (HSE_SI = 00, HSE_LP = 1)		24MHz			
				F_{HCLK} = 16MHz	2.8	2.5	
				F_{HCLK} = 8MHz	2.5	2.4	
				F_{HCLK} = 750KHz	1.7	1.7	
		Runs on the high-speed internal RC oscillator (HSI)	0	F_{HCLK} = 48MHz	3.6	2.7	
				F_{HCLK} = 24MHz	2.5	2.0	
				F_{HCLK} = 16MHz	2.1	1.7	
				F_{HCLK} = 8MHz	1.8	1.6	
				F_{HCLK} = 750KHz	0.9	0.9	
			1	F_{HCLK} = 40KHz	0.6	0.6	

Note: The above are measured parameters.

Table 3-7 Typical current consumption in Sleep mode, data processing code runs from internal Flash or SRAM

Symbol	Parameter	Condition			Typ.		Unit
		HSI/HSE	HSI_LP	F_{HCLK}	All peripherals enabled	All peripherals disabled	
I_{DD}(1)	Supply current in Sleep mode (In this case, peripheral	Runs on the high-speed external clock (HSE) (HSE_SI = 00,	X	F_{HCLK} = 48MHz	3.0	2.1	mA
				F_{HCLK} = 24MHz	2.3	1.8	
				F_{HCLK} =	2.1	1.8	

	power supply and clock are maintained)	HSE_LP = 1)		16MHz			
				F_{HCLK} = 8MHz	1.8	1.7	
				F_{HCLK} = 750KHz	1.6	1.6	
		Runs on the high-speed internal RC oscillator (HSI)	0	F_{HCLK} = 48MHz	2.2	1.3	
				F_{HCLK} = 24MHz	1.5	1.0	
				F_{HCLK} = 16MHz	1.3	1.0	
				F_{HCLK} = 8MHz	1.1	0.9	
				F_{HCLK} = 750KHz	0.9	0.9	
			1	F_{HCLK} = 40KHz	0.6	0.6	

Note: The above are measured parameters.

Table 3-8 Typical current consumption in Standby mode

Symbol	Parameter	Condition			Typ.	Unit
		Independent watchdog	LSI	V_{DD}		
I_{DD}	Supply current in Standby mode	Enable	Disable	3.3V	10.7	uA
				5V	11.6	
		Disable	Disable	3.3V	10.2	
				5V	11.1	
		Disable	Enable	3.3V	10.6	
				5V	11.6	

Note: The above are measured parameters.

3.3.5 External Clock Source Characteristics

Table 3-9 From external high-speed clock

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{HSE_ext}	External clock frequency		3	24	32	MHz
V_{HSEH}(1)	XI input pin high level voltage		0.8V_{DD}		V_{DD}	V
V_{HSEL}(1)	XI input pin low-level voltage		0		0.2V_{DD}	V
$C_{in(HSE)}$	XI input capacitance			5		pF
$DuCy_{(HSE)}$	Duty cycle		40	50	60	%
I_L	XI input leakage current				±1	uA

Note: 1. Failure to meet this condition may cause level recognition error.

Figure 3-3 External high-frequency clock source circuit

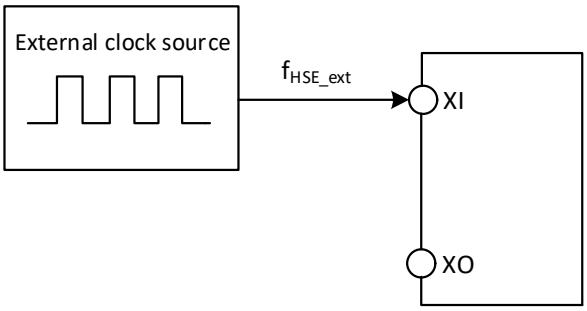


Table 3-10 High-speed external clock generated from a crystal/ceramic resonator

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{XI}	Resonator frequency		3	24	32	MHz
R_F	Feedback resistor (no external)			250		kΩ
C_{LOAD}	Recommended load capacitance and corresponding crystal series impedance R_S	R_S = 60Ω(1)		20		pF
I_{HSE}	HSE drive current	HSE_LP = 0, 20p load		1.6		mA
		HSE_LP = 1, 20p load		0.8		
g_m	Oscillator transconductance	Startup		21		mA/V
$t_{SU(HSE)}$	Startup time	V_{DD} is stable		1.5 (2)		ms

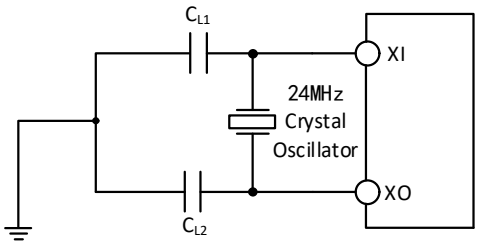
Note: 1. 25M crystal ESR is recommended not more than 80Ω, less than 25m can be appropriately relaxed.

2. Startup time refers to the time difference between when HSEON is turned on and when HSERDY is set.

Circuit reference design and requirements:

The load capacitance of the crystal is subject to the recommendation of the crystal manufacturer, generally C_{L1} = C_{L2}.

Figure 3-4 Typical circuit of external 24M crystal



3.3.6 Internal Clock Source Characteristics

Table 3-11 Internal high-speed (HSI) RC oscillator characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{HSI}	Frequency (after calibration)	HSI_LP = 0		24		MHz
		HSI_LP = 1	30	42	58	KHz
$DuCy_{HSI}$	Duty cycle		45	50	55	%
ACC_{HSI}	Accuracy of HSI oscillator (after calibration)	HSI_LP = 0, TA = -10℃~70℃	-2		2	%
$t_{SU(HSI)}$(1)	HSI oscillator startup stabilization time			3	8	us
$I_{DD(HSI)}$	HSI oscillator power consumption	HSI_LP = 0		200		uA
		HSI_LP = 1		8.5		

Note: 1. Register RCC_CTLR HSION is set to 1 and wait for HSIRDY to be set to 1.

Table 3-12 Internal low-speed (LSI) RC oscillator characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{LSI}	Frequency		90	128	172	KHz
$DuCy_{LSI}$	Duty cycle		45	50	55	%
$t_{SU(LSI)}$(1)	LSI oscillator startup stabilization time			30	100	us
$I_{DD(LSI)}$(1)	LSI oscillator power consumption			550		nA

Note: 1. Register RCC_CTLR LSION is set to 1 and wait for LSIRDY to be set to 1.

3.3.7 Wakeup Time from Low-power Mode

Table 3-13 Wakeup time from low-power mode(1)

Symbol	Parameter	Condition	Typ.	Unit
$t_{WUSLEEP}$	Wakeup from Sleep mode	Use HSI RC clock to wakeup	10	us
$t_{WUSTDBY}$	Wakeup from Standby mode	LDO stabilization time + HSI RC clock wake up	250	us

Note: The above are measured parameters.

3.3.8 Memory Characteristics

Table 3-14 Flash memory characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{prog_page}	Page (256 bytes) program time			1.5	2.0	ms
t_{erase_page}	Page (256 bytes) erase time			2.5	3.0	ms
t_{erase_sec}	Sector (1K bytes) erase time			2.7	3.3	ms

Table 3-15 Flash memory endurance and data retention

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
N_{END}	Erase and write times	T_A = 25℃	100K			次
t_{RET}	Data retention period		10			年

3.3.9 I/O Port Characteristics

Table 3-16 General-purpose I/O static characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IH}	Standard I/O pin, input high level voltage		0.20*(V_{DD}-2.7)+1.55		V_{DD}+0.3	V
V_{IL}	Standard I/O pin, input low-level voltage		-0.3		0.20*(V_{DD}-2.7)+0.65	V
V_{hys}	Schmitt trigger voltage hysteresis		150			mV
I_{lkg}	Input leakage current				1	uA
R_{PU}	Pull-up equivalent resistance		35	45	55	kΩ

R_{PD}	Pull-down equivalent resistance		35	45	55	kΩ
C_{IO}	I/O pin capacitance			5		pF

Output drive current characteristics

GPIO (General-Purpose Input/Output Port) can sink or output up to ±8mA current, and sink or output ±20mA current (not strictly to V_{OL}/V_{OH}). In user applications, the total driving current of all I/O pins cannot exceed the absolute maximum ratings given in Section 3.2:

Table 3-17 Output voltage characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit
V_{OL}	Output low level, 8 pins input current	TTL port, I_{IO} = +8mA 2.7V< V_{DD} <5.5V		0.4	V
V_{OH}	Output high level, 8 pin output current		V_{DD}-0.4		
V_{OL}	Output low level, 8 pins input current	CMOS port, I_{IO} = +8mA 2.7V< V_{DD} <5.5V		0.4	V
V_{OH}	Output high level, 8 pin output current		2.3		
V_{OL}	Output low level, 8 pins input current	I_{IO} = +20mA 2.7V< V_{DD} <5.5V		1.3	V
V_{OH}	Output high level, 8 pin output current		V_{DD}-1.3		

Note: The sum of current must not exceed the absolute maximum rating given in Section 3.2 of the table if more than one I/O pin is driven at the same time in the above conditions. When multiple I/O pins are driven at the same time, the current on the power supply/ground wire point is very large, which will cause the voltage drop so that the voltage of the internal I/O cannot reach the power supply voltage in the meter, resulting in the drive current less than the nominal value.

Table 3-18 Input/output AC characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit
$F_{max(IO)out}$	Maximum frequency	CL = 50pF,V_{DD} = 2.7-5.5V		30	MHz
$t_{f(IO)out}$	Output high to low fall time	CL = 50pF,V_{DD} = 2.7-5.5V		10	ns
$t_{r(IO)out}$	Output low to high rise time	CL = 50pF,V_{DD} = 2.7-5.5V		10	ns
t_{EXTIpw}	The EXTI controller detects the pulse width of the external signal		10		ns

Note: Above parameters are guaranteed by design.

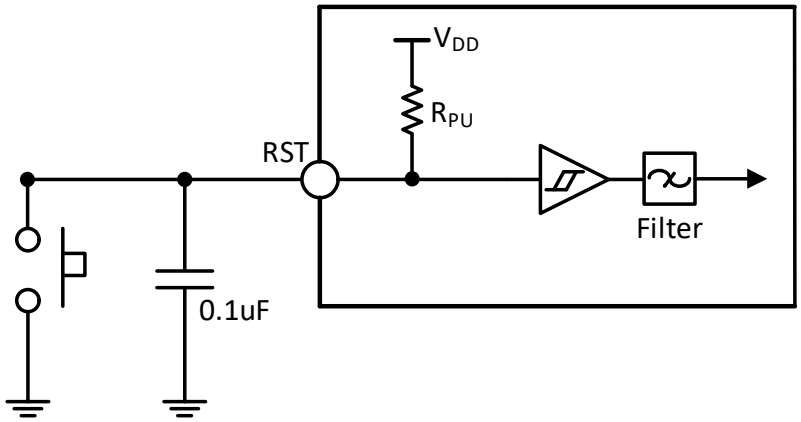
3.3.10 NRST Pin Characteristics

Table 3-19 External reset pin characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$V_{IL(RST)}$	RST input low-level voltage		-0.3		0.20*(V_{DD}-2.7)+0.65	V
$V_{IH(RST)}$	RST input high-level voltage		0.20*(V_{DD}-2.7)+1.55		V_{DD}+0.3	V
$V_{hys(RST)}$	NRST Schmitt Trigger voltage hysteresis		150			mV
R_{PU}	Pull-up equivalent resistance		35	45	55	kΩ
$V_{F(RST)}$	RST input can be filtered pulse width				100	ns
$V_{NF(RST)}$	RST input cannot be filtered pulse width		300			ns

Circuit reference design and requirements:

Figure 3-5 Typical circuit of external reset pin



Note: The capacitance in the figure is optional and can be used to filter out key jitter.

3.3.11 TIM Timer Characteristics

Table 3-20 TIMx characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit
$t_{res(TIM)}$	Timer reference clock		1		$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48MHz	20.8		ns

F_{EXT}	Timer external clock frequency on CH1 to CH4		0	$f_{TIMxCLK}$/2	MHz
		$f_{TIMxCLK}$ = 48MHz	0	24	MHz
R_{esTIM}	Timer resolution			16	位
$t_{COUNTER}$	16-bit counter clock cycle when the internal clock is selected		1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48MHz	0.0208	1363	us
t_{MAX_COUNT}	Maximum possible count			65535	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48MHz		1363	us

3.3.12 I2C Interface Characteristics

Figure 3-6 I2C bus timing diagram

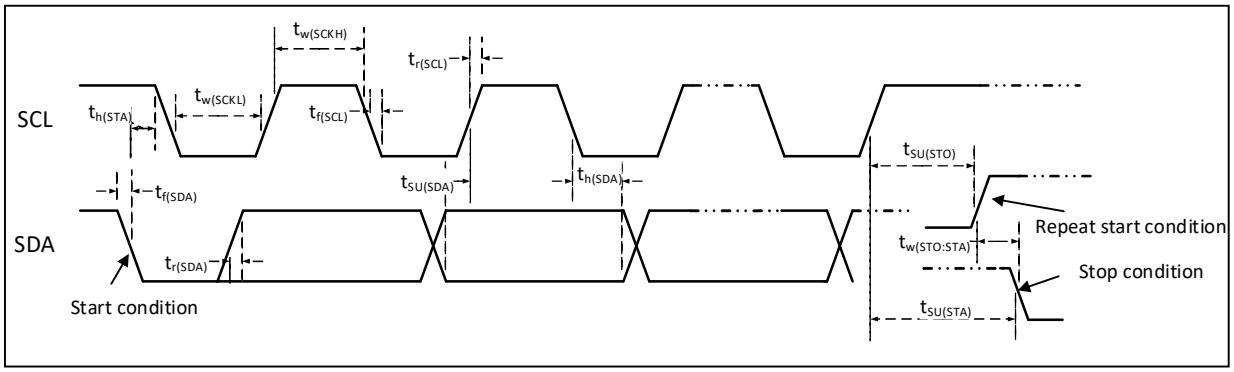


Table 3-21 I2C interface characteristics

Symbol	Parameter	Standard I2C		Fast I2C		Unit
		Min.	Max.	Min.	Max.	
$t_{w(SCKL)}$	SCL clock low-level time	4.7		1.2		us
$t_{w(SCKH)}$	SCL clock high-level time	4.0		0.6		us
$t_{SU(SDA)}$	SDA data setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0		0	900	ns
$t_{r(SDA)}$/$t_{r(SCL)}$	SDA and SCL rise time		1000	20		ns
$t_{f(SDA)}$/$t_{f(SCL)}$	SDA and SCL fall time		300			ns
$t_{h(STA)}$	Start condition hold time	4.0		0.6		us

$t_{SU(STA)}$	Repeated start condition setup time	4.7		0.6		us
$t_{SU(STO)}$	Stop condition setup time	4.0		0.6		us
$t_{w(STO:STA)}$	Time from stop condition to start condition (bus free)	4.7		1.2		us
C_b	Capacitive load for each bus		400		400	pF

3.3.13 SPI Interface Characteristics

Figure 3-7 SPI timing diagram in Master mode

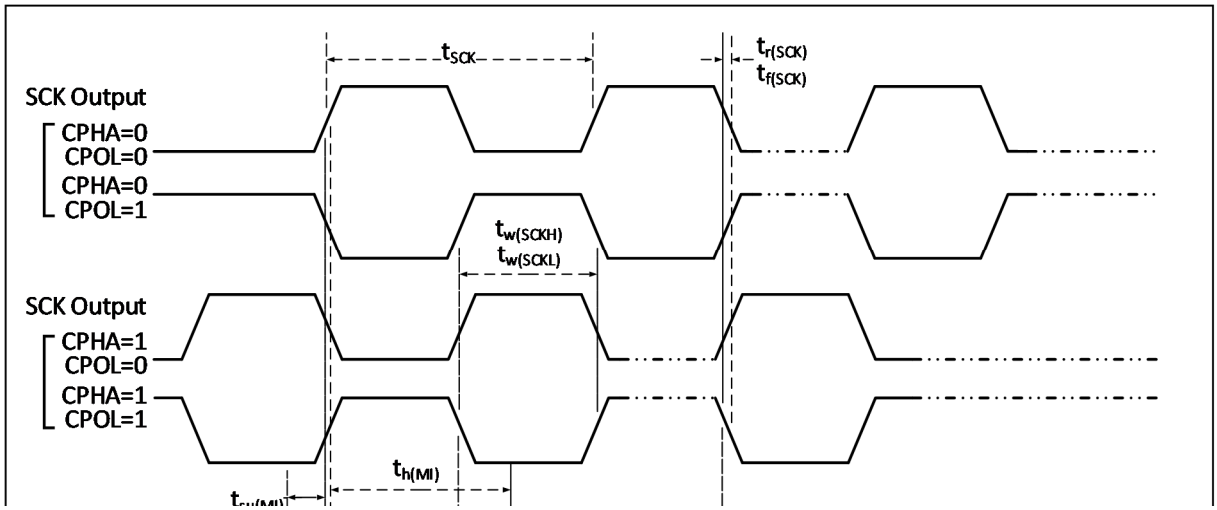


Figure 3-8-1 SPI timing diagram in Slave mode (CPHA = 0, CPOL=0)

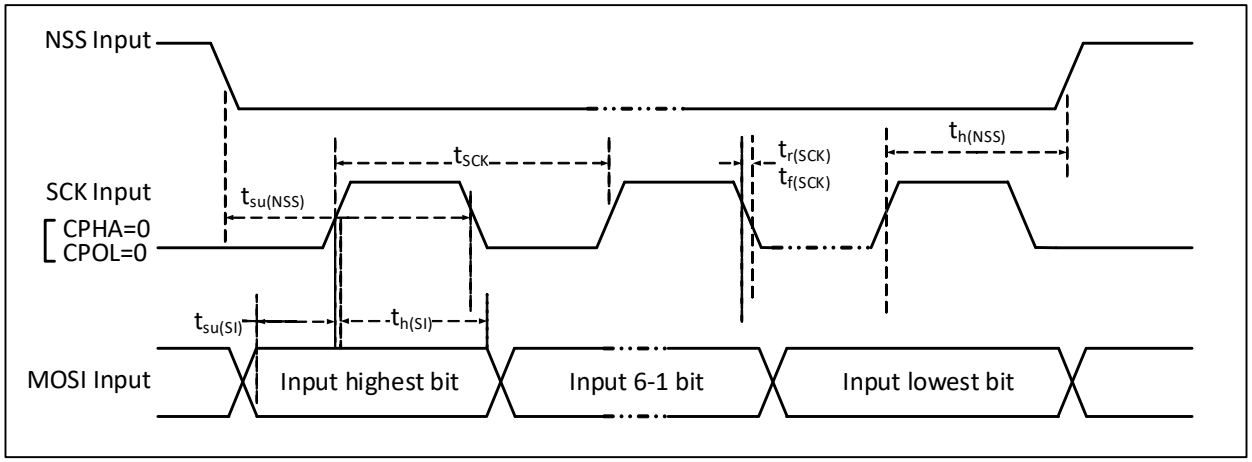


Figure 3-8-2 SPI timing diagram in Slave mode (CPHA = 0, CPOL=1)

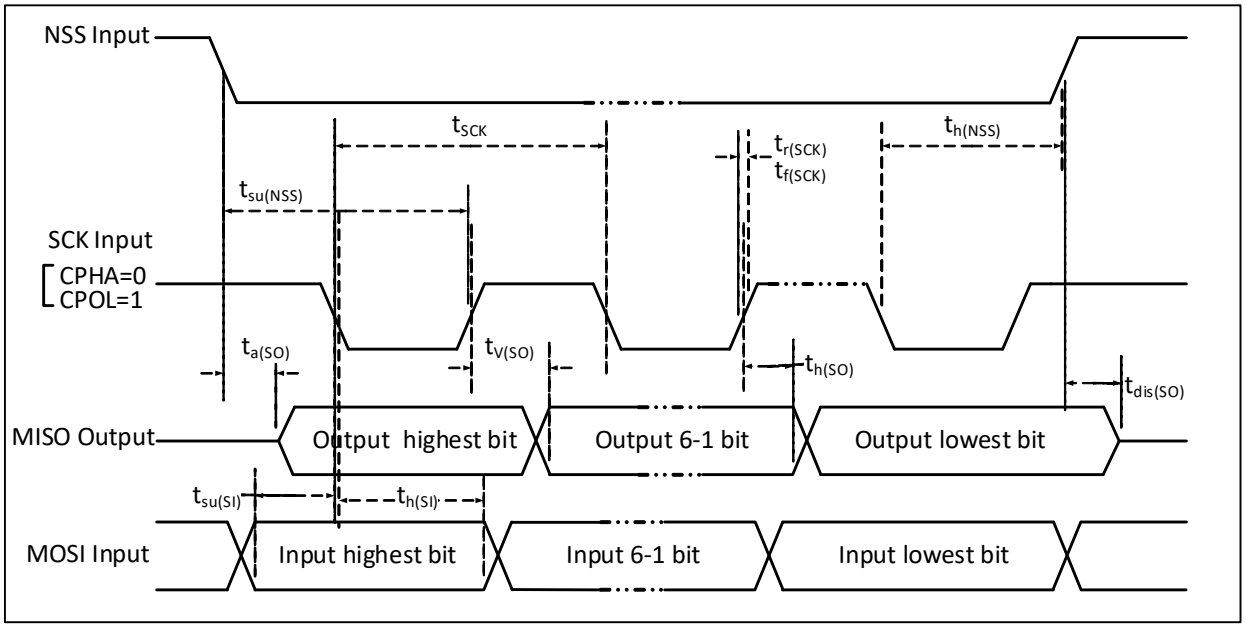


Figure 3-9-1 SPI timing diagram in Slave mode (CPHA = 1, CPOL=0)

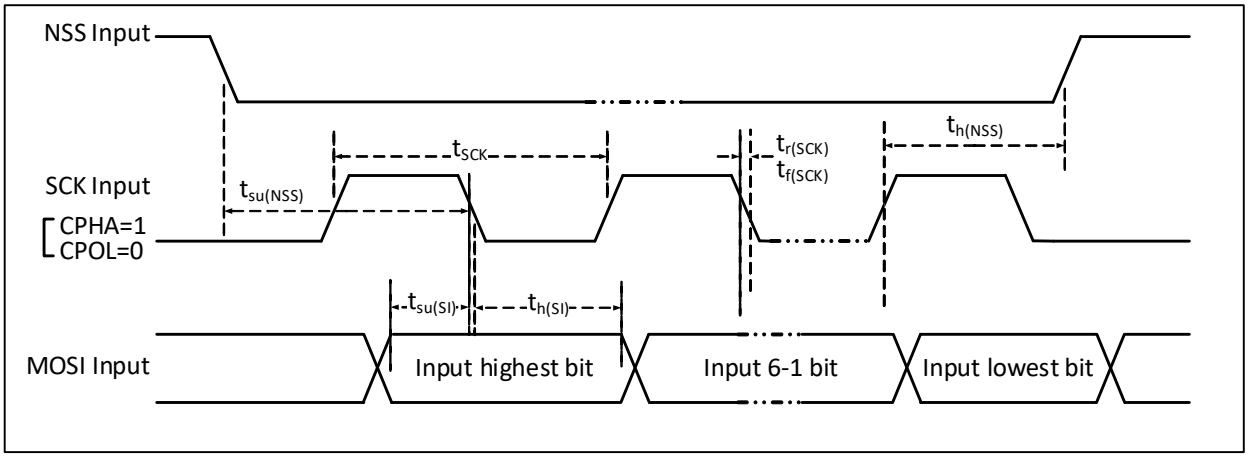


Figure 3-9-2 SPI timing diagram in Slave mode (CPHA = 1, CPOL=1)

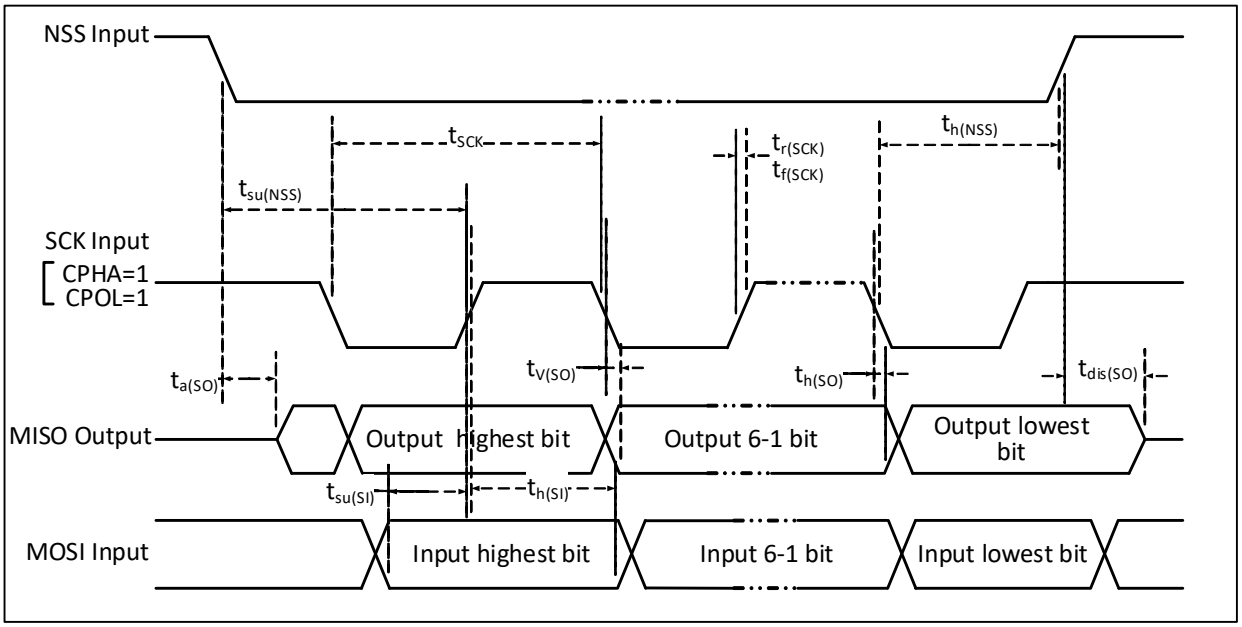


Table 3-22 SPI interface characteristics

Symbol	Parameter	Condition		Min.	Max.	Unit
f_{SCK}/t_{SCK}	SPI clock frequency	Master mode			24	MHz
		Slave mode			24	MHz
$t_{r(SCK)}/t_{f(SCK)}$	SPI clock rise and fall time	Load capacitance: C = 30pF			10	ns
$t_{SU(NSS)}$	NSS setup time	Slave mode		$2t_{HCLK}$		ns
$t_{h(NSS)}$	NSS hold time	Slave mode		$2t_{HCLK}$		ns
$t_{w(SCKH)}/t_{w(SCKL)}$	SCK high and low time	Master mode, f_{HCLK} = 24MHz, Prescaler factor = 4		70	97	ns
$t_{SU(MI)}$	Data input setup time	Master mode	HSRXEN = 0	15		ns
			HSRXEN = 1	$15-0.5t_{SCK}$		
$t_{SU(SI)}$		Slave mode		4		ns
$t_{h(MI)}$	Data input hold time	Master mode	HSRXEN = 0	-4		ns
			HSRXEN = 1	$0.5t_{SCK}-4$		
$t_{h(SI)}$		Slave mode		4		ns
$t_{a(SO)}$	Data output access time	Slave mode, f_{HCLK} = 20MHz		0	$1t_{HCLK}$	ns
$t_{dis(SO)}$	Data output disable time	Slave mode		0	10	ns
$t_{V(SO)}$	Data output valid time	Slave mode (After enable edge)			15	ns

$t_{V(MO)}$		Master mode (After enable edge)		5	ns
$t_{h(SO)}$	Data output hold time	Slave mode (After enable edge)	6		ns
$t_{h(MO)}$		Master mode (After enable edge)	0		ns

3.3.14 10-bit ADC Characteristics

Table 3-23 ADC characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	f_S < 1MHz	2.7		5.5	V
		f_S = 3MHz	4.5		5.5	V
I_{DDA}	ADC supply current (Without buffer)	f_S = 3MHz		1.34		mA
		f_S = 1MHz		0.42		mA
I_{BUF}	ADC buffer own current	ADC_LP = 0		0.68		mA
		ADC_LP = 1		0.13		mA
f_{ADC}	ADC clock frequency			16	48	MHz
f_S	Sampling rate		0.06		3	MHz
f_{TRIG}	External trigger frequency	f_{ADC} = 16MHz			900	KHz
		f_{ADC} = 48MHz			2.7	MHz
					18	$1/f_{ADC}$
V_{AIN}	Switching voltage range		0		V_{DD}	V
R_{AIN}	External input impedance				50	kΩ
R_{ADC}	Sampling switch resistance			0.6	1.5	kΩ
C_{ADC}	Internal sample and hold capacitance			4		pF
t_{CAL}	Calibration time	f_{ADC} = 16MHz			6.25	us
					100	$1/f_{ADC}$
t_{Iat}	Injection trigger conversion delay	f_{ADC} = 16MHz			0.125	us
		f_{ADC} = 48MHz			0.042	us
					2	$1/f_{ADC}$
t_{Iatr}	Conventional trigger conversion	f_{ADC} = 16MHz			0.125	us

	delay	f_{ADC} = 48MHz			0.042	us
					2	$1/f_{ADC}$
t_s	Sampling time	f_{ADC} = 16MHz	0.218		14.97	us
			3.5		239.5	$1/f_{ADC}$
		f_{ADC} = 48MHz	0.073		0.739	us
			3.5		35.5	$1/f_{ADC}$
t_{STAB}	Power-on time				1	us
t_{CONV}	Total conversion time (including sampling time)	f_{ADC} = 16MHz	1		15.75	us
			16		252	$1/f_{ADC}$
		f_{ADC} = 48MHz	0.33		1	us
			16		48	$1/f_{ADC}$

Note: Above parameters are guaranteed by design.

Formula: Maximum R_{AIN}

The above formula is used to determine the maximum external impedance so that the error can be less than 1/4 LSB. Where N = 12 (represents a 12-bit resolution).

Table 3-24-1 Maximum R_{AIN} when f_{ADC} = 16MHz

T_S(Cycle)	t_S(us)	Maximum R_{AIN}(kΩ)
3.5	0.22	4
7.5	0.47	10
13.5	0.84	20
28.5	1.78	45
41.5	2.59	65
55.5	3.47	/
71.5	4.47	/
239.5	14.97	/

Table 3-24-2 Maximum R_{AIN} (High-speed) when f_{ADC} = 48MHz

T_S(Cycle)	t_S(us)	Maximum R_{AIN}(kΩ)

3.5	0.073	1.5
7.5	0.16	3
11.5	0.24	5
19.5	0.41	9
35.5	0.74	17
55.5	1.16	28
71.5	1.49	37
239.5	4.99	/

Table 3-25 ADC error (f_{ADC} = 16MHz, ADC_LP = 1)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
EO	Offset error	R_{AIN} < 10kΩ, V_{DD} = 5V		±2	±6	LSB
ED	Differential nonlinear error			±2	±8	
EL	Integral nonlinear error			±2	±8	

Note: Above parameters are guaranteed by design.

C_p represents the parasitic capacitance on the PCB and the pad (about 5pF), which may be related to the quality of the pad and PCB layout. A larger C_p value will reduce the conversion accuracy, the solution is to reduce the f_{ADC} value.

Figure 3-10 ADC typical connection diagram

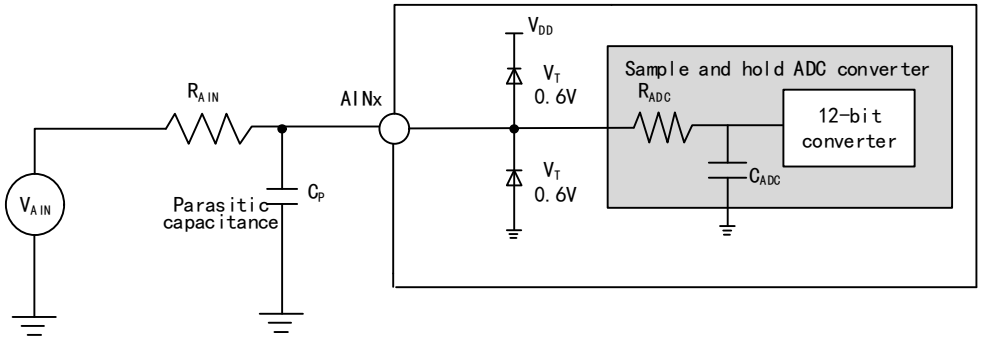
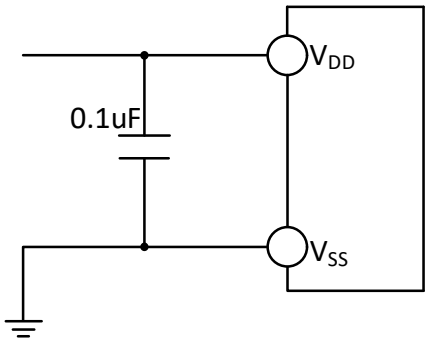


Figure 3-11 Analog power supply and decoupling circuit reference



Chapter 4 Package and Ordering Information

Packages

Package Form	Body Size	Pin Pitch		Package Description	Order Model
TSSOP20	4.4*6.5mm	0.65mm	25.6mil	Thin Shrink Small Outline Package	CH32V004F6P1
QFN20	3*3mm	0.4mm	15.7mil	Quad Flat No-lead Package	CH32V004F6U1

Note: All dimensions are in millimeters. The pin center spacing values are nominal values, with no error. Other than that, the dimensional error is not greater than the greater of ±0.2mm or 10%.

Figure 4-1 TSSOP20 package

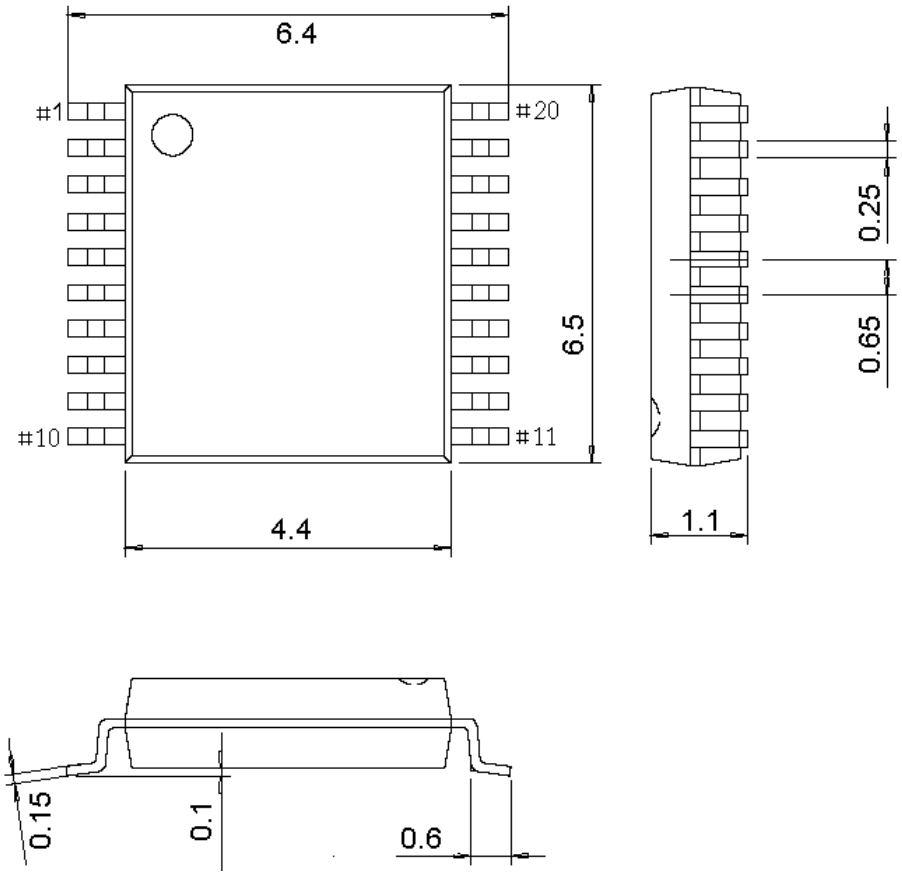


Figure 4-2 QFN20 package

Series Product Naming Rules

Example: CH32 V 303 R 8 T 6

Device family

F = Arm core, general-purpose MCU

V = QingKe RISC-V core, general-purpose MCU

L = QingKe RISC-V core, low-power MCU

X = QingKe RISC-V core, dedicated or special peripherals MCU

M = QingKe RISC-V core, built-in pre-drive motor MCU

Product type (*) + product subseries (*)

Product type	Product subseries
0 = QingKe V2/V4 core, Super value version, system frequency <=48M	02 = 16K Flash memory super value general-purpose 03 = 16K Flash basic general-purpose, OPA 05 = 32K Flash enhanced general-purpose, OPA, dual serial port 06 = 64K Flash versatile, OPA, dual serial port, TKey 07 = Basic motor application, OPA+CMP 35 = Connection, USB, USB PD/Type-C 33 = Connection, USB
1 = M3/QingKe V3/V4 core, Basic version, system frequency<=96M 2 = M3/QingKe V4 non-floating-point core, Enhanced, system frequency <=144M 3 = QingKe V4F floating-point core, Enhanced,	03 = Connection, USB 05 = Connection, USB HS, SDIO, CAN 07 = Interconnected, USB HS, CAN, Ethernet, SDIO, FSMC 08 = Wireless, BLE5.x, CAN, USB, Ethernet 17 = Interconnected, USB HS, CAN, Ethernet (built-in PHY), SDIO, FSMC

system frequency <=144M	

Pin number

J = 8 pins	D = 12 pins	A = 16 pins	F = 20 pins	E = 24 pins
G = 28 pins	K = 32 pins	T = 36 pins	C = 48 pins	R = 64 pins
W = 68 pins	V = 100 pins	Z = 144 pins		

Flash memory size

4 = 16K Flash memory	6 = 32K Flash memory	7 = 48K Flash memory
8 = 64K Flash memory	B = 128K Flash memory	C = 256K Flash memory

Package

T = LQFP	U = QFN	R = QSOP	P = TSSOP	M = SOP

Temperature range

6 = -40℃~85℃ (industrial-grade)	7 = -40℃~105℃ (automotive-grade 2)
3 = -40℃~125℃ (automotive-grade 1)	D = -40℃~150℃ (automotive-grade 0)