Type-C/PD High-Voltage Interface Chip CH211

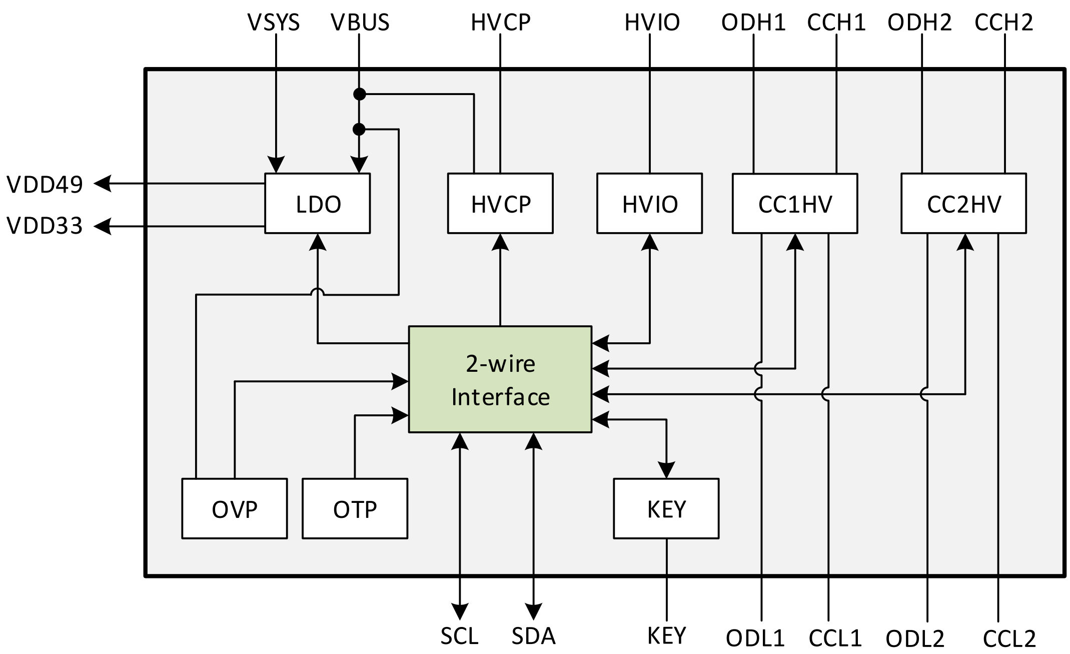
Version: V1.4

https://wch-ic.com

1. Overview

CH211 is a Type-C/PD high-voltage interface chip with built-in high-voltage switch and boost module. The chip has a built-in 4-channel high-voltage switch, which is used to connect the MCU's PD signals to the high-voltage Type-C interface; built-in boost circuit to support external N-type MOSFET power tube control; built-in 2 LDO regulators to support dual high-voltage power inputs; internal integration of VBUS power-up and power-down monitoring, over-voltage monitoring, over-temperature monitoring and other modules; single-pin supports the key detection and wake-up; provide 2-wire control interface and interrupt; can be used for MCU management of Type-C interface power supply and USB PD signal high-voltage expansion, etc.

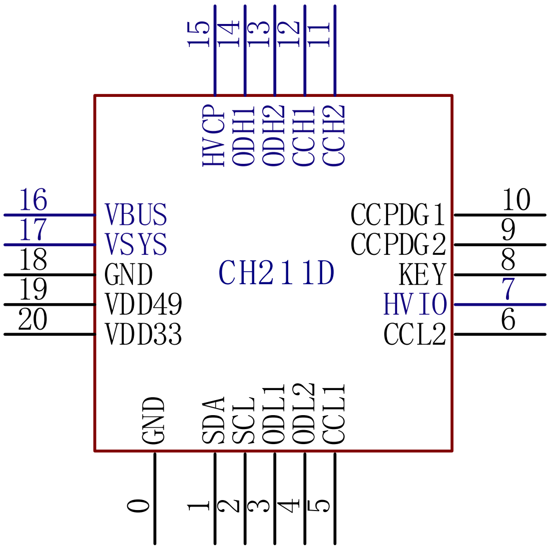
The following is the internal block diagram of CH211, for reference only.

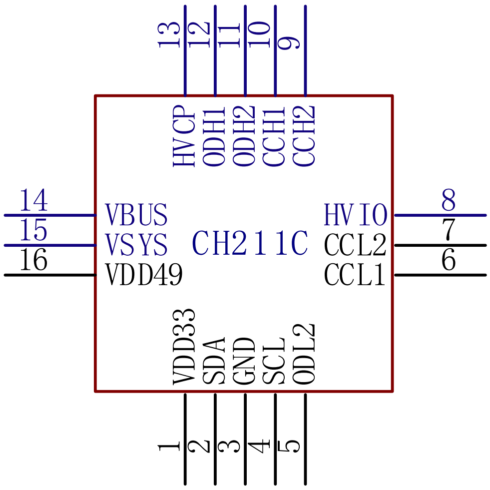


2. Features

- 2 pairs of PD signal high-voltage switch, also do the Type-C interface CC high-voltage signal two choices.
- Built-in boost module HVCP, support external N-type MOSFET power tube gate control.
- Built-in 2-channel high-voltage LDO, support 2-channel power input and automatic switching.
- Single-pin supports power switch key detection and wake-up and P-type MOSFET control, one key switch.
- I2C-compatible 2-wire serial control interface, supports 5V, 3.3V, 2.5V control signals.
- Special designed SCL pin can be reused for interrupt request output, saving MCU pins.
- VBUS supports power discharge, power-up/-down monitoring, supports over-voltage monitoring OVP.
- Built-in chip over-temperature monitoring module OTP.
- Built-in LDO low dropout regulator, output 4.9V and 3.3V for MCU simple power supply.
- Support 28V supply voltage, 30V tolerant voltage for Type-C interface signals.
- ESD support 6KV HBM for Type-C interface signals.
- QFN20 and QFN16C2 packages are available.

3. Pinouts





Package form	Body size		Pin pitch		Package description	Order model
QFN20_3×3	3*3mm		0.4mm	15.7mil	Quad Flat No-lead Package	CH211D
QFN16C_2×2	2*2mm		0.4mm	15.7mil	Quad Flat No-lead Package	CH211C

Note: Pin 0# is for the QFN package EPAD.

Blue pins are for high-voltage support.

CH211C is small in size and is printed with 211C and the lot code on the second line.

4. Pin Definitions

Pin No.		Pin name	Type	Pin description
211D	211C			
17	15	VSYS	High-voltage power	System high voltage power input, usually a standby power supply
16	14	VBUS	High-voltage power	Type-C interface VBUS high-voltage power input, supports discharge and monitoring
19	16	VDD49	Low-voltage power	Internal 4.9V regulator LDO output, external 1uF decoupling capacitor.
20	1	VDD33	Low-voltage power	Internal 3.3V adjustable regulator LDO output, when used, external decoupling capacitor is required.
18,0	3	GND	Power	Common ground
2	4	SCL	Input and open-drain output	Clock input of 2-wire serial interface, configurable as open-drain output of interrupt request.
1	2	SDA	Input and open-drain output	Data input and output of 2-wire serial interface, built-in controllable pull-up resistor.
5	6	CCL1	Low-voltage bidirectional	The low-voltage side port of CC1 of PD signal switch 1#, usually connected to the CC pin of MCU.
12	10	CCH1	High-voltage open-drain	The CC1 high-voltage side port of PD signal switch 1# is off by default, with built-in Rd pull-down resistor, which supports the power supply of output VCONN and is usually connected to CC pin of Type-C.
3	-	ODL1	Low-voltage bidirectional	The through port of OD1 low-voltage side of PD signal switch 1# is connected with ODH1.
14	12	ODH1	High-voltage open-drain	OD1 high-voltage side port of PD signal switch 1# is connected with ODL1 by default, and CCL1 connection can be added optionally.
6	7	CCL2	Low-voltage bidirectional	The CC2 low-voltage side port of PD signal switch 2#, usually connected to the CC pin of MCU.
11	9	CCH2	High-voltage open-drain	The CC2 high-voltage side port of PD signal switch 2# is off by default, with built-in Rd pull-down resistor, which supports the power supply of output VCONN and is usually connected to CC pin of Type-C.
4	5	ODL2	Low-voltage bidirectional	The through port of OD2 low-voltage side of PD signal switch 2#, connected with ODH2.
13	11	ODH2	High-voltage open-drain	OD2 high-voltage side port of PD signal switch 2#, connected with ODL2 by default, and CCL2 connection can be added optionally.
15	13	HVCP	High-voltage output	High voltage output of the boost module, can output low level, VBUS level and VBUS boost.
7	8	HVIO	High-voltage	High-voltage output and input, built-in weak pull-up resistor and

			bidirectional	controllable pull-up resistor, single pin supports key detection and wake-up and P-type MOSFET control.
8	-	KEY	Low-voltage bidirectional	Low-voltage output and input, built-in pull-up resistor, single-pin support for key detection and wake-up and P-type MOSFET control.
10	Internal to GND	CCPDG1	Auxiliary power supply	The low-voltage terminal of controllable Rd pull-down resistor is built into CCH1 pin. If it floats independently, the built-in Rd pull-down resistor is disabled. If PCB is directly connected to GND, pull-down will be enabled by default when powering up, support software to turn it off.
9	Internal to GND	CCPDG2	Auxiliary power supply	The CCH2 pin has a low-voltage terminal with controllable Rd pull-down resistor. If it floats independently, the built-in Rd pull-down resistor is disabled. W If PCB is directly connected to GND, pull-down will be enabled by default when powering up, support software to turn it off.

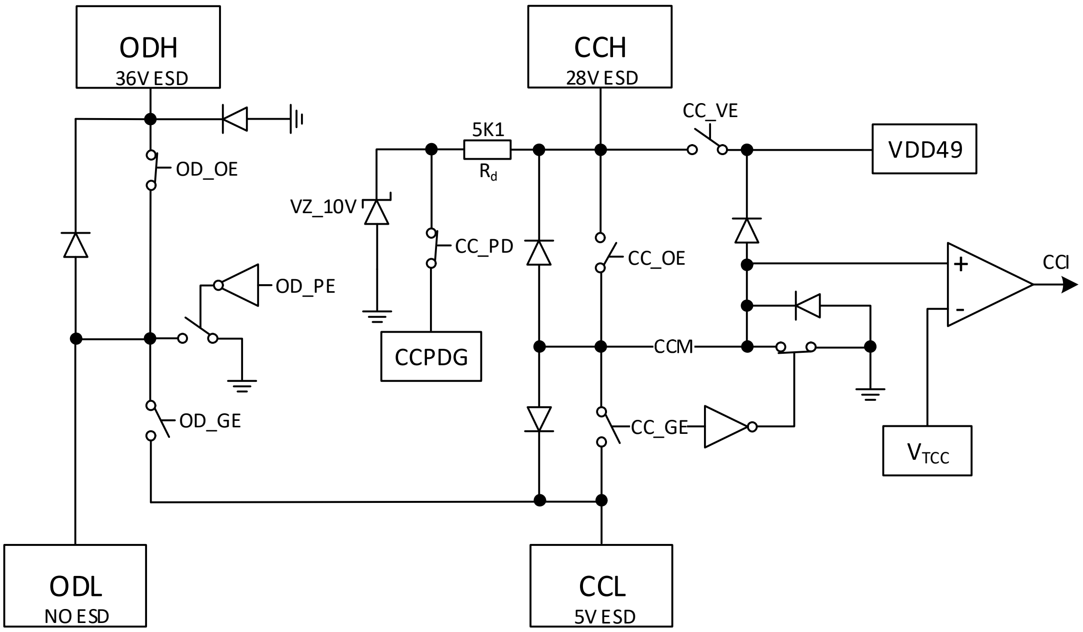
Note: CCPDG1 and CCPDG2 pins are mainly used for internal connection, and the ESD characteristics are poor.
CH211C has internally shorted CCPDG1 and CCPDG2 to GND.
Low-voltage refers to the reference VDD49 power supply voltage, which supports 5V, 3.3V and 2.5V signal levels.
VSYS, VBUS, CCH1 and CCH2 are rated at 5V ~ 28V.
HVCP, ODH1, ODH2 and HVIO are rated at 5V ~ 36V.

5. Function Module

5.1. PD Signal Switch

PD signal high-voltage switch includes CC channel and OD channel, which is used to isolate the high-voltage of Type-C interface, and prevent the CC pin of MCU from directly bearing unexpected high voltage while maintaining PD signal transmission. CH211 has 2 pairs of PD signal high-voltage switches, which can support up to 4 CC signals.

Refer to the figure below for the structure of PD signal high-voltage switch.



The CCH pin has 2 applications: one is used as a high voltage channel for CCL, and the other is used independently for open-drain output. CCL usually connects to the low voltage PD signal of the MCU's CC pin, and CCH usually connects to the high voltage PD signal of the Type-C interface, with CCM as the intermediate node. Default CC_OE=0, CCH disconnects CCM and CCL. Default CC_GE=0, CCL disconnects CCM and CCM to GND. When CC_OE=1 and CC_GE=0, CCH open-drain outputs low. When CC_OE=1 and CC_GE=1, CCH is connected to CCL and CCM, and CCM outputs CCI after comparing with the high threshold reference voltage V_{TCC}. Default CC_VE=0. If CC_VE=1, VDD49 outputs to CCH as VCONN supply. Default CC_PD=1, if CCPDG is connected to GND, CCH connects to the 5.1K Rd pull-down resistor. Note that there are diodes between CCM and CCH, and between CCM and CCL. If CC_GE=1 and CC_OE=0, CCH is theoretically disconnected, but the above diodes will still transmit a high level signal from CCL to CCH.

Note that there is a voltage regulator of about 10V between the Rd pull-down resistor of 5.1K and GND, which will turn on when the CCH voltage is high.

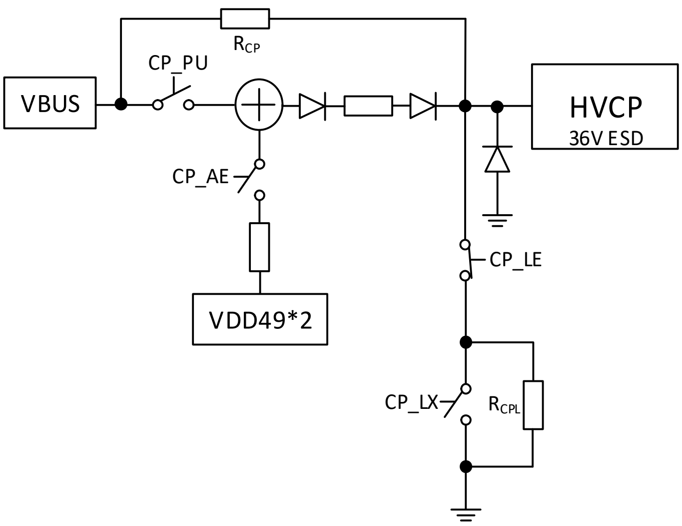
ODH pin has three applications: One is as another high-voltage channel of CCL, the other is as a high-voltage channel of ODL, and the third is for open-drain output independently. Default OD_PE=1, default OD_OE=1, ODH and ODL are connected. By default, OD_GE=0, and ODL is disconnected from CCL. When OD_OE=1, OD_GE=0 and OD_PE=1, ODH and ODL are connected, and ODL can be connected to the CC pin of MCU. When ODL is suspended, OD_OE=1, OD_GE=1 and OD_PE=1, ODH is connected with CCL, and ODH is another high-voltage channel of CCL. When ODL is suspended, OD_OE=1, OD_GE=0 and OD_PE=0, the open-drain output of ODH is low.

The internal resistance of PD signal switch is not large, so overcurrent should be avoided when it is used as an open-drain output, and external series resistance can be used to limit the current if necessary.

5.2. Boost Module

The boost module generates a higher voltage based on VBUS, and the boost voltage VCP is about twice that of VDD49 minus 2.3V, which is used to control the gate of the external N-type MOSFET power tube.

Refer to the figure below for the structure of the booster module.



HVCP pin has 2 applications: One is single-tube control, and the other is 3-tube control. Single-tube control means that HVCP directly controls the gate of external N-tube, which can output low level (Disable N-tube), pull up to VBUS level and boost voltage based on VBUS (Enable N-tube). Three-transistor control means that HVCP is connected with a capacitor of about 100nF to provide a simple boost power supply. Three megohm resistors are respectively connected to the gates of three N-transistors, and at the same time, 3 high-voltage pins, namely ODH1, ODH2 and HVIO, are respectively connected to realize the switching control of the three N-transistors in an open-drain drive mode.

R_{CP} is a built-in discharge resistor, R_{CPL} is a built-in pull-down resistor, and HVCP pin does not need an external pull-down resistor.

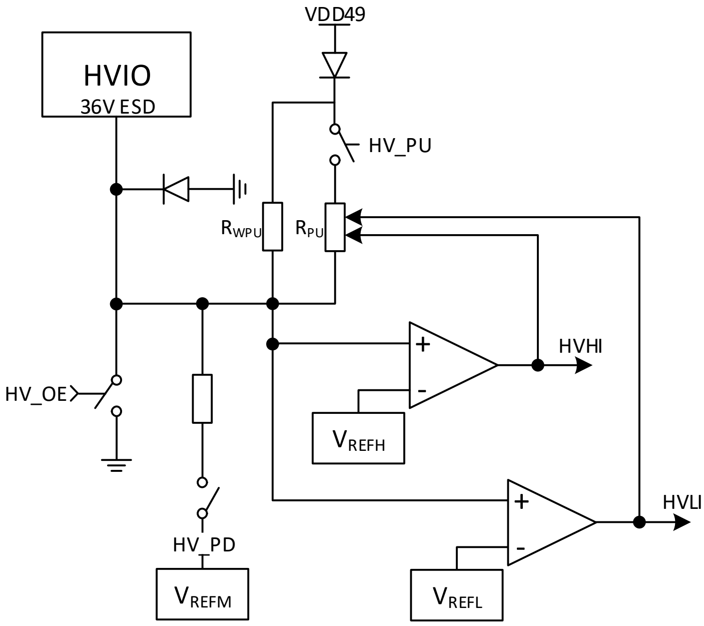
By default, CP_PU=0, CP_AE=0, CP_LX=0, and CP_LE=1. The voltage of HVCP is divided by R_{CP} and R_{CPL}, and the HVCP does not exceed 0.2V when VBUS defaults to 5V, and the external N tube is turned off. After the MCU is powered on, CP_LX=1 can be set to make HVCP output a low level with strong pull-down. After that, if the MCU applies for USB PD high-voltage power supply, HVCP can also maintain a low-voltage to turn off the external N tube. When CP_PU=1, CP_AE=0 and CP_LE=0, the VBUS pull-up is turned on, and the output of HVCP is close to the VBUS voltage, which is attenuated by a resistor and 2 diodes in series. When CP_PU=0, CP_AE=1 and CP_LE=0 (actually this combination is not supported), boost is turned on, and HVCP outputs the net boost voltage V_{CP}. When CP_PU=1, CP_AE=1 and CP_LE=0, turn on VBUS to boost the voltage, and the output voltage of HVCP is VBUS plus the net boost voltage V_{CP}.

HVCP has poor load capacity, and the larger the load current, the smaller the V_{CP} voltage value. It is suggested that N-tube with lower turn-on voltage Vth should be preferred.

5.3. High-voltage I/O

HVIO is a high-voltage general-purpose I/O that supports high-voltage open-drain output and input, and can also be used as an interrupt output. It has a built-in weak pull-up resistor RWPU and a controllable pull-up resistor RPU, and supports power switch key detection and wake-up and P-type MOSFET control.

Refer to the figure below for the structure of HVIO.



The default HV_OE=0, and HVIO open-drain output is prohibited. The default HV_PU=0, the default HV_PD=0, and only the weak pull-up resistor RWPU is provided. When HV_PD=1, the output V_{REFM} of HVIO is weak and low, which supports external P-type MOSFET gate control and key detection. HVHI and HVLI are input samples at high and low thresholds, and the pull-up resistance value is fine-tuned according to the results, and RPU pull-up is provided when HV_PU=1.

When used in HVIO single-pin one-key switch, the internal R_{PU} pull-up resistor or external pull-up resistor is enabled to a higher voltage, the power switch button is connected between HVIO and GND, and HVIO is also used to drive the gate of external P-type MOSFET, and the source of the P-tube is connected to the power supply, and the drain of the P-tube outputs the power supply to the target. Turning off the P-tube requires a high level, and HVIO has a built-in pull-up resistor with a voltage of VDD49, which can directly drive the P-tube to control the power supply with a voltage of 5V or lower. If it is used to control a high-voltage power supply higher than 5V, HVIO needs to connect a pull-up resistor from tens of KΩ to hundreds of KΩ to the high-voltage power supply, and the pull-up current cannot exceed I_{PDK}. For example, the high-voltage power supply is 20V, which is connected to the source of the P tube, and HVIO is connected to the gate of the P-tube, and is connected to the high-voltage power supply through a 100KΩ pull-up resistor.

The following table shows several working states of single-pin one-key switch.

Working state	HV_OE	HV_PU	HV_PD	HVLI	HVHI	HVIO pin	Description
Default on at power-up	0	0	0	0	0	Low charging period	HVIO to GND capacitor
Default off at power-up	0	0	0	1	1	Pull up to high	Optional: HVIO connects a capacitor or resistor to the

							power supply.
Maintain power on and standby.	0	1	1	1	0	Weak low level	MCU sets HV_PD=1 and outputs VREFM to turn on p-tube.
Press the key to connect GND.	0	1	1	0	0	Low level	Query HVLI or interrupt
MCU active shutdown	0	1	0	1	1	Pull up to high	

When HVIO has external pull-up resistor, HV_PU need not be set to 1.

The capacitance value of HVIO to GND depends on the start-up time of MCU, and is also used for key debounce. RWPU, an internal weak pull-up resistor in HVIO, and an optional external pull-up resistor form an RC charging circuit with this capacitor. During charging, the P-tube is kept open until the MCU is started and takes over. Set HV_PD=1 to keep the P-tube open. If the capacitance value is too small, it will cause the MCU to complete charging before taking over and cut off the power supply of the MCU.

The VDD33 of CH211 can be turned off. for the application where the MCU is powered by VDD33, a KEY switch can be realized without external P-type MOSFET, and the keys can be connected by KEY or HVIO.

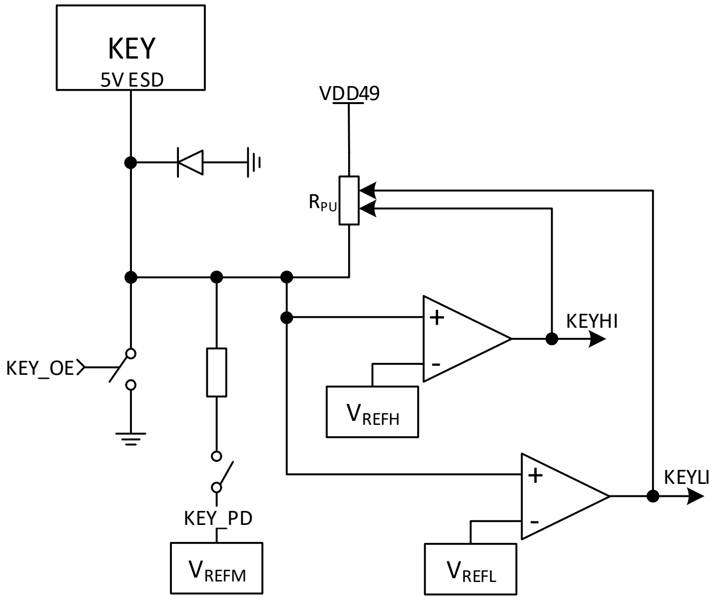
The shutdown state means that the MCU sleeps when VDD33 is turned on, or LDO33_OFF=1 and LDO33_WAKE=1 turns off the VDD33 power supply, and HV_PD=0. When the key is pressed, HVIO is low, which triggers the interruption to restore the power supply of VDD33 and wake up the MCU.

The MCU enters the working state after wake-up, sets HV_PD=1, and the HVIO outputs VREFM weakly low, which is used to drive the external P-type MOSFET to keep the main power supply turned on, while continuing to monitor the keys on the HVIO pin. When the key is pressed, the MCU interrupt is triggered and HV_PD=0 is set; when the key is released, HVIO goes back to high level and turns off the external P-type MOSFET or the MCU sets LDO33_OFF=1.

5.4. Low-voltage I/O

KEY is a low-voltage general-purpose I/O that supports open-drain output and input, and can also be used as an interrupt output. It has a built-in pull-up resistor RPU, which supports power switch key detection and wake-up and low-voltage P-type MOSFET control.

Refer to the figure below for the structure of KEY.



Default KEY_OE=0, KEY open-drain output disabled. Default KEY_PD=0, pull-up only. When KEY_PD=1, KEY outputs VREFM weak low level, which supports gate control of external P-type MOSFET power tubes not exceeding the voltage of VDD49, as well as key detection. KEYHI and KEYLI are high and low sub-threshold inputs to be sampled, and the value of the pull-up resistor is fine-tuned according to its result.

When KEY is used for single-pin one-key switch, it is equivalent to the low-voltage version of HVIO. Refer to HVIO. The difference is that the KEY does not support high-voltage, but can only drive the power supply with P tube controlling 5V or lower voltage, and the KEY usually does not need external pull-up resistor.

5.5. Power System

CH211 has 3 built-in LDO regulators, 2 of which are high-voltage LDOs, which support 2 power inputs and automatic switching, and the other low-voltage LDO output can be adjusted by 3.3V for simple power supply of MCU.

VSYS is a high-voltage power supply input of the system, usually a standing power supply, and its own power consumption is small. It outputs VDD49 power supply, and its load-carrying capacity is slightly weak.

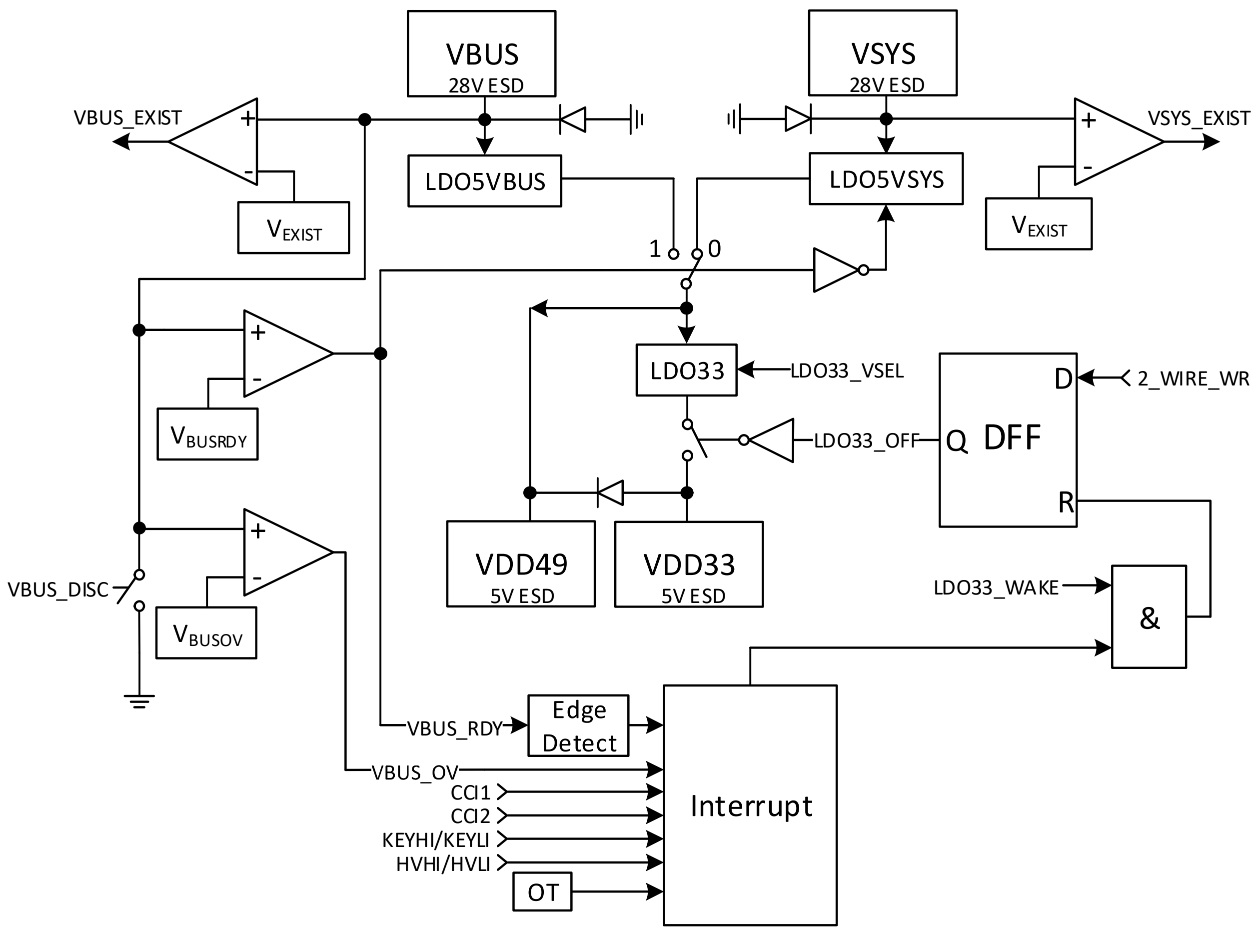
VBUS is an external high-voltage power supply input, usually a Type-C interface VBUS high-voltage power supply input, which supports VBUS discharge and monitoring, including VBUS power-on and power-off monitoring and over-voltage monitoring. After detecting that the VBUS voltage is higher than VBUSRDY, i.e., the VBUS power supply is ready, internally, VDD49 is automatically switched to the VBUS power supply and does not consume current from the VSYS; when the VBUS is powered down, it is then automatically switched back to the VSYS power supply, and interrupts are triggered by either VBUS power-up or power-down.

VSYS and VBUS support rated power supply voltages of 5V, 9V, 12V, 20V, 28V, etc., and external decoupling capacitors of not less than 0.1uF are required. VDD49 needs to place decoupling capacitors in the range of 0.33uF ~ 3.3uF close to VDD49 and GND pins, and the rated output voltage is 4.9V. However, when the input of VSYS or VBUS is lower than 5.1V, the output of VDD49 may be less than 4.9V.

VDD33 is generated from VDD49 by the built-in low-voltage LDO. The default value is 3.3V, and the step is 0.3V. It supports multiple gears from 2.4V to 4.5V. It is used to provide a simple 3.3V power supply of no more than 20mA for MCU, and the decoupling capacitor in the range of 0.1uF~3.3uF is externally connected as required, and no external capacitor is needed when MCU and other peripherals are not powered.

By default, LDO33_OFF=0, the low voltage LDO and VDD33 outputs are on. When LDO33_OFF=1, VDD33 output is off. Default LDO33_WAKE=0. If LDO33_WAKE=1 and LDO33_OFF=1, the VDD33 is in the output off state but can be woken up and turned on by any interrupt to the VDD33, including events such as a power switch keystroke connected by the KEY or HVIO or a VBUS power up or power down.

Refer to the figure below for the structure of power supply system.



5.6. Control and Status Register

There are 8 registers in CH211, which are used for function and pin control and status return. MCU can read and write through 2-wire interface.

The register attributes in the following table use 2 abbreviations: RO means read-only and RW means readable and writable. The register list is as follows:

Name	Address	Description	Reset value
PIN_STAT	0	Pin status register	0Fh
PIN_CFG	1	Pin configuration register	00h
CC_CTRL	2	CC channel control register	44h

OD_CTRL	3	OD channel control register	AAh
HVCP_CTRL	4	HVCP control register	02h
HVIO_KEY	5	HVIO and KEY control registers	00h
SYS_CFG	6	System configuration register	08h
SYS_STAT	7	System status register	01h

Pin Status Register (PIN_STAT):

Bit	Name	Access	Description	Reset value
7	CCI2	RO	CCM2 node level state of PD signal switch 2#, CC2 high threshold level state.	0
6	CCI1	RO	CCM1 node level state of PD signal switch 1#, CC1 high threshold level state.	0
5	VBUS_OV	RO	Over-voltage state of VBUS power supply, with VBUS voltage higher than V_{BUSOV}.	0
4	VBUS_RDY	RO	The VBUS power supply is ready, and the VBUS voltage is higher than V_{BUSRDY}.	0
3	HVHI	RO	High threshold level state of HVIO pin, pin voltage is higher than V_{REFH}.	1
2	HVLI	RO	Low threshold level state of HVIO pin, pin voltage is higher than V_{REFL}.	1
1	KEYHI	RO	High threshold level state of KEY pin, pin voltage is higher than V_{REFH}.	1
0	KEYLI	RO	Low threshold level state of KEY pin, pin voltage is higher than V_{REFL}.	1

Pin Configuration Register (PIN_CFG):

Bit	Name	Access	Description	Reset value
7	CC2_IE	RW	CC2 low-level interrupt is enabled. When it is 0, it prohibits CC2 from triggering interrupts. When it is 1, CC2_GE=1 and CCI2=0, it generates interrupts.	0
6	CC1_IE	RW	CC1 low-level interrupt is enabled, 0 prohibits CC1 from triggering interrupts, and generates interrupts when it is 1 and CC1_GE=1 and CCI1=0.	0
5	HVIO_IE	RW	The low-level interrupt of HVIO pin is enabled. When it is 0, it prohibits HVIO from triggering an interrupt, and when it is 1, HVIL = 0 and HVII = 0, it generates an interrupt.	0
4	KEY_IE	RW	The low-level interrupt of the KEY pin is enabled, 0 prohibits the KEY from triggering the interrupt, and generates an interrupt when it is 1, KEYLI=0 and KEYHI=0.	0
3	VBUS_DOWN _IE	RW	The interruption of VBUS power failure event is enabled, and 0 prohibits VBUS power failure from triggering the interruption. When it is 1 and VBUS_RDY=0 and VBUS_LAST=1, an interrupt is generated. VBUS power-on	0

			event interrupt is always enabled, and an interrupt is generated when VBUS_RDY=1 and VBUS_LAST=0.	
2	SDA_PU	RW	The internal pull-up resistor of SDA pin is enabled. When it is 0, the internal pull-up is prohibited, and when it is 1, the internal pull-up is turned on, which is suitable for weak internal pull-up of MCU pin. If LDO33_WAKE=1 and LDO33_OFF=1, pull-up will be inhibited.	0
1	INT_PIN	RW	Interrupt output pin selection: 00 turns off the interrupt request output; 01 output interrupt request at low level by weak driving of SCL pin, saving pins; 10 Drive low-level output interrupt request through HVIO pin; 11 Drive the low-level output interrupt request through the KEY pin. Continue to request an interrupt unless the cause of the interrupt is eliminated.	0
0		RW		0

CC Channel Control Register (CC_CTRL):

Bit	Name	Access	Description	Reset value
7	CC2_VCE	RW	VCONN power output of CCH2 is enabled, and 0 disables CCH2 power output, and 1 outputs VDD49 to CCH2 pin.	0
6	CC2_PD	RW	The Rd pull-down resistor of CCH2 is enabled, 0 disables the CCH2 pull-down resistor, and 1 turns on the CCH2 pull-down resistor Rd when CCPDG2=GND.	1
5	CC2_OE	RW	Connectivity of CCH2 pin is enabled; if it is 0, CCH2 connectivity is prohibited; if it is 1, CCH2 is connected to the intermediate node CCM2.	0
4	CC2_GE	RW	The connection between the CCL2 pin and the intermediate node CCM2 is enabled. If it is 0, CCM2 will short-circuit GND and disconnect CCL2. If it is 1, CCM2 will disconnect GND and connect CCL2.	0
3	CC1_VCE	RW	VCONN power output of CCH1 is enabled, and 0 disables CCH1 power output, and 1 outputs VDD49 to CCH1 pin.	0
2	CC1_PD	RW	The Rd pull-down resistor of CCH1 is enabled, 0 disables the CCH1 pull-down resistor, and 1 turns on the CCH1 pull-down resistor Rd when CCPDG1=GND.	1
1	CC1_OE	RW	Connectivity of CCH1 pin is enabled; if it is 0, CCH1 connectivity is prohibited; if it is 1, CCH1 is connected to the intermediate node CCM1.	0
0	CC1_GE	RW	It is enabled that the CCL1 pin is connected with the intermediate node CCM1. If it is 0, CCM1 will short-circuit GND and disconnect CCL1. If it is 1, CCM1 will disconnect GND and connect CCL1.	0

OD Channel Control Register (OD_CTRL):

Bit	Name	Access	Description	Reset value
7	OD2_OE	RW	The connectivity of ODH2 pin is enabled. If it is 0, ODH2 connectivity is prohibited, and if it is 1, ODH2 is connected to ODL2.	1
6	OD2_GE	RW	The connection between ODL2 pin and CCL2 is enabled. If it is 0, ODL2 will disconnect CCL2, and if it is 1, ODL2 will connect CCL2.	0
5	OD2_PE	RW	ODL2 disconnect GND is enabled. If it is 0, ODL2 will be shorted to GND, and if it is 1, ODL2 will disconnect GND.	1
4		RO	Reserved	0
3	OD1_OE	RW	Connectivity of ODH1 pin is enabled, 0 disables ODH1 connectivity, and 1 enables ODH1 to ODL1 connectivity.	1
2	OD1_GE	RW	The connection between ODL1 pin and CCL1 is enabled. If it is 0, ODL1 disconnects CCL1, and if it is 1, ODL1 connects CCL1.	0
1	OD1_PE	RW	ODL1 disconnect GND is enabled. If it is 0, ODL1 will be shorted to GND, and if it is 1, ODL1 will disconnect GND.	1
0		RO	Reserved	0

HVCP Control Register (HVCP_CTRL):

Bit	Name	Access	Description	Reset value
7	VBUS_DISC	RW	VBUS discharge is enabled. If it is 0, it will turn off the VBUS discharge, and if it is 1, it will turn on the VBUS discharge. It is recommended not to discharge continuously for a long time.	0
6		RO	Reserved	0
5		RO	Reserved	0
4	CP_AUTO	RW	HVCP automatic boost is enabled, and it is 0 to turn off automatic boost, and 1 to turn on automatic boost. CP_LE should be set to 0.	0
3	CP_AE	RW	HVCP manual boost control, if 0, boost will be completed and idle, if 1, boost will be prepared.	0
2	CP_PU	RW	Manual pull-up output of HVCP pin, 0 turns off the pull-up of HVCP pin, 1 turns on the pull-up of HVCP pin by VBUS, and weakly drives high level.	0
1	CP_LE	RW	Manual pull-down control of HVCP pin: 0 turns off the pull-down of HVCP pin, and 1 turns on the pull-down or low-level driving of HVCP pin.	1
0	CP_LX	RW	HVCP pull-down strength selection: for 0, select weak pull-down and drive low level weakly; for 1, select strong pull-down and drive low level.	0

HVIO and KEY Control Register (HVIO_KEY):

Bit	Name	Access	Description	Reset value
7		RO	Reserved	0
6		RO	Reserved	0
5	KEY_PD	RW	The KEY pin is pulled down to VREFM to enable, 0 turns off the KEY pull-down, and 1 turns the KEY pin down to VREFM, which is between VREFH and VREFL.	0
4	KEY_OE	RW	Open-drain output of KEY pin is enabled. If it is 0, the KEY is prohibited from outputting low level; if it is 1, the KEY outputs low level.	0
3		RO	Reserved	0
2	HV_PU	RW	The HVIO pin pull-up is enabled, which is 0 to turn off the HVIO pull-up, and 1 to pull up the HVIO pin to VDD49 (through a resistor and diode in series).	0
1	HV_PD	RW	The HVIO pin is pulled down to VRFM enabled, 0 turns off the HVIO pull-down, and 1 turns the HVIO pin down to VRFM, between VREFH and VREFL.	0
0	HV_OE	RW	The open-drain output of HVIO pin is enabled. If it is 0, HVIO output is prohibited from being low; if it is 1, HVIO output is low.	0

System Configuration Register (SYS_CFG):

Bit	Name	Access	Description	Reset value
7	LDO33_OFF	RW	VDD33 disable control, turn on the output of VDD33 when it is 0, and turn off the output of VDD33 when it is 1. If LDO33_WAKE=1, it can be automatically cleared by interruption.	0
6	CC_HVT3V	RW	CC high threshold reference voltage V_{TCC} is selected, with 0 for VDD49=4.9V and 1 for VDD49 = 3.3V.	0
5	CPLE_OVOT	RW	Automatic HVCP pull-down is enabled in case of over-voltage and over-temperature; if it is 0, it will not be automatically pulled down; if it is 1, it will force the HVCP pin to pull down or low level during the over-voltage or over-temperature of VBUS, which is equivalent to setting CP_LE to 1.	0
4	RST_OV	RW	Auto-reset is enabled in case of over-voltage; if it is 0, it will not be reset automatically; if it is 1, it will automatically reset CC channel control register CC_CTRL, OD channel control register OD_CTRL and HVCP control register HVCP_CTRL in case of VBUS over-voltage.	0
3	LDO33_WAKE	RW	VDD33 interrupt wake-up is enabled, 0 does not support interrupt wake-up, and 1 supports interrupt wake-up. When an interrupt occurs, LDO33_OFF will be cleared automatically.	1
2	LDO_VSEL	RW	VDD33 voltage selection: 000 select 3.3V; 001 select 3V; 010 select 2.7V; 011 select 2.4V;	0
1		RW		0

0		RW	100 select 3.6V; 101 select 3.9V; 110 select 4.2V; 111 select 4.5V	0

System Status Register (SYS_STAT):

Bit	Name	Access	Description	Reset value
7	LDO33_OFF	RO	VDD33 turns off the control status, with 0 indicating on and 1 indicating off.	0
6	OT_RST	RO	Over-temperature status: 0 indicates that the temperature does not exceed TSD, and 1 indicates over-temperature, which triggers an interrupt and automatically resets CC_CTRL, OD_CTRL and HVCP_CTRL.	0
5	VBUS_OV	RO	Over-voltage status of VBUS power supply, with VBUS voltage higher than V_{BUSOV}.	0
4	VBUS_RDY	RO	Ready status of VBUS power supply, with VBUS voltage is higher than V_{BUSRDY}.	0
3	VBUS_LAST	RO	Record the VBUS power supply ready state when reading SYS_STAT last time. When reading SYS_STAT, this bit is automatically updated to the current power supply state VBUS_RDY.	0
2		RO	Reserved	0
1	VBUS_EXIST	RO	Exist status of VBUS power supply, and the VBUS voltage is higher than V_{EXIST}.	0
0	VSYS_EXIST	RO	Exist status of VSYS power supply, and the VSYS voltage is higher than V_{EXIST}.	1

5.7. 2-wire Serial Interface

CH211 has 8 control and status registers, provides a 2-wire serial interface, including SCL and SDA pins, and is IIC-compatible for MCU control.

SDA is used for serial data input and open-drain output, quasi-bidirectional signal, and requires pull-up resistor, which is high by default. High level means bit data 1, low level means bit data 0, and the sequence of serial data input is high bit first and low bit last.

SCL is used to provide serial clock input, CH211 inputs data from SDA during the high level after its rising edge and outputs data from SDA during the low level after its falling edge.

The falling edge of SDA during SCL high level is defined as the START signal of serial interface, and the rising edge of SDA during SCL high level is defined as the STOP signal of serial interface. When the I/O pin resources of MCU are tight, the SCL pin can also be shared with other interface circuits while keeping the SDA pin status unchanged.

A serial data frame usually contains a START bit, a 7-bit device address, a command bit and an answer bit, 8-bit data and an answer bit and their repetition, and finally ends with a STOP bit. By default, the device address of CH211 is 0x35 or 0x34, which needs to be shifted to the left by one bit and then transmitted as 8-bit data. 0x35 is the address for normal read-write operation of 2-wire interface, and 0x34 is the address for fast read-write operation of 2-wire interface. CH211 supports 0x35 device address writing register operation, 0x35 device address reading register operation and 0x34 device address fast reading register operation.

Steps for a regular write operation:

MCU (Or other host) transmits a START signal;

MCU transmits a 7-bit device address 0x35 and a write command bit 0, and CH211 returns a reply bit 0 when checking the device address matching;

MCU transmits an 8-bit register address (Valid only from 0 to 7), and CH211 records this starting address and returns a reply bit 0;

MCU transmits 8-bit data, and CH211 writes the data into the register, at the same time, the address automatically adds 1 and returns a reply bit 0;

Optionally, MCU can choose to continue transmitting 8-bit data to the next register and wait for CH211 to write and reply;

MCU transmits a STOP signal to end the operation.

Steps for a regular read operation:
MCU (Or other host) transmits a START signal;
MCU transmits a 7-bit device address 0x35 and a write command bit 0, and CH211 returns a reply bit 0 when checking the device address matching;
MCU transmits an 8-bit register address (Valid only from 0 to 7), and CH211 records this starting address and returns a reply bit 0;
The MCU transmits the START signal again;
MCU transmits a 7-bit device address 0x35 and a read command bit 1, and CH211 returns a reply bit 0 when checking the address match;
CH211 reads data from the register and returns, at the same time, the address is automatically increased by 1, and MCU receives 8 bits of data and returns 1 reply bit;
Optionally, MCU can choose to continue reading 8-bit data from the next register and reply;
MCU transmits a STOP signal to end the operation.

Steps for fast read operation:
MCU (Or other host) transmits a START signal;
MCU transmits a 7-bit device address 0x34 and a write command bit 1, and CH211 returns a reply bit 0 when checking the device address matching;
CH211 reads data from the 0 address register PIN_STAT and returns, the address is automatically incremented by 1, and the MCU receives the data and returns a reply;
Optionally, MCU can choose to continue reading 8-bit data from the next register and reply;
MCU transmits a STOP signal to end the operation.
The internal pull-up of MCU pin is usually weak, and the rising edge of SDA is slow. In order to improve the communication speed of 2-wire interface, SDA_PU=1 can be set to enable the internal SDA pull-up resistor of CH211. Under the power supply of VDD33, the pull-up will be automatically turned off when power is turned off, and it will be automatically restored when power is turned on.

5.8. Interrupt

CH211 supports 8 interrupt signal sources, including HVIO pin low level, KEY pin low level, CC1 low level, CC2 low level, VBUS power-on, VBUS power-off, VBUS over-voltage and over-temperature. Among them, VBUS power-on, VBUS over-voltage and over-temperature always enable interrupts, and other signal sources need to turn on the corresponding interrupt enable bits.

CH211 will always request an interrupt unless the cause of the interrupt is eliminated. For the power-on and power-off events of VBUS, VBUS_LAST will be automatically updated after reading SYS_STAT, thus eliminating the interrupt reason and canceling the interrupt request. However, other interrupts, such as VBUS over-voltage, will not cancel the interrupt request until VBUS is no longer over-voltage.

CH211 can choose three interrupt output modes, which are selected by INT_PIN. Among them, it is a conventional way to output low-level request interrupts through HVIO or KEY pins, and I/O pins can be saved by weakly driving low-level request interrupts through SCL pins.

The SCL pin of CH211 supports weak driving low level, which is stronger than the pull-up driving current of ordinary MCU pin, but weaker than the push-pull driving current of ordinary MCU pin.

In idle state, the SCL pin of MCU is set to no output, and at the same time, the pull-up resistor or pull-up current of SCL pin inside MCU is enabled, which usually does not exceed 200uA. If CH211 requests an interrupt, the SCL pin of CH211 will output a weak drive low level, which can pull the SCL signal line to a low level, which can trigger MCU interrupt.

In the communication state of 2-wire interface, MCU turns off the low-level interrupt input function of SCL pin and sets SCL pin as push-pull output. Usually, its high-level driving current exceeds 2mA, far exceeding the low-level driving current of SCL pin of CH211, which can ensure the normal communication of SCL signal line. After the communication, MCU turns on the low-level interrupt input function of SCL pin.

The reuse of SCL pin for interrupt request can save one pin for MCU and CH211 respectively. The related program flow of MCU is as follows.

MCU main program initialization process	MCU communication interface subroutine flow	Interrupt program flow
Enable the internal pull-up resistor of SCL pin; Clear the interrupt flag of SCL pin; Initialize SCL pin as interrupt input (Active low); Wait for an interrupt.	Temporarily disable SCL pin interrupt, IE = 0; Set SCL=1 and push-pull output; Set SDA=1 and output; Transmit the START signal of 2-wire interface normally; Normal 2-wire interface serial data communication; Transmit the STOP signal of 2-wire interface normally; Change SCL from push-pull output to input with pull-up; Clear the interrupt flag of SCL pin; Restore the interrupt enable of SCL pin, IE = 1; 2-wire interface subroutine returns.	Handle interrupts; Clear interrupt cause; Interrupt and exit.

5.9. VBUS Voltage Monitoring

CH211 has built-in over-voltage monitoring module, which continuously monitors the voltage of VBUS. When the voltage of VBUS power supply is higher than V_{BUSOV}, it will trigger an interrupt or optionally reset, and automatically force the HVCP pin to pull down or low level, which is equivalent to turning off the HVCP to boost the voltage.

CH211 has a built-in VBUS voltage monitoring module. When the VBUS power supply voltage is higher than VBUSRDY, it triggers an interrupt and automatically switches to VBUS power supply, and the system no longer consumes VSYS current; when the VBUS power supply voltage is lower than VBUSRDY, it optionally triggers an interrupt and automatically switches to VSYS power supply.

In addition, the VBUS power supply voltage is also compared with the lower voltage threshold V_{EXIST}, and VBUS_EXIST is generated.

5.10. Over-temperature Monitoring OTP

CH211 has a built-in temperature monitoring module. When the temperature of the chip reaches the over-temperature protection point T_{SD}, it will trigger an over-temperature interrupt or optionally reset, and automatically force the HVCP pin to pull down or low level, which is equivalent to turning off the HVCP to boost the voltage.

6. Parameters

6.1. Absolute Maximum Ratings

Stresses at or above the absolute maximum ratings listed in the table below may cause permanent damage to the device.

Name	Parameter description		Min.	Max.	Unit
T_A	Ambient temperature during operation		-40	85	℃
T_J	Operating junction temperature		-40	125	℃
T_S	Ambient temperature during storage		-55	150	℃
V_{SYS}	Supply voltage of VSYS pin		-0.4	32	V
V_{BUS}	Supply voltage of VBUS pin		-0.4	32	V
V_{DD49}	Supply voltage of VDD49 pin		-0.4	6.5	V
V_{DD33}	Supply voltage of VDD33 pin		-0.4	VDD49+0.4	V
V_{CCH}	Signal voltage of CCH1/CCH2 pin		-0.4	32	V
V_{ODH}	Signal voltage of ODH1/ODH2/HVIO pins		-0.4	40	V
V_{LVIO}	Signal voltages of other pins such as SCL/SDA/CCL/ODL/KEY/CCPDG.		-0.4	6.5	V
V_{ESDCC}	HBM model ESD tolerant voltage of CCH/VBUS pin		6		KV
V_{ESDHV}	HBM ESD tolerant voltage of ODH/HVIO/HVCP/VSYS pins		2		KV
V_{ESDNO}	HBM model ESD tolerant voltage of CCPDG pins		0.8		KV
V_{ESDLV}	HBM model ESD tolerant voltage of SCL/SDA/CCL/ODL/KEY/VDD pin		2		KV
I_{IO1}	Continuous conduction current of a single I/O pin			30	mA
I_{IO8}	Pulse current with a duty cycle of less than 1/8 of a single I/O pin			100	mA
I_{ALL}	Total current of all I/O pins			150	mA
PD	Maximum power consumption of the whole chip	QFN20_3×3		500	mW
		QFN16C_2×2		350	mW
θ_{JA}	Packaging thermal resistance	QFN20_3×3	100		℃/W
		QFN16C_2×2	150		℃/W

6.2. Electrical Characteristics

(Test conditions: T_A=25℃, V_{SYS}=5~28V and V_{BUS}=5~28V.)

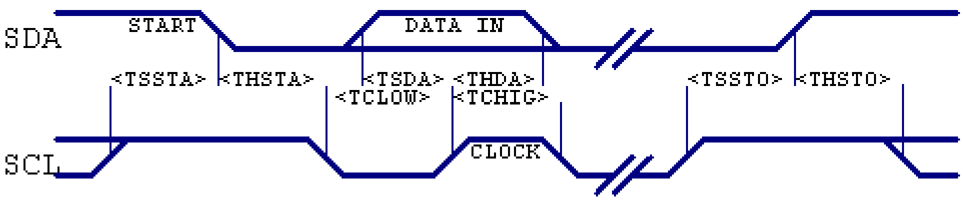
Symbol	Parameter description		Min.	Typ.	Max.	Unit
V_{SYS}	Supply voltage of VSYS pin		2.8	5~28	29	V
V_{BUS}	Supply voltage of VBUS pin		4.7	5~28	29	V
V_{DD49}	VDD49 pin LDO output voltage	V_{SYS} or V_{BUS}>=5.2V, 10mA load	4.7	4.9	5.1	V
		V_{SYS}=5V and V_{BUS}=0V, 10mA load	4.6	4.8	5.0	V
V_{DD33}	Power voltage of VDD33 pin LDO output, 10mA load		V-0.1	2.4~4.5	V+0.1	V

I_{VDD49}	VDD49 and VDD33 add up the output load current, including VCONN.	V_{SYS}>=5V and V_{BUS}<3V			15	mA
		V_{BUS}>=5V			35	mA
I_{VDD33}	VDD33 output load current	V_{BUS}>=5V			20	mA
I_{VCONN}	CCH pin VCONN load current				25	mA
V_{EXIST}	Voltage threshold of power supply with 0.3V hysteresis.		2.8	3~3.3	3.5	V
V_{BUSRDY}	Voltage threshold of VBUS power supply ready	Voltage threshold when VBUS rises	4.2	4.4	4.6	V
		Voltage threshold when VBUS falls	4.0	4.2	4.4	V
V_{BUSOV}	Voltage threshold of VBUS over-voltage monitoring OVP		31.5	33	34.5	V
I_{W}	Operating current when HVCP is turned on but there is no load			0.8	2	mA
I_{QS}	V_{SYS} static current; Idle state with HVCP off	V_{SYS}>=5V and V_{BUS}<3V		15	40	uA
		V_{BUS}>=5V		1	10	uA
I_{QB}	V_{BUS} static current; Idle state with HVCP off	V_{BUS}>=5V		40	100	uA
V_{IL}	Low level input voltage of SCL/SDA pin		0		0.8	V
V_{IH}	High level input voltage of SCL/SDA pin		2.1		5	V
V_{REFL}	Low reference voltage at HVIO/KEY pin with 0.1V hysteresis.		0.9	1.1	1.35	V
V_{REFM}	The middle reference voltage of HVIO/KEY pin is related to the load.		1.35	1.6	2.5	V
V_{REFH}	High reference voltage at HVIO/KEY pin with 0.1V hysteresis.		3.2	3.5	3.8	V
V_{TCC}	High threshold reference voltage of CC with 0.1V hysteresis	V_{DD49}=4.9V, CC_HVT3V=0	2.1	2.4	2.8	V
		V_{DD49}=3.3V, CC_HVT3V=1	2.1	2.3	2.5	V
V_{CP}	CP_AUTO=1 Wait for the stabilized net boost voltage.	Load current<=10uA	5	7.4	8	V
I_{OLSDA}	Low-level sinking current of SDA pin	SDA=0.4V	5	10	16	mA
I_{OLSCL}	Low-level sinking current of SCL pin (SCL is reused for interrupt output)	SCL=0.4V	0.18	0.3	0.5	mA
		SCL=V_{DD49}		1.3	2.0	mA
I_{PDK}	Pull-down load current of HVIO/KEY pin to V_{REFM}				800	uA
$I_{VBUSDISC}$	Discharge current VBUS pin	V_{BUS}=5V		25		mA
		V_{BUS}=28V		30		mA
I_{CP}	Load current of HVCP rising voltage module				60	uA
I_{CPX}	Load current of HVCP strong	HVCP=0.5V	400	700	1200	uA

	pull-down	HVCP=28V		6		mA
I_{CPL}	Load current of HVCP weak pull-down	HVCP=3V ~ 28V	60	100	140	uA
R_{PUSDA}	Built-in pull-up resistor of SDA pin		7	10	15	KΩ
R_d	Built-in Rd pull-down resistor of CCH pin	V_{CCH}>=1.2V	4.2	5.1	6	KΩ
R_{GCC}	CC channel on-resistance	V_{CCH}<=1.2V		14	20	Ω
R_{GOD}	OD channel on-resistance	V_{ODH}<=1.2V		32	45	Ω
R_{WPU}	HVIO built-in weak pull-up resistor		4000	8000	15000	KΩ
R_{PU}	HVIO/KEY built-in pull-up resistor	HV_PD/KEY_PD=0	30	60	180	KΩ
		HV_PD/KEY_PD=1	80	160	400	KΩ
R_{CP}	HVCP built-in discharge resistor		800	1200	1600	KΩ
R_{CPL}	HVCP weak pull-down series resistance		25	40	60	KΩ
T_{SD}	OTP over-temperature monitoring threshold		115	135	160	℃
V_{LVR}	Voltage thresholds for power-on reset and low-voltage reset		2.0	2.2	2.5	V

6.3. Interface Timing Parameter

(Test conditions: T_A=25℃, V_{SYS}=5~28V. Refer to the attached drawings.)



Symbol	Parameter description	Min.	Typ.	Max.	Unit
T_{SSTA}	Setup time of SDA falling edge start signal	90			nS
T_{HSTA}	Holding time of SDA falling edge start signal	90			nS
T_{SSTO}	Setup time of SDA rising edge stop signal	90			nS
T_{HSTO}	Holding time of SDA rising edge stop signal	90			nS
T_{CLOW}	Low level width of SCL clock signal	90			nS
T_{CHIG}	High level width of SCL clock signal	90			nS
T_{SDA}	Setup time of rising edge of SCL by SDA input data	30			nS
T_{HDA}	Holding time of rising edge of SCL by SDA input data	10			nS
Rate	Average data transmission rate	0		2M	bps

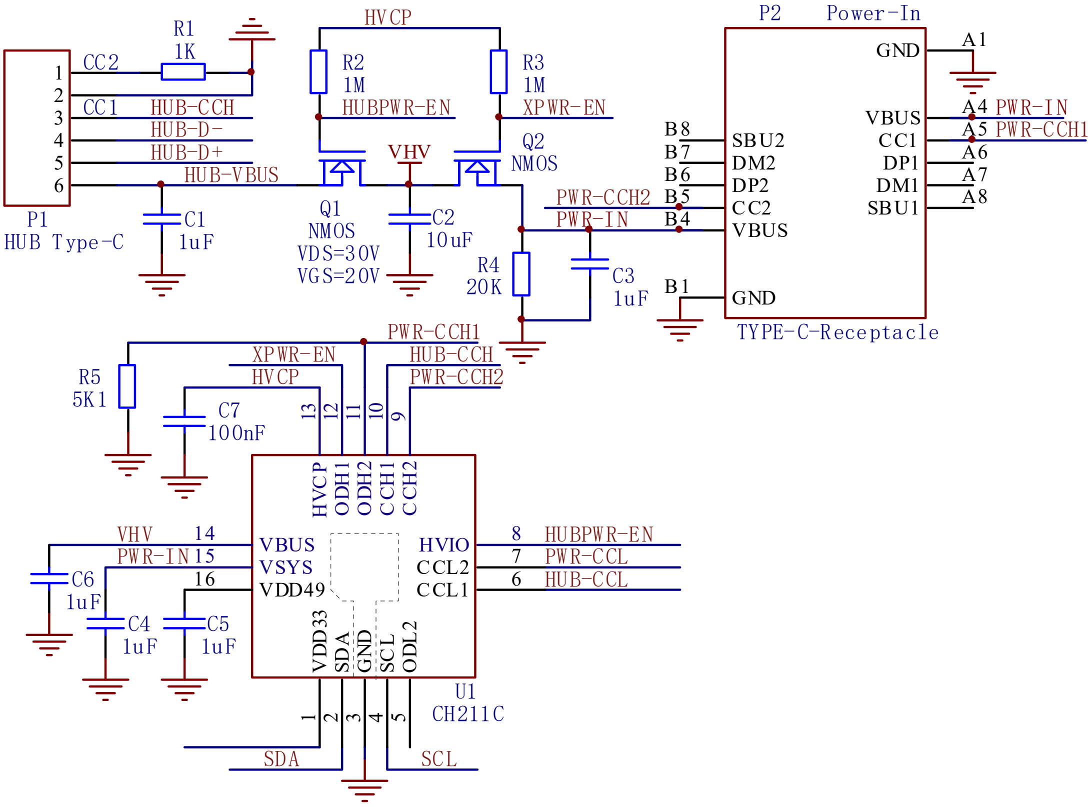
7. Applications

7.1. PD-HUB High-voltage Expansion

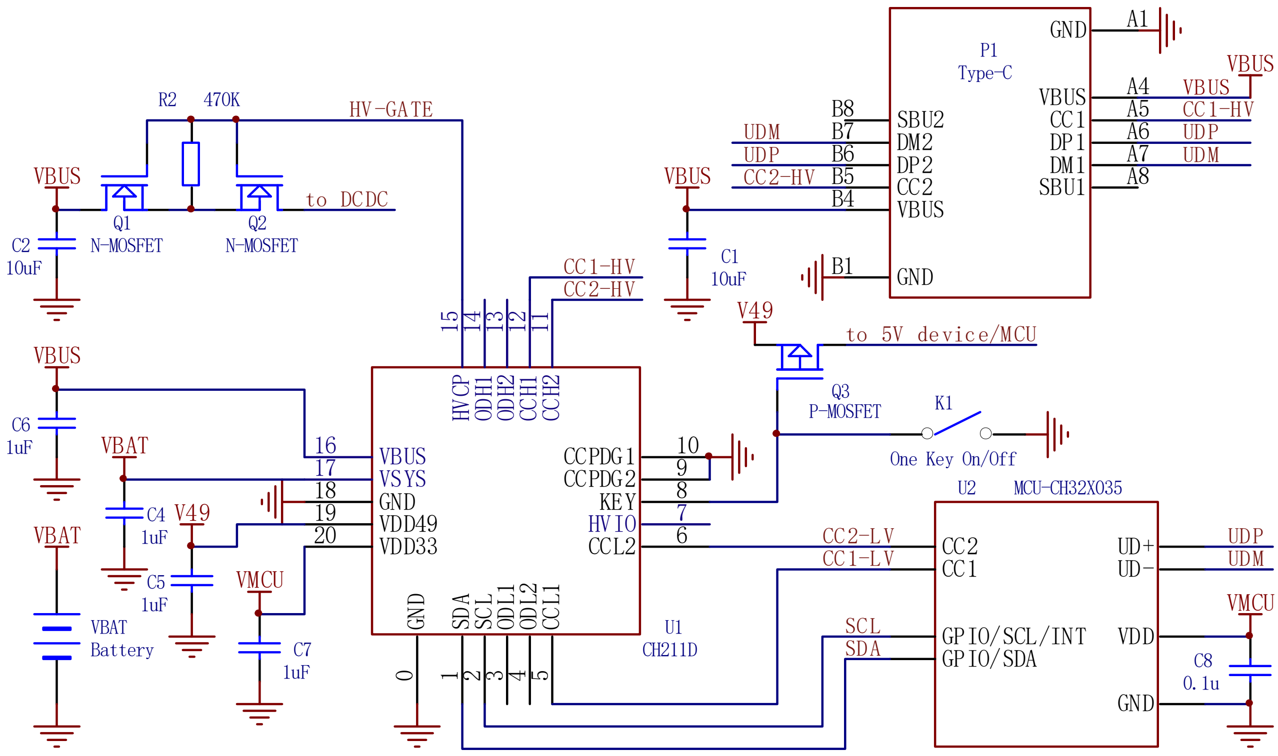
The HUB chip (Such as CH634 or CH339) with built-in PD controls CH211 via SCL and SDA. One of the 2 CCs serves as PWR_CCL, which connects to the Type-C power port P2 2 CC pins for two-way selection via CH211, and the other serves as HUB_CCL, which connects to the HUB port P1, which connects to the USB host and is the USB communication port, via CH211.

CH211C has built-in 5K1 pull-down resistors for CCH1 and CCH2, and an additional pull-down resistor is required for ODH2. In this circuit, VSYS is only used to detect whether Type-C powered port P2 is powered or not.

The HVCP of CH211 can boost VHV, connect to the gates of 2 N-type MOSFET power tubes Q1 and Q2 through 2 pull-up resistors, and independently turn on or off the 2 N-tubes under the control of 2 high-voltage open-drain pins of CH211. If you do not boost, you can also use 2 high-voltage open-drain pins and 2 pull-up resistors connected to the VHV independently control the 2 P-tubes to achieve the same function. the difference between the P-tubes and the N-tubes is that the P-tubes conduction resistance is slightly larger under the same conditions, or slightly higher cost.



7.2 One-touch Switch with DRP



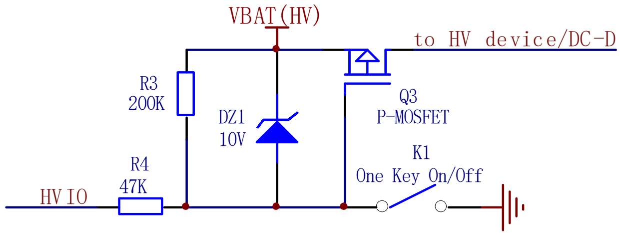
The CH211 provides Type-C Rd pull-down resistors for PDUSB MCUs (e.g. CH32X035 or CH32L103) that support PD Source, Sink, and DRP, and the HVCP pin generates a high voltage that can be used to control the DCDC on/off, charging the battery, or reversing the output. If it is used for Source only, then the 2 CCPDG pins should be dangling, and the VBUS pin of CH211 does not need to be connected.

The MCU connects to the CH211 through a 2-wire interface, and SCL is also used for interrupts to realize I/O expansion or high-voltage open-drain I/O drive. The Type-C signal after high voltage expansion by CH211 can directly tolerant the accidental high voltage contact of the adjacent high voltage pin VBUS on port C, thus protecting the CC pin of the MCU.

If the voltage at the VSYS pin is much higher than the output voltage of the DCDC, then the output power of the DCDC can be sent to the VBUS pin of the CH211 instead of the VSYS power supply, thus reducing the LDO power consumption of the CH211.

In order to reduce the VBAT battery standby power consumption, the MCU can be in a power-off state during idle time, and a one-touch switch is realized by a single button K1. after K1 is pressed, CH211 wakes up, the MCU obtains the VDD33 power supply of CH211 (or V49 or other 5V power supply controlled by Q3), and the MCU sets the KEY pin of CH211 to output a weak low level to maintain Q3 on; when the MCU is idle for a long time, or the MCU outputs VBUS pin to replace VSYS power supply, the LDO power consumption of CH211 can be reduced. When the MCU is idle for a long time, or the MCU detects that K1 is pressed again or K1 is pressed for a long time, the VDD33 is set to be turned off (or the KEY pin is set to turn off Q3) and CH211 waits for K1 to wake up. The P-tube Q3 in the above diagram is optional, and Q3 is not needed if the MCU uses the CH211's controllable VDD33 power supply.

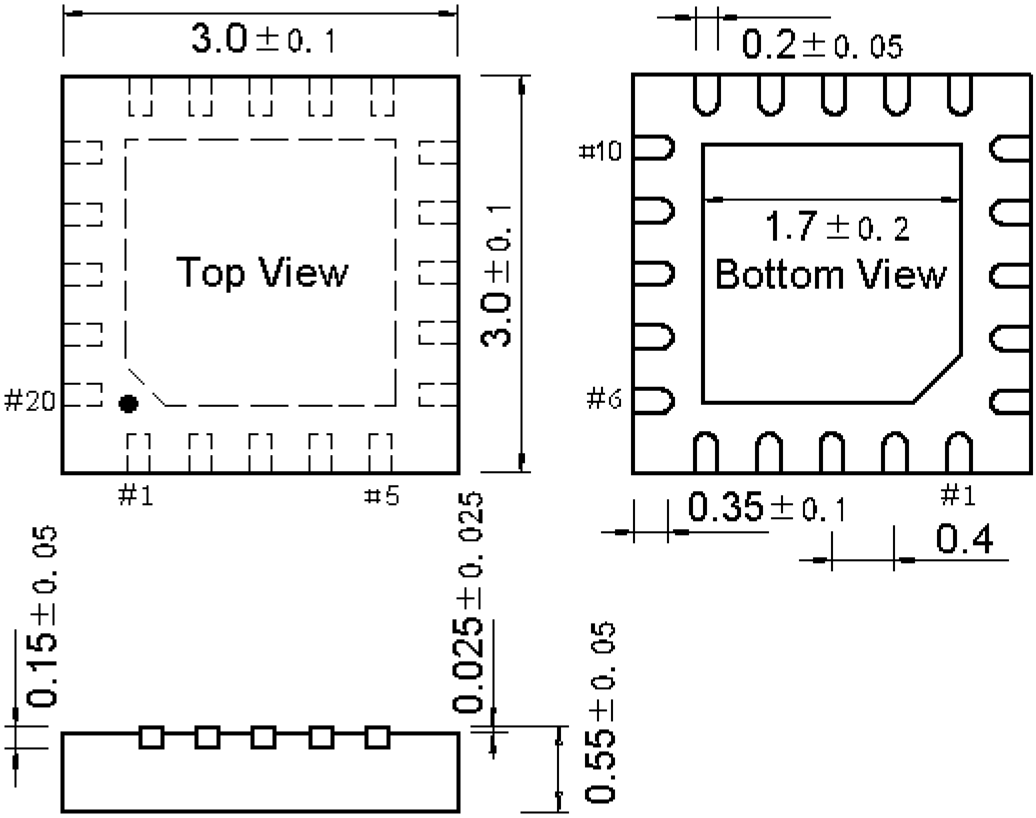
If you need to control a high voltage power supply that exceeds 5V, then refer to the following diagram and change K1 and Q3 from the KEY pin to the HVIO pin and add pull-up resistor R3 between the gate and source of Q3. regulator DZ1 and current limiting resistor R4 are optional and are only used to protect the Q3 gate if the high voltage supply voltage exceeds the Q3 gate source tolerant voltage.



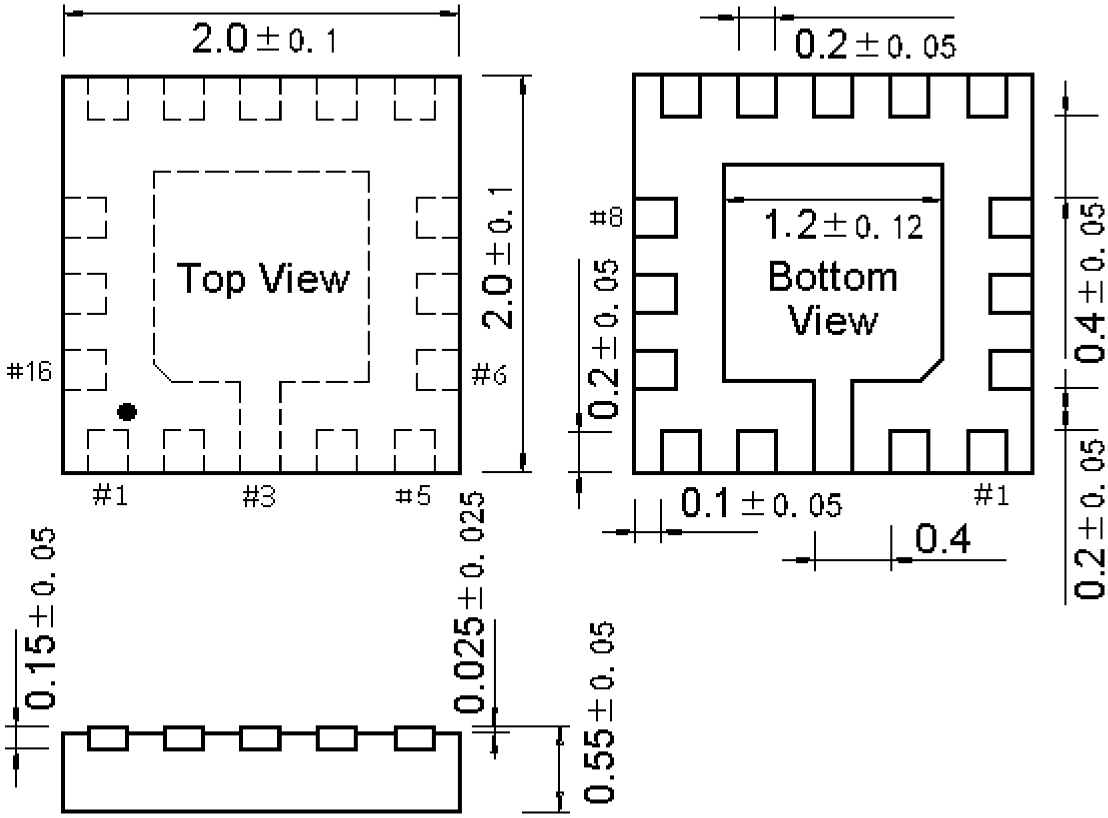
8. Package Information

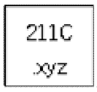
All dimensions are in mm, and the packaging error of QFN is less than ±0.1, and the packaging error of non-QFN is less than ±0.2.

8.1. QFN20_3×3×0.55-0.4



8.2. QFN16C_2×2×0.55-0.4



CH211C printed as follows 

, where xyz is the lot number code, and "."corresponds to pin 1#.