4-port USB3.0 HUB Controller Chip CH634

Datasheet 1

Version: V1.3

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1. Overview

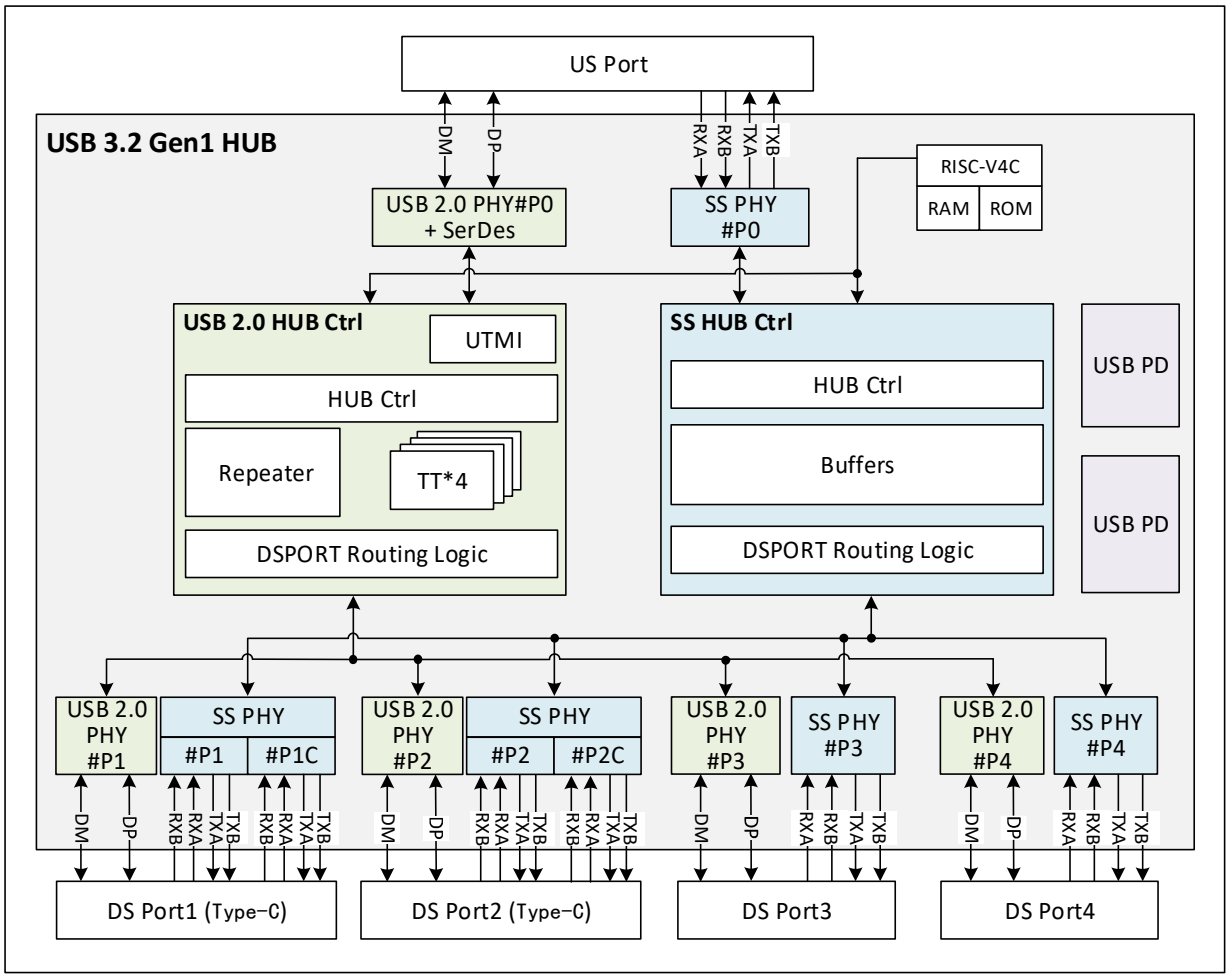
CH634 is a 4-port USB ultra-high-speed HUB controller chip conforming to the USB3.2 Gen1 protocol specification, and the single chip integrates the functions of 4-port USB HUB and USB PD. CH634 has independent SS HUB controller and USB2.0 HUB controller, and has built-in 5 sets of SS PHY, 5 sets of USB2.0 PHY and 2 sets of PD PHY. The upstream port of CH634 chip supports USB3.0 ultra-high speed 5Gbps, USB2.0 high-speed 480Mbps and full-speed 12Mbps, and the downstream port supports USB3.0 ultra-high-speed, USB2.0 high-speed, full-speed and low-speed 1.5Mbps.

CH634W8G has 2 built-in Type-C dual-channel USB3.0 PHYs and dual PD PHYs, compatible with USB-C cables and connection specifications, native support for Type-C forward and reverse plugging adaptive, native support for PDHUB and Type-C power 15W fast charging.

CH634 supports high-performance concurrent processing MTT mode, adopts industrial-grade design, and the periphery is simplified, which can be applied to computer and industrial computer motherboards, docking stations, peripherals, embedded systems and other scenarios.

The following figure shows the system block diagram of CH634.

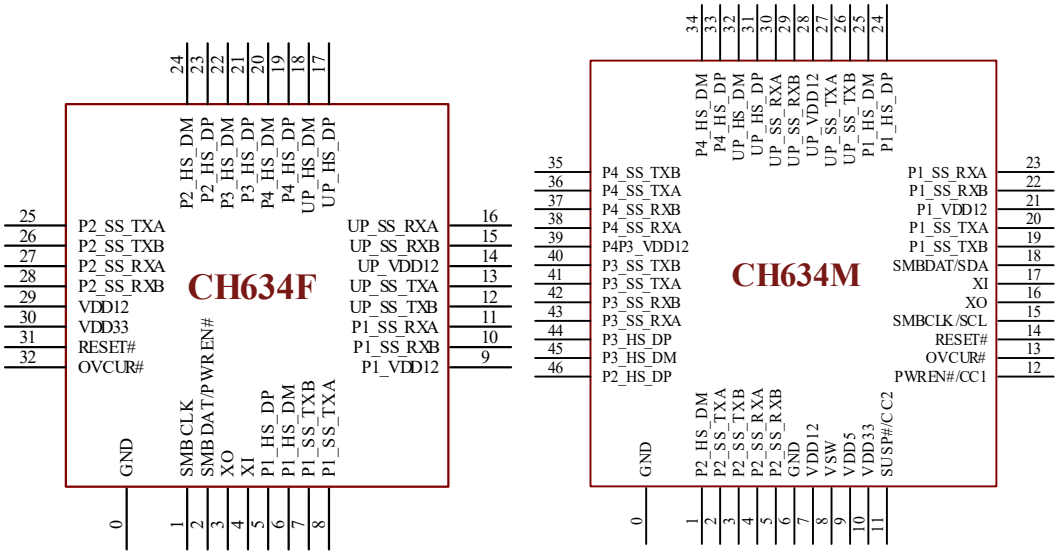
Figure 1-1 System block diagram

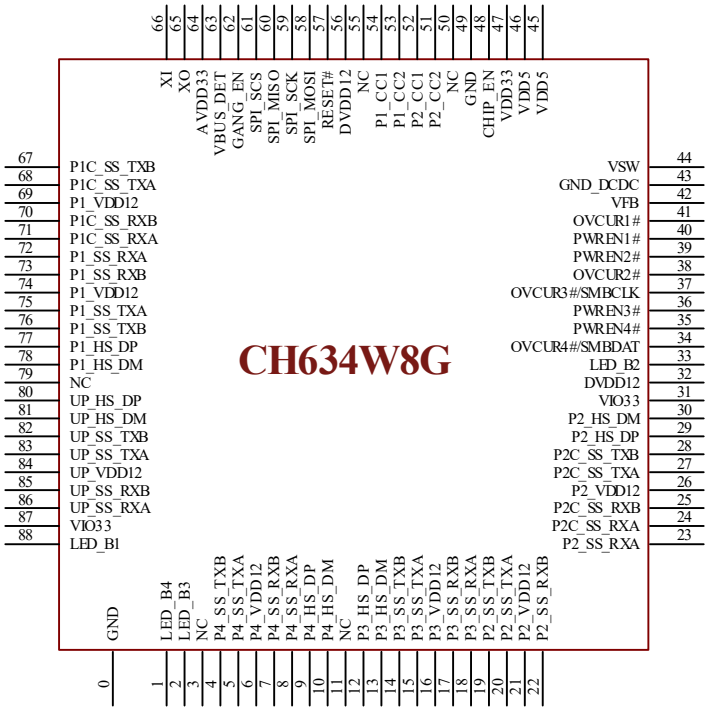


2. Feature

- 4-port USB3.2 Gen1 HUB, providing 4 downstream ports, supporting USB3.2 Gen1(5Gbps), and accommodating USB3.1, USB3.0, USB2.1, USB2.0, USB1.1 and USB1.0 forward.
- USB3.2 Gen1 HUB module supports U0/U1/U2/U3 power management mode conforming to USB 3.2gen1 protocol specification.
- Some models have built-in 2 sets of self-developed Type-C dual-channel USB3.0 PHY, which native support for Type-C forward insertion and reverse insertion.
- USB2.0 HUB module supports L0/L1/L2/L3 power management mode conforming to USB2.1 protocol specification.
- Support low-cost STT or high-performance MTT mode, and MTT configures independent TT for each port to realize high-speed transmission.
- Built-in 2 USB PD PHY, native support for 15W fast charging of Type-C power supply, support for PDHUB and docking station.
- Support BC1.2 charging protocol and CDP.
- Compatible with USB Type-C cable and connection specification, 3 C-port working modes, and support for downstream double C-port or upstream C-port.
- Support GANG integrated linkage power supply control and GANG integrated overcurrent detection
- Some models support independent power control of each port and independent overcurrent detection of each port.
- Self-developed USBPHY for HUB, low-power technology, supporting self-power supply or bus power supply.
- Some models support SMBus bus and support motherboard integration and management.
- CH634M and CH634W8G support upstream port exchange function, which is convenient for 2 USB hosts to manage multiple USB devices.
- Support independent or integral control, power supply mode and other functions through I/O pin configuration
- The external EEPROM, external FLASH or internal EEPROM can be used to configure whether the HUB chip supports composite devices, non-removable devices, custom VID, PID, port configuration, USB vendor, product, serial number string descriptor, etc.
- Built-in information memory, which can customize the information and configuration of manufacturers or products in lots according to the special needs of the industry
- It integrates a 3.3V LDO voltage regulator and a 1.2V DC-DC buck, supports external 5V power supply, and simplifies the periphery.
- Some models support adding Type-C interface chip CH211 to realize 28V high-voltage PDHUB and docking station.
- QingKe RISC-V processor core, controllers such as overspeed USB, high-speed USB and USBPD, and the IP of the physical layer transceiver are all self-researched, and all modules are closely coordinated, with high efficiency and low cost, and the IP licensing fee is exempted.
- Provide QFN32, QFN46C5, QFN88 and other packaging forms.

3. Pinouts





Package Form	Body Size	Pin Pitch		Package description	Order Model
QFN32	4*4mm	0.4mm	15.7mil	Quad Flat No-Lead Package	CH634F
QFN46C5	5*5mm	0.4mm	15.7mil	Quad Flat No-Lead Package	CH634M
QFN88	10*10mm	0.4mm	15.7mil	Quad Flat No-Lead Package	CH634W8G

Note: 1. Pin 0# is the EPAD of QFN package and is a necessary connection.

2. CH634F, CH634W5M and CH634W6T have no LDO voltage regulator and DC-DC step-down, and need external power supply of 3.3V and 1.2V at the same time. Other models have built-in 3.3V LDO voltage regulator and 1.2V DC-DC buck, and external single power supply is 5V or 3.3V.

3. The 4 downstream ports of CH634F include 2 USB3.2 Gen1 and 2 USB2.0; Other models include 4 USB3.2 Gen1 downstream ports and 4 USB2.0; Among them, CH634W8G contains 2 sets of native Type-C/PD forward and backward insertion adaptive ports.

4. Custom pins CH634W5M, CH634W6C, CH634W6G, CH634W6T, CH634W7G, CH634W7R, CH634W7S, CH634W7U, CH634W7V are only reserved in lots. For the pin arrangement, pin definition and package information, please refer to the CH634DS2 manual.

4. Pin Definitions

Table 4-1 USB signal related pin function description

USB signal pin	Pin name	Type(1)	Function description
Upstream port USBSS differential signal	UP_SS_TXA UP_SS_TXB	USB3	Upstream port USBSS differential transmission signal line TX+/TX- or TX-/TX+ (automatic cross identification).
	UP_SS_RXA UP_SS_RXB	USB3	Upstream port USBSS differential receiving signal line RX+/RX- or RX-/RX+ (automatic cross identification).
Upstream port USB2.0 differential signal	UP_HS_DP	USB2	Upstream port USB2.0 differential signal D+。
	UP_HS_DM	USB2	Upstream port USB2.0 differential signal D-。
1#downstream port USBSS differential signal	P1_SS_TXA P1_SS_TXB	USB3	1#Downstream port USBSS differential transmission signal line TX+/TX- or TX-/TX+ (automatic cross identification).
	P1_SS_RXA P1_SS_RXB	USB3	1# Downstream port USBSS differential receiving signal line RX+/RX- or RX-/RX+ (automatic cross identification).
1# downstream port USB2.0 differential signal	P1_HS_DP	USB2	1# Downstream port USB2.0 differential signal D+.
	P1_HS_DM	USB2	1# Downstream port USB2.0 differential signal D-。
2# downstream port USBSS differential signal	P2_SS_TXA P2_SS_TXB	USB3	2# Downstream port USBSS differential transmission signal line TX+/TX- or TX-/TX+ (automatic cross identification).
	P2_SS_RXA P2_SS_RXB	USB3	2# Downstream port USBSS differential receiving signal line RX+/RX- or RX-/RX+ (automatic cross identification).
2# downstream port USB2.0 differential signal	P2_HS_DP	USB2	2# Downstream port USB2.0 differential signal D+.
	P2_HS_DM	USB2	2# Downstream port USB2.0 differential signal D-.
3# downstream port USBSS differential signal	P3_SS_TXA P3_SS_TXB	USB3	3# Downstream port USBSS differential transmission signal line TX+/TX- or TX-/TX+ (automatic cross identification).
	P3_SS_RXA P3_SS_RXB	USB3	3# Downstream port USBSS differential receiving signal line RX+/RX- or RX-/RX+ (automatic cross identification).
3# downstream port USB2.0 differential signal	P3_HS_DP	USB2	3# Downstream port USB2.0 differential signal line D+。
	P3_HS_DM	USB2	3# Downstream port USB2.0 differential signal line D-。
4# downstream port USBSS differential signal	P4_SS_TXA P4_SS_TXB	USB3	4# Downstream port USBSS differential transmission signal line TX+/TX- or TX-/TX+ (automatic cross identification).
	P4_SS_RXA P4_SS_RXB	USB3	4# Downstream port USBSS differential receiving signal line RX+/RX- or RX-/RX+(automatic cross identification).
4# downstream port USB2.0 differential signal	P4_HS_DP	USB2	4# Downstream port USB2.0 differential signal line D+.
	P4_HS_DM	USB2	4# Downstream port USB2.0 differential signal line D-.

1# or 2# downstream port Type-C differential signal	PxC_SS_TXA PxC_SS_TXB	USB3	1# or 2# Downstream port Type-C differential signal line TX+/TX- or TX-/TX+ (automatic cross identification).
	PxC_SS_RXA PxC_SS_RXB	USB3	1# or 2# Downstream port Type-C differential signal line RX+/RX- or RX-/RX+ (automatic cross identification).

Table 4-2 CH634F and CH634M pin definitions

Pin No. (Pin with the same name can be referenced)		Pin name	Type(1)	Function description
CH634F	CH634M			
-	9	VDD5	P	5V power input, it is recommended to connect 0.1uF parallel 10uF decoupling capacitor. If the voltage of VDD5 is less than 3.6V, it should be shorted to VDD33.
-	8	VSW	P	DCDC output, need to be close to the pin series inductor to generate 1.2V power supply, and 1.2V power supply needs to be placed close to the ground capacitance, it is recommended to use a 2.2uH inductor and at least one 10uF capacitor.
-	10	VDD33	P	3.3V LDO output terminal, analog power supply and I/O pin power supply input, it is recommended to connect 0.1uF parallel 10uF decoupling capacitor.
30	-	VDD33	P	Analog power supply and I/O pin power supply input, it is recommended to connect 0.1uF parallel 10uF decoupling capacitor.
29	7	VDD12	P	1.2V core power supply and 1.2V power supply input of 2# downstream port, it is proposed to connect 0.1uF or 1uF decoupling capacitor externally.
0	0/6	GND	P	Common ground terminal, must be connected to GND.
14	28	UP_VDD12	P	Upstream port 1.2V power input, external 0.1uF decoupling capacitor
9	21	P1_VDD12	P	1#Downstream port 1.2V power input, external 0.1uF decoupling capacitor
-	-	P3_VDD12	P	3#Downstream port 1.2V power input, external 0.1uF decoupling capacitor
-	39	P4P3_VDD12	P	3# and 4# Downstream port 1.2V power input, external 0.1uF decoupling capacitor
4	17	XI	I	The input terminal of crystal oscillator is connected with one terminal of external 24MHz crystal and capacitor to ground.
3	16	XO	O	The inverted output terminal of the crystal oscillator is connected to the other terminal of the external 24MHz crystal and the capacitor to ground.
13/12/16/15	27/26/30/29	UP_SS_xxx	USB3	Upstream port USBSS differential transmit or receive signal line.

17/18	31/32	UP_HS_xx	USB2	Upstream port USB2.0 differential signal line.
8/7/11/10	20/19/23/22	P1_SS_xxx	USB3	1#Downstream port USBSS differential transmit or receive signal line.
5/6	24/25	P1_HS_xx	USB2	1#Downstream port USB2.0 differential signal line.
26/25/28/27	2/3/4/5	P2_SS_xxx	USB3	2#Downstream port USBSS differential transmit or receive signal line.
23/24	46/1	P2_HS_xx	USB2	2#Downstream port USB2.0 differential signal line.
-	41/40/43/42	P3_SS_xxx	USB3	3#Downstream port USBSS differential transmit or receive signal line.
21/22	44/45	P3_HS_xx	USB2	3#Downstream port USB2.0 differential signal line.
-	36/35/38/37	P4_SS_xxx	USB3	4#Downstream port USBSS differential transmit or receive signal line.
19/20	33/34	P4_HS_xx	USB2	4#Downstream port USB2.0 differential signal line.
32	13	OVCUR#	I	Overall mode downstream port overcurrent detection input pin, low level overcurrent, built-in pull-up.
2	-	SMBDAT/ PWREN#	I/O	SMBus bus data signal line.
			O	Overall mode downstream port power output control pin, low on.
1	-	SMBCLK	I	SMBus clock signal line. As a configuration pin during power-on, it is used to configure the SMBDAT/PWREN# pin function of CH634F chip. If an external pull-up resistor (such as 4.7K resistor) is detected, it is configured as SMBDAT function, otherwise it is configured as PWREN# function.
31	14	RESET#	I	External reset input, built-in pull-up resistor, active low level, can be suspended when not in use, it is recommended to short-circuit VDD33 to prevent interference.
-	18	SMBDAT/SDA	I/O	Universal HUB mode: SMBus data signal line.
			I/O	PD-HUB mode: Data signal line of 2-wire serial interface, used to connect CH211 chip.
-	15	SMBCLK/SCL	I	Universal HUB mode: SMBus clock signal line.
			O	PD-HUB mode: clock signal line of 2-wire serial interface, used to connect CH211 chip.
-	12	PWREN#/CC1	O	Universal HUB mode: overall mode downstream port power output control pin, low level on. As a configuration pin during reset, it is used to configure general HUB mode or PD-HUB mode. If external pull-up resistance (such as 4.7K resistance) is detected, it is configured as general HUB mode, otherwise it is configured as PD-HUB function. *Note: In PD-HUB mode, the downstream port power*

				output control pin is provided by CH211.
			I/O (FT)	PD-HUB mode: upstream port PD protocol communication pin CC1, used to connect USB host such as mobile phone/computer.
-	11	SUSP#/CC2	I/O	Universal HUB mode: SUSP sleep state output pin, high level indicates sleep state, low level indicates normal state. If the chip configuration parameter enables the upstream port switching function, the pin switches to the upstream port and the downstream PORT1 port switching control input pin, floating or pull-up does not switch, and the input low level controls the switching.
			I/O (FT)	PD-HUB mode: External power supply PD protocol communication pin CC2, used to connect to Type-C power adapter.

Table 4-3 CH634W8G pin definitions

Pin No. (Pin with the same name can be referenced)	Pin name	Type(1)	Function description
45	VDD5	P	DCDC power input, recommended external 10uF capacitor.
46	VDD5	P	The 5V power supply input of 3.3V LDO is recommended to be externally connected with 1uF capacitor. If the voltage of VDD5 is less than 3.6V, it should be shorted to VDD33.
44	VSW	P	At the output end of DCDC, an inductor needs to be connected in series close to the pin to generate a 1.2V power supply, and the 1.2V power supply needs to be placed with a ground capacitor nearby. It is recommended to use a 2.2uH inductor and at least one 10uF capacitor.
42	VFB	P	For the voltage feedback end of DCDC, it is recommended to connect 0.1uF capacitor to ground and directly connect the DC-DC output 1.2V power supply.
47	VDD33	P	3.3V LDO output terminal, it is recommended to externally connect 1uF~10uF capacitance to ground.
64	AVDD33	P	3.3V analog power input, it is recommended to connect 0.1uF parallel 10uF or 4.7uF decoupling capacitor.
31/87	VIO33	P	I/O pin power input, external supply of 3.3V, it is recommended to externally connect 1uF or 0.1uF decoupling capacitor.

32/56	DVDD12	P	1.2V core power input, it is recommended to connect 0.1uF or 1uF decoupling capacitor externally.
43	GND_DCDC	P	DCDC ground terminal must be connected to GND.
0	GND	P	Common ground terminal, must be connected to GND.
49	GND	P	Optional ground terminal, it is recommended to connect GND.
84	UP_VDD12	P	Upstream port 1.2V power input, external 0.1uF decoupling capacitor.
69(74)/21(26)/16/6	Px_VDD12	P	1-4# downstream port has 1.2V power input, and is externally connected with 0.1uF decoupling capacitor.
66	XI	I	The input end of the crystal oscillator is connected with one end of the external 24MHz crystal and the capacitance to the ground.
65	XO	O	The invert output end of that crystal oscillator is connected with the other end of the external 24MHz crystal and the capacitance to the ground.
83/82/86/85	UP_SS_xxx	USB3	Upstream port USBSS differential transmit or receive signal line.
80/81	UP_HS_xx	USB2	Upstream port USB2.0 differential signal line.
75/76/72/73	P1_SS_xxx	USB3	1# Downstream port USBSS differential transmit or receive signal line.
68/67/71/70	P1C_SS_xxx	USB3	1# Downstream port Type-C differential transmit or receive signal line.
77/78	P1_HS_xx	USB2	1# Downstream port USB2.0 differential signal line.
20/19/23/22	P2_SS_xxx	USB3	2# Downstream port USBSS differential transmit or receive signal line.
27/28/24/25	P2C_SS_xxx	USB3	2# Downstream port Type-C differential transmit or receive signal line.
29/30	P2_HS_xx	USB2	2# Downstream port USB2.0 differential signal line.
15/14/18/17	P3_SS_xxx	USB3	3# Downstream port USBSS differential transmit or receive signal line.
12/13	P3_HS_xx	USB2	3# Downstream port USB2.0 differential signal line.
5/4/8/7	P4_SS_xxx	USB3	4# Downstream port USBSS differential transmit or receive signal line.
9/10	P4_HS_xx	USB2	4# Downstream port USB2.0 differential signal line.
40	PWREN1#	O	1# Downstream port power output control pin, low level turns on.
39	PWREN2#	O	2# Downstream port power output control pin, low level turns on.
36	PWREN3#	O	3# Downstream port power output control pin, low level turns on.
35	PWREN4#	O	4# Downstream port power output control pin, low level turns on.
41	OVCUR1#	I	1# Downstream port overcurrent detection input pin, low

			level overcurrent.
38	OVCUR2#	I	2# Downstream port overcurrent detection input pin, low level overcurrent.
37	OVCUR3#/ SMBCLK	I	3# Downstream port overcurrent detection input pin, low level overcurrent. SMBus bus clock signal line.
34	OVCUR4#/ SMBDAT	I/O	4# Downstream port overcurrent detection input pin, low level overcurrent. SMBus bus clock signal line.
63	VBUS_DET	I	USB bus VBUS status detection input, the VBUS power supply should be connected to this pin after dividing through two resistors; when this function is not used, this pin needs to be shorted to VIO33.
62	GANG_EN	I	During reset, it is used as a configuration pin to configure the overall mode or independent mode. If it is floating or high level, it is the overall mode, and if it is low level, it is the independent mode. It has a built-in pull-up resistor.
48	CHIP_EN	I	Chip operation enable control; A low level controls the chip to enter low-power consumption mode, and a high level controls the chip to enter normal working mode.
61	SPI_SCS	O	Chip select output of the SPI interface.
59	SPI_SCK	O	Clock output of the SPI interface.
58	SPI_MOSI	O	Data output of the SPI interface.
60	SPI_MISO	I	SPI interface data input, built-in pull-up resistor. If the chip configuration parameters enable the upstream port swap function, this pin will be switched to the upstream port and downstream PORT1 port swap control input pin. If it is left floating or pulled up, it will not switch. If the input is low level, it will control the switching.
57	RESET#	I	External reset input, built-in pull-up resistor, low level is valid, can be left floating when not in use, it is recommended to short-circuit VDD33 to prevent interference.
88	LED_B1	O	1# Downstream port abnormal status indication signal.
33	LED_B2	O	2# Downstream port abnormal status indication signal.
2	LED_B3/ FUN_CFG0	O	3# Downstream port abnormal status indication signal. During reset, it is used as the C port working mode configuration pin 0, and cooperates with the FUN_CFG1 pin for function configuration, refer to Table 5-3.
1	LED_B4/ FUN_CFG1	O	4# Downstream port abnormal status indication signal. During reset, it serves as port C working mode configuration pin 1 and cooperates with the FUN_CFG0

			pin for function configuration, refer to Table 5-3.
54	P1_CC1	I/O (FT)	1# Downstream port PD protocol communication pin CC1.
53	P1_CC2	I/O (FT)	1# Downstream port PD protocol communication pin CC2.
52	P2_CC1	I/O (FT)	2# Downstream port PD protocol communication pin CC1.
51	P2_CC2	I/O (FT)	2# Downstream port PD protocol communication pin CC2.
3/11/50/55/79	NC	-	Reserved, suggested suspension

Note 1: Pin type abbreviation explanation:

USB3 = USB3.0 signal pin;

USB2 = USB2.0 signal pin;

I = Signal input;

O = Signal output;

P = Power or ground;

NC = Reserved;

FT = Tolerant 5V voltage.

5. Function Description

5.1 Overcurrent Detection and Power Control

5.1.1 Overcurrent Detection

Some CH634 models support 2 overcurrent protection modes: Independent overcurrent mode and overall overcurrent mode, while some models only support overall overcurrent mode, as shown in Table 5-1.

Table 5-1 Overcurrent protection control description

Chip model	Overcurrent configuration	Overcurrent mode	Overcurrent detection sampling pin	Reference figure
CH634F	-	Overall overcurrent	OVCUR#	Figure 5-2
CH634M	-	Overall overcurrent	OVCUR#	Figure 5-2
CH634W6G	-	Overall overcurrent	OVCUR#	Figure 5-2
CH634W5M CH634W6C CH634W6T CH634W7G CH634W8G	EEPROM default configuration/ GANG_EN=High level	Independent overcurrent	OVCUR1#, OVCUR2#, OVCUR3#, OVCUR4#	Figure 5-1
	EEPROM configured as overall overcurrent /GANG_EN=Low level	Overall overcurrent	OVCUR1#	Figure 5-2
CH634W7R CH634W7S	EEPROM default configuration	Independent overcurrent	OVCUR1#, OVCUR2#, OVCUR3#, OVCUR4#	Figure 5-1
CH634W7U CH634W7V	EEPROM configured as overall overcurrent	Overall overcurrent	OVCUR1#	Figure 5-2

5.1.2 Power Control

Some CH634 models support 2 power control modes: independent power control mode and overall power control mode, while some models only support overall power control mode, as shown in Table 5-2.

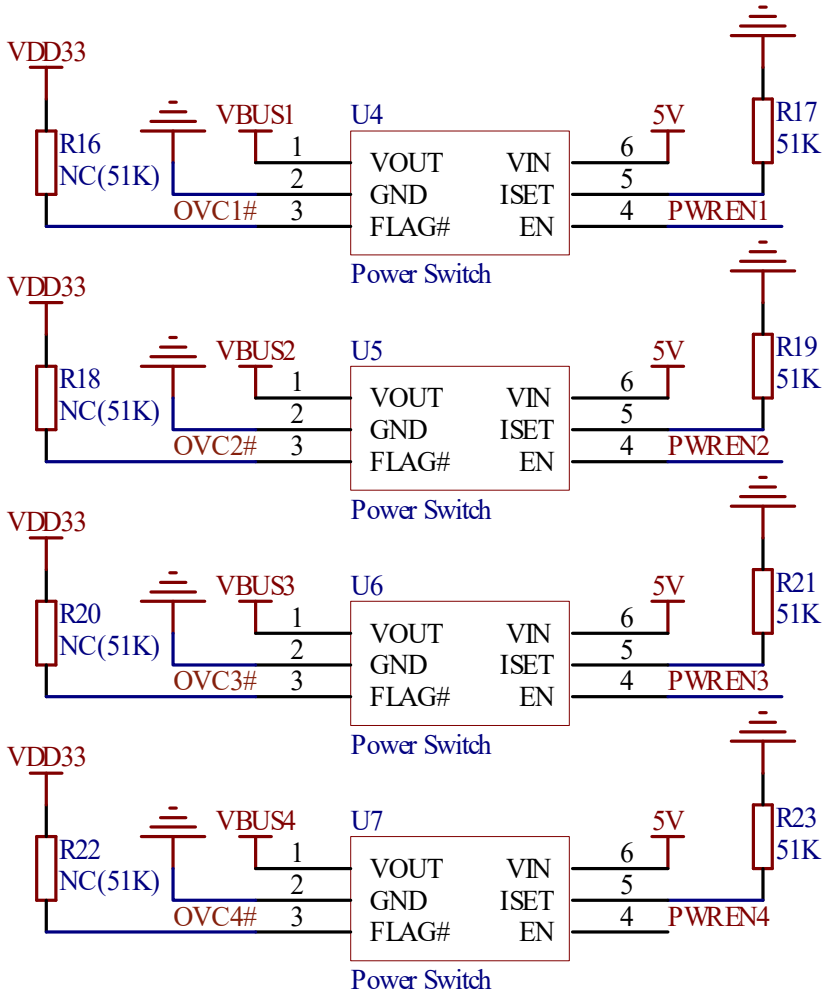
Table 5-2 Power control description

Chip model	Power control configuration	Power control	Power control pin	Reference figure
CH634F	-	Overall control	PWREN#	Figure 5-2
CH634M	-	Overall control	PWREN#	Figure 5-2
CH634W6C	-	Overall control	PWREN#	Figure 5-2
CH634W6G	-	Overall	PWREN#	Figure 5-2

		control		
CH634W5M CH634W6T CH634W7G CH634W8G	EEPROM default configuration/ GANG_EN= High level	Independent control	PWREN1#, PWREN2#, PWREN3#, PWREN4# *(Note: W5M and W6T are high level valid by default)*	Figure 5-1
	EEPROM configure as overall control /GANG_EN=Low level	Overall control	PWREN1# *(Note: W5M and W6T are high level valid by default)*	Figure 5-2
CH634W7R CH634W7S CH634W7U CH634W7V	EEPROM default configuration	Independent control	PWREN1#, PWREN2#, PWREN3#, PWREN4# *(Note: W7V defaults to high level valid)*	Figure 5-1
	EEPROM configure as overall control	Overall control	PWREN1# *(Note: W7V defaults to high level valid)*	Figure 5-2

5.1.3 Independent Overcurrent Detection and Independent Power Control

Figure 5-1 CH634 independent overcurrent detection and independent power supply control

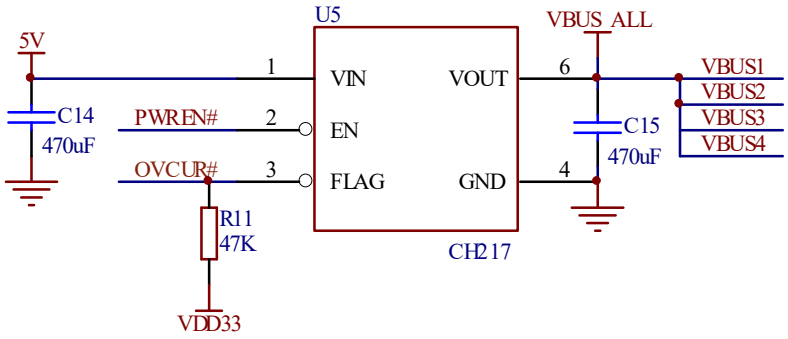


In the above figure, VBUS1-VBUS4 are connected to the VBUS power pins of downstream ports 1-4 respectively. U4~U7 are USB current-limited power distribution switch chips with integrated overcurrent detection for VBUS power distribution management. In applications where 5V is not externally powered, it is recommended to set the

current limit to less than 1A or even 500mA through an external resistor connected to ISET. The FLAG pins of U4~U7 are open-drain outputs and need to be pulled up by resistors respectively. The OVCUR# pin of the CH634 chip provides a built-in weak pull-up current, so resistors R16, R18, R20 and R22 can be omitted. The PWRENx# pin of some models of CH634 chips outputs a low level when the power is turned on, and the PWRENx# pin of some models of CH634 chips outputs a high level when the power is turned on (not applicable to the above figure), which can be configured through the PWREN_POL pin or parameterized through the EEPROM.

5.1.4 Overall Overcurrent Detection and Independent Power Control

Figure 5-2 Overall overcurrent detection and overall power control



U5 is a USB current-limited power switch chip, such as CH217 chip or similar function chip. R11 can be omitted in the default configuration. The capacity of C14 can be selected as needed. VBUS-ALL is connected to the VBUS power pins of downstream ports 1-4 at the same time. The current limit setting value of U5 needs to take into account the 4 downstream ports and whether it is self-powered.

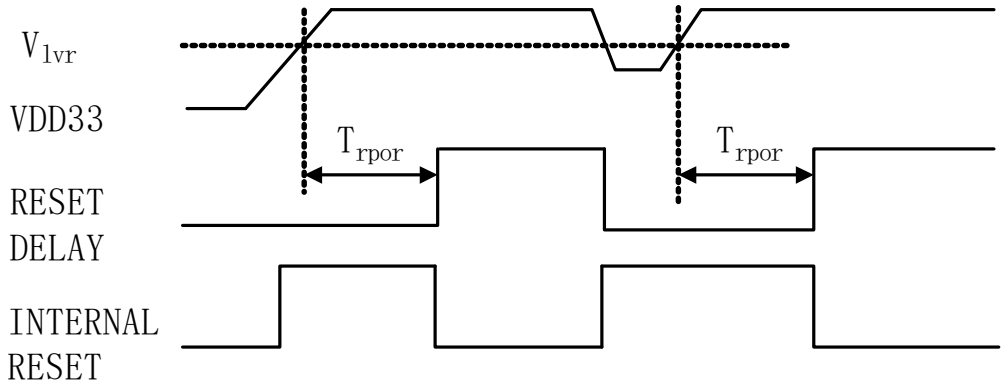
5.2 Reset

The chip has a built-in power-on reset module. Generally, no external reset signal is required. An external reset input pin RESET# is also provided, which has a built-in pull-up resistor.

5.2.1 Power-on Reset

When the power is on, the POR power-on reset module inside the chip will generate a power-on reset sequence and delay T_{rpor} by about 25mS to wait for the power to stabilize. During operation, when the power supply voltage is lower than V_{lvr}, the LVR low-voltage reset module inside the chip will generate a low-voltage reset until the voltage rises, and delay to wait for the power to stabilize. The following figure shows the power-on reset process and the low-voltage reset process.

Figure 5-3 Reset during power-on



5.2.2 External Reset

The external reset input pin RESET# has a built-in pull-up resistor. If the chip needs to be reset externally, the pin can be driven to a low level. The reset low level pulse width needs to be greater than 4uS.

5.3 Bus-powered and Self-powered

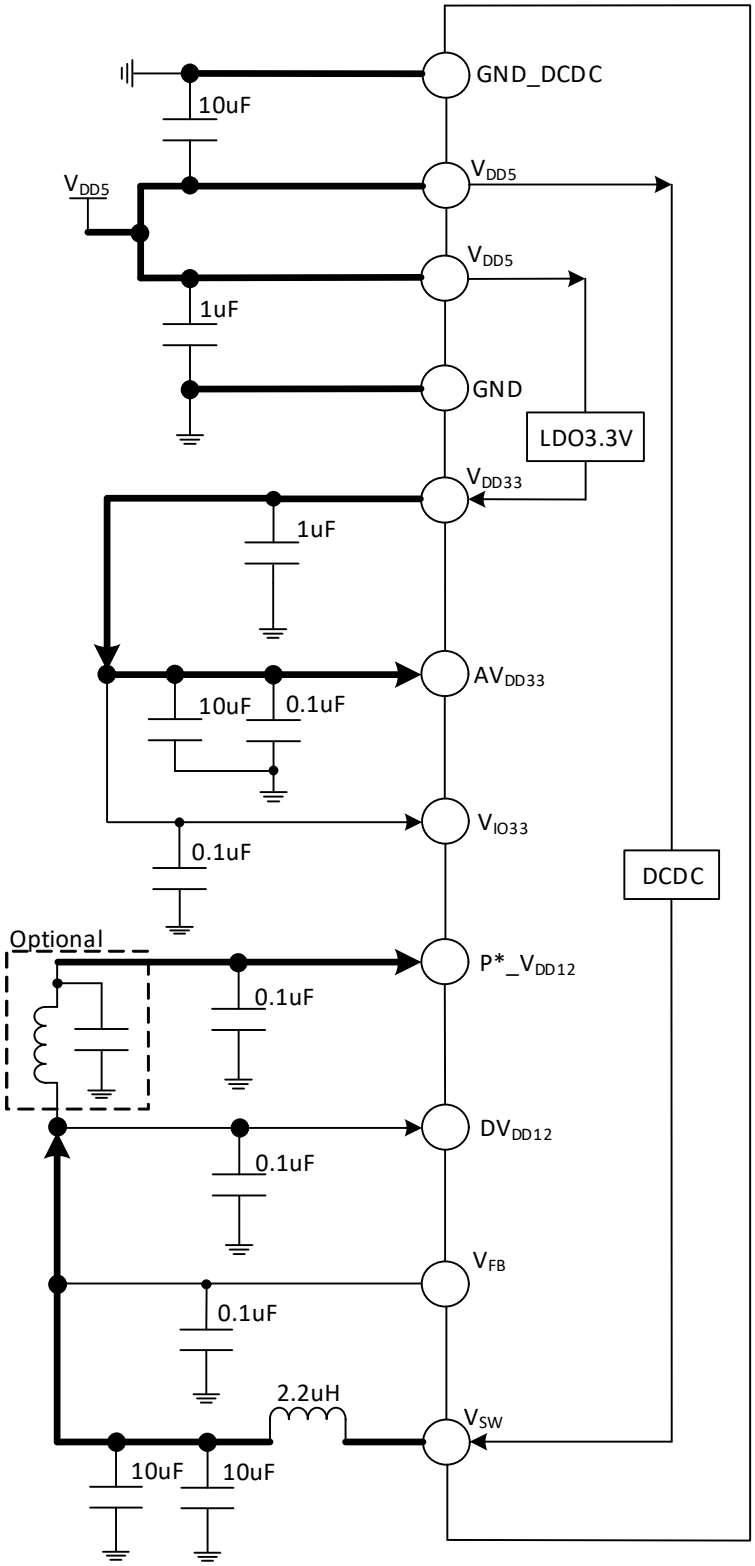
CH634 supports USB bus power supply mode and self-power supply mode. Bus power supply comes from the USB upstream port, and the power supply capacity is 500mA, 900mA, 1.5A and other standards. The internal resistance loss of the USB cable and the HUB's own consumption will reduce the power supply capacity of the downstream port, and the downstream port voltage may be low. Self-power supply usually comes from an external power port, which depends on the power supply capacity of the external power supply.

Since the voltage of the self-powered and bus-powered devices is not completely equal, the HUB needs to avoid short-circuiting the 2 devices to generate a large current. In addition, when the USB upstream port is powered off, the HUB must also prevent the self-powered external power supply from backflowing current into the USB bus and USB host.

5.3.1 Single 5V Power Supply Solution

The CH634 with VDD5 pin supports a single 5V supply scheme using the built-in LDO and DC-DC. 5V rated input from VDD5 is supplied to the LDO regulator and DC-DC buck, the LDO regulator generates 3.3V to VDD33 which is then connected to AVDD33 and VIO33, and the DC-DC buck generates 1.2V connected to VDD12 and P*_VDD12. _VDD12 and VFB, it is recommended that the 1.2V supply be LC filtered and then supplied to P*_VDD12. 3.3V supply has a cumulative capacitance of not less than 10uF to ground, 1.2V supply has a cumulative capacitance of not less than 10uF to ground, it is recommended that the dual 10uF capacitors be connected in parallel, and the ground capacitance of the 5V supply has not been less than 10uF. The 5V supply supports a wider range of voltages, which can be as low as 4V. It is recommended that the 5V power supply be coupled with a 5.5V overvoltage protection device.

Figure 5-4 Schematic diagram of single 5V power supply scheme



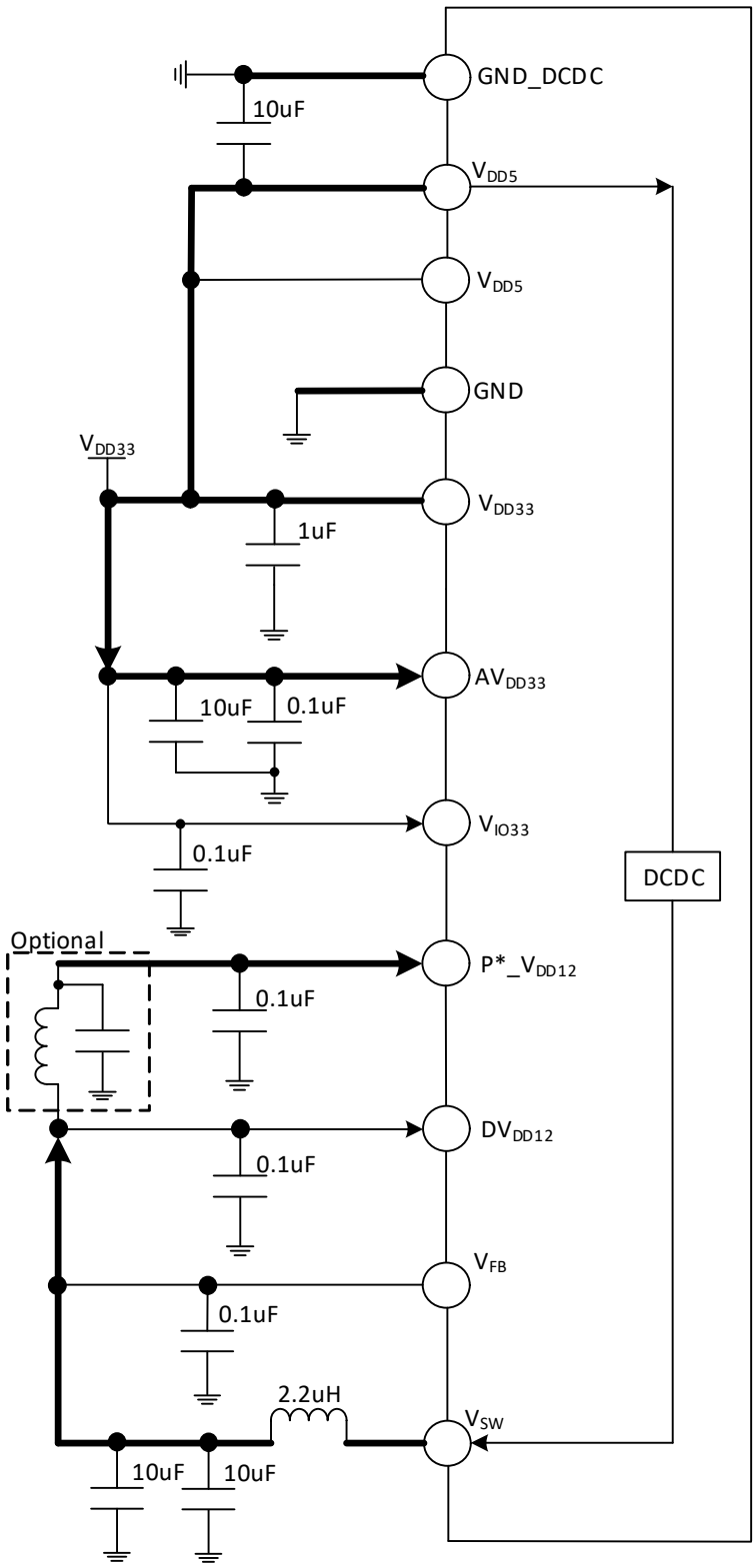
Note: The bolded line in the figure indicates a higher current, and the PCB needs to be designed to ensure sufficient line width and number of vias.

5.3.2 Single 3.3V Power Supply Solution

CH634 with VDD5 pin supports a single 3.3V power supply scheme and uses built-in DC-DC. Rated 3.3V is

connected to AVDD33, VIO33 and VDD33. At the same time, rated 3.3V is input from VDD5 and supplied to DC-DC step-down. The DC-DC step-down generates 1.2V which is connected to VDD12, P*_VDD12 and VFB. It is recommended that the 1.2V power supply be supplied to P*_VDD12 after LC filtering. The cumulative capacitance to ground of 3.3V power supply is not less than 10uF, and the cumulative capacitance to ground of 1.2V power supply is not less than 10uF. It is recommended that double 10uF capacitors be connected in parallel.

Figure 5-5 Schematic diagram of a single 3.3V power supply scheme



Note: The bolded line in the figure indicates a higher current, and the PCB needs to be designed to ensure sufficient

line width and number of vias.

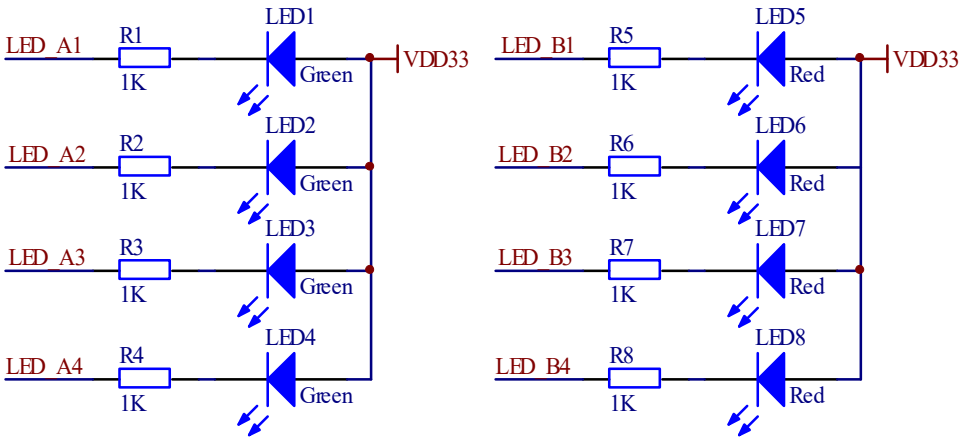
5.3.3 3.3V+1.2V Dual Power Supply Solution

CH634 without VDD5 pin only supports 3.3V+1.2V dual power supply scheme. The rated 3.3V is connected to AVDD33 and VIO33, and at the same time, the rated 1.2V is connected to VDD12 and P*_VDD12. The cumulative capacitance to ground of 3.3V power supply is not less than 10uF, and that of 1.2V power supply is not less than 10uF.

5.4 LED Indicator

Some models of CH634 chip provide a downstream port status LED indicator control pin. When the green light corresponding to the port is on, it means the port is normal. When the green light is off, it means there is no device on the port or it is suspended. When the red light corresponding to the port is on, it means the port is abnormal.
Figure 5-6 is a schematic diagram of the 8-light mode application of the CH634W7G chip, where LED1-4 are the normal status indicators (green lights) of ports 1-4 respectively. When they are on, it means that a device is plugged into the port and the port is normal. When they are off, it means that there is no device or the port is suspended. LED5-8 are the abnormal status indicators (red lights) of ports 1-4 respectively. When they are on, it means that the port is abnormal, such as overcurrent.

Figure 5-6 Schematic diagram of 8-LED mode application of CH634W7G chip



5.5 I/O Function Configuration

Some functions of the CH634 chip can be configured in 4 ways: built-in EEPROM, external EEPROM, external SPI interface FLASH and configuration pins. The parameter configuration function of the external EEPROM and external SPI interface FLASH has a higher priority than the parameter configuration function of the internal EEPROM, and the parameter configuration function of the internal EEPROM has a higher priority than the pin configuration function. Configuration pins are generally multiplexed pins, which are used as configuration pins during reset and switch to corresponding function pins after reset is completed. For specific configuration pins of different models, see the corresponding pin description list.
CH634W8G chip has three C-port working modes, which can be configured and selected through LED_B4/FUN_CFG1 and LED_B3/FUN_CFG0 pins.

Table 5-3 Configuration of C-port working mode of CH634W8G chip

C-port operation mode	LED_B4/ FUN_CFG1 level	LED_B3/ FUN_CFG0 level	Function description
Mode 0	1	1	The upstream port is a type interface, and the downstream port is 2 Type-C interfaces+2 Type-A interfaces. The Type-C interface supports forward and backward insertion and adaptation.
Mode 1	1	0	The upstream port is a Type-C interface, and the downstream port is a Type-C interface+3 Type-A interfaces. The Type-C interface supports forward and backward insertion adaptation.
Mode 2	0	1	The upstream port is a single-sided Type-C interface, and the downstream port is a Type-C interface+3 A-type interfaces, and it supports the fast charging function of Type-C/PD, which is applied to PDHUB.

5.6 Parameter Configuration Interface

Some models of CH634 provide 2-wire I2C interfaces (SCL and SDA) to communicate with external EEPROM memory chips, and the EEPROM chip address is 0. Some models of CH634 provide communication between 4-wire SPI interfaces (SCS, SCK, MOSI and MISO) and FLASH memory chips with external SPI interfaces. In EEPROM or FLASH, user-defined manufacturer ID, product ID, number of downstream ports, device non-removable characteristics of downstream ports, USB string descriptor and function configuration are stored.

Figure 5-7 Schematic diagram of external EEPROM connection

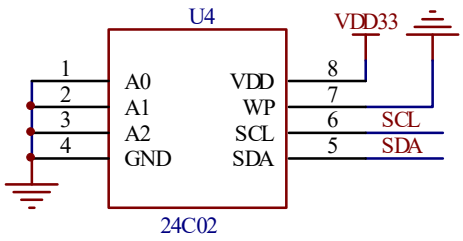
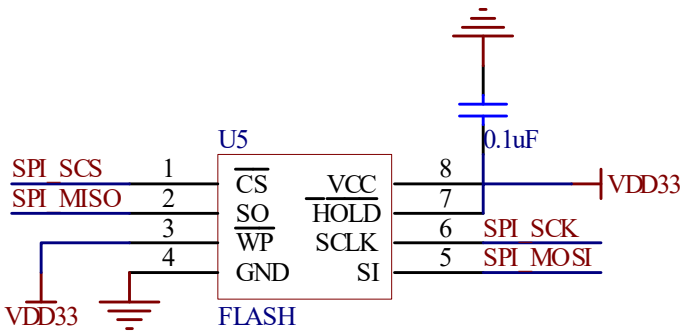


Figure 5-8 Schematic Diagram of External FLASH Connection



CH634 has built-in information memory, which can replace external EEPROM or FLASH to customize manufacturer or product information and configuration in batches according to the special needs of the industry,

such as setting the number of downstream ports and setting the equipment non-removable characteristics of downstream ports.

5.7 SMBus Configuration Interface

Some models of CH634 provide 2-wire SMBus slave interface to communicate with the external master chip. The SMBus interface contains two pins, SMCLK and SMDAT, and the communication address is 0x2C, which supports block reading and block writing operations, with a maximum of 32 bytes per block. The external master can read and write EEPROM built in the chip through SMBus interface. Figure 5-9 is the schematic diagram of block reading, and Figure 5-10 is the schematic diagram of block writing.

Figure 5-9 Block reading schematic diagram

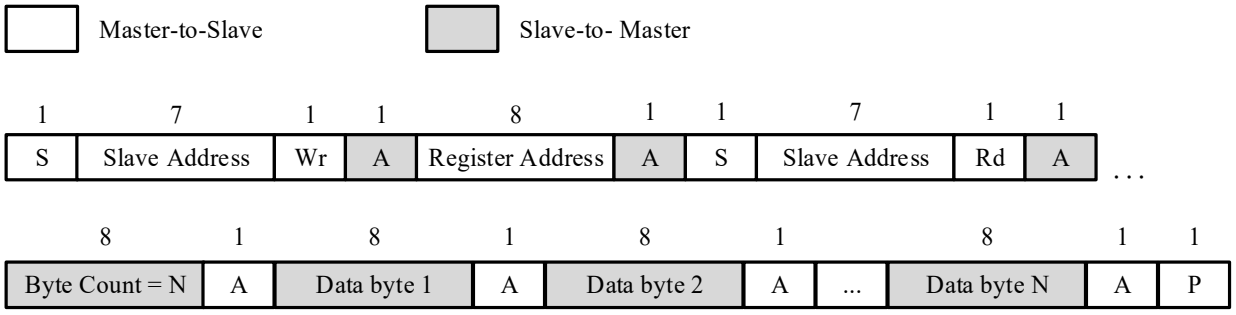
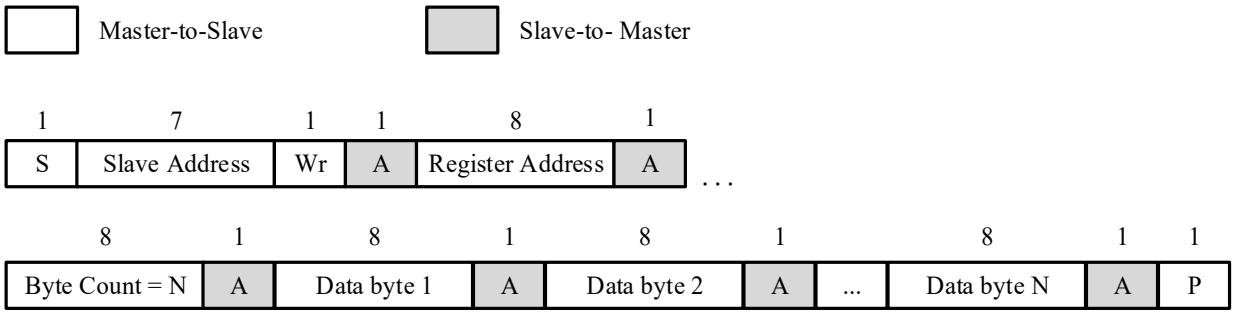


Figure 5-10 Block writing schematic diagram



5.8 EEPROM Configuration

CH634 supports loading configuration information such as manufacturer ID VID, product ID PID, USB string descriptor and function configuration from external EEPROM/FLASH or internal EEPROM. If the information in EEPROM is invalid, the default configuration information will be automatically loaded. Table 5-4 describes the specific configuration information of internal/external EEPROM/FLASH. Reserved bytes or reserved bits need to be written according to the original read value during the writing operation.

Table 5-4 Configuration information of internal/external EEPROM/FLASH

Offset address	Parameter abbreviation	Parameter description	Default value
00h	VID_L	Low byte of vendor identification VID.	86h
01h	VID_H	High byte of vendor identification VID.	1Ah
02h	PID_L	The low byte of the product identification code PID is A0h by default.	A0h

		Note: USB2.0 PID is A0h, USB3.0 PID is A1h.	
03h	PID_H	High byte of product identification code PID.	80h
04h	bcdDevice_L	bcdDevice low byte, used to indicate the chip package model; Fixed and cannot be modified.	Follow the model
05h	bcdDevice_H	bcdDevice high byte, used to indicate the chip version; Fixed and cannot be modified.	Follow the model
06h	Fun_Cfg1	Functional configuration byte 1. Bit7: Power supply mode selection; 0: Bus power supply mode (default); 1: Self-powered mode; Bit6: Reserved; Bit5: High-speed mode prohibition control; 0: High-speed mode enabled (default); 1: High-speed mode disabled; Bit4: STT and MTT mode selection; 0: STT mode; 1: MTT mode (default); Bit3: Reserved; Bit2-1: Port overcurrent function control; 00: Overall overcurrent control; 01: Independent overcurrent control; 1x: Overcurrent control is not supported; Bit0: Port power control; 0: Overall power control; 1: Independent power control.	Follow the model
07h	Fun_Cfg2	Functional configuration byte 2。 Bit7: Reserved; Bit6: Reserved; Bit5: Reserved; Bit4: Reserved; Bit3: Whether HUB is Compound Device; 0: No; 1: Yes. Bit2-0: Reserved.	20h
08h	Fun_Cfg3	Functional configuration byte 3。 Bit7-4: Reserved; Bit3: Port remapping function control; 0: Disable (default); 1: Enable. Bit2-1: Reserved; Bit0: String descriptor enable control; 0: Disable (default);	00h

		1: Enable.	
09h	Dev_ Removable	Whether the downstream port device can remove the control.。 Bit7-5: Reserved; Bit4-1: Whether the downstream port 4-1 device can be removed; 0: Removable (default); 1: Non-removable; Bit0: Reserved, must be 0.	Follow the model
0Ah	Port_Dis_Sp	Port prohibition in self-powered mode. Bit7-5: Reserved; Bit4-1: Whether downstream port 4-1 is prohibited; 0: Enable (Default) 1: Disable; Bit0: Reserved, must be 0.	00h
0Bh	Port_Dis_Bp	Port prohibition in bus power supply mode. Bit7-5: Reserved; Bit4-1: Whether downstream port 4-1 is prohibited; 0: Enable (Default) 1: Disable; Bit0: Reserved, must be 0.	00h
0Ch	MaxPwr_Sp	Maximum working current in self-powered mode, in 2mA.	01h
0Dh	MaxPwr_Bp	Maximum working current in bus power supply mode, in 2mA.	32h
0Eh	HubCurrent_Sp	Maximum current required by HUB in self-powered mode.	01h
0Fh	HubCurrent_Bp	Maximum current required by HUB in bus power supply mode.	32h
10h	Pwr_OnTime	Delay time from power-on of downstream port to effective power supply.	32h
11h	LanguageID_H	Language ID high byte.	00h
12h	LanguageID_L	Language ID low byte.	00h
13h	Vendor_StrLen	Manufacturer string descriptor length.	00h
14h	Product_StrLen	Product string descriptor length.	00h
15h	SN_StrLen	Length of serial number string descriptor.	00h
16h-53h	Vendor String	Vendor string descriptor; Vendor string descriptor in Unicode code format.	00h
54h-91h	Product String	Product string descriptor; Product string descriptor in Unicode code format.	00h
92h-CFh	Serial Number String	Serial number string descriptor; Serial number string descriptor in Unicode code	00h

		format.	
D0h	PortNum	Number of downstream ports, valid range: 1-4.	Follow the model
D1h	bcdUSB_L	USB version low byte. bcdUSB_L=0x00，USB2.00； bcdUSB_L=0x01，USB2.01； bcdUSB_L=0x10，USB2.10。	10h
D2h	Fun_Cfg4	Functional configuration byte 4. Bit7-2: Reserved, when writing, you need to write the original read value; Bit1: Forcing the downstream port to be in full speed mode; 0: High-speed mode (default); 1: Full-speed mode; Bit0: LED function enables configuration; 0: Disable (default); 1: Enable.	00h
D3h	Fun_Cfg5	Functional configuration byte 5. Bit7: Polarity configuration of LED indicator; 0: Active low (default); 1: Active high; Bit6: Polarity configuration of port overcurrent detection; 0: Active low (default); 1: Active high; Bit5: Port power control polarity configuration; 0: Active low (Some models default); 1: Active high (Some models default); Bit4: Port BC charge configuration; 0: Disable (default); 1: Enable. Bit3: Whether LPM configuration is enabled; 0: Disable; 1: Enable (default); Bit2: Whether the upstream switching function is enabled; 0: Disable (default); 1: Enable. Bit1-0: Reserved;	Follow the model
D4-E3h	BOS_UUID	UUID field in BOS descriptor, accounting for 16 bytes.	00h
E4-FEh	Reserved	Reserved	00h
FFh	Switch_Ctl	The upstream port exchange function control byte; This byte defaults to 00h. Writing COh controls	00h

		switching, writing 8Oh cancels switching, and writing other values is invalid.	

6. Parameters

6.1 Absolute Maximum

(Critical or exceeding the absolute maximum value may cause the chip to operate improperly or even be damaged.)

Name	Parameter description	Min.	Max.	Unit
T_A	Ambient temperature at work	-40	85	℃
T_J	Junction temperature range	-40	100	℃
T_S	Ambient temperature during storage	-55	150	℃
V_{DD5}	Input supply voltage of LDO voltage regulator and DC-DC buck (V_{DD5})	-0.4	5.5	V
*V_{DD33}	Operating power supply voltage (V_{DD33}/AV_{DD33})	-0.4	4.0	V
V_{IO33}	I/O supply voltage (V_{IO33})	-0.4	4.0	V
*V_{DD12}	USB module power supply voltage (P*_VDD12)/ core power supply voltage (DVDD12)	-0.4	1.5	V
V_{FB}	DCDC voltage feedback terminal	-0.4	1.5	V
V_{USB2}	Voltage on USB2.0 physical signal pin	-0.4	V_{DD33}+0.4	V
V_{USB3}	Voltage on USB3.0 physical signal pin	-0.4	V_{DD12}+0.4	V
V_{IN}	Input voltage on FT (tolerant 5V) pin.	-0.4	5.5	V
	Input voltage on other pins	-0.4	V_{IO33}+0.4	V
$V_{ESD(HBM)}$	ESD electrostatic discharge voltage (HBM) of common I/O pin.	4K		V

6.2 Electrical Parameters (Test condition: T_A = 25℃, *V_{DD33} = V_{IO33} = 3.3V， *V_{DD12} = 1.2V)

Name	Parameter description		Min.	Typ.	Max.	Unit
V_{DD5}	Input power supply voltage of LDO regulator and DCDC buck		4.0	5.0	5.25	V
*V_{DD33}	Operating power supply voltage of single 3.3V power supply scheme or chip package without VDD5 pin.		3.2	3.3	3.4	V
	Operating voltage under single 5V power supply scheme (LDO regulator output)		3.2	3.3	3.4	V
*V_{DD12}	USB module power supply voltage (P*_V_{DD12})/ core power supply voltage (DV_{DD12})		1.18	1.2	1.3	V
V_{IO33}	I/O pin supply voltage		3.0	3.3	3.6	V
I_{SLP}	Deep sleep power supply current (excluding 1.5KΩ pull-up)			1.7		mA
V_{IL}	Low level input voltage	Standard I/O pin	0		0.8	V
		FT I/O pin	0		0.8	V
V_{IH}	High level input voltage	Standard I/O pin	2.0		V_{IO33}	V
		FT I/O pin	2.0		5.0	V

V_{OL}	Low level output voltage	Sink current 5mA		0.4	0.6	V
V_{OH}	High level output voltage	Source current 5mA	V_{IO33}-0.6	V_{IO33}-0.4		V
R_{PU}	Pull-up equivalent resistance			70		KΩ
R_{PD}	Pull-down equivalent resistance			70		KΩ

6.3 Typical Working Current (Test condition: CH634W8G, T_A = 25℃)

Number of downstream connection devices		Single 5V power supply scheme	3.3V+1.2V dual power supply scheme		Unit
		5V power supply	3.3V power supply	1.2V power supply	
USB3.0	Sleep mode	0.35	0.16	1.3	mA
	Suspension	1.9	2.4	1.2	mA
	1	88.1	19.6	234	mA
	2	114	19.6	308	mA
	3	141	19.6	380	mA
	4	170	19.6	450	mA
USB2.0	Sleep mode	0.35	0.16	1.3	mA
	Suspension	1.9	2.4	1.2	mA
	1	46	41	17	mA
	2	59	55	17.1	mA
	3	73	71	17.3	mA
	4	97	84	17.5	mA

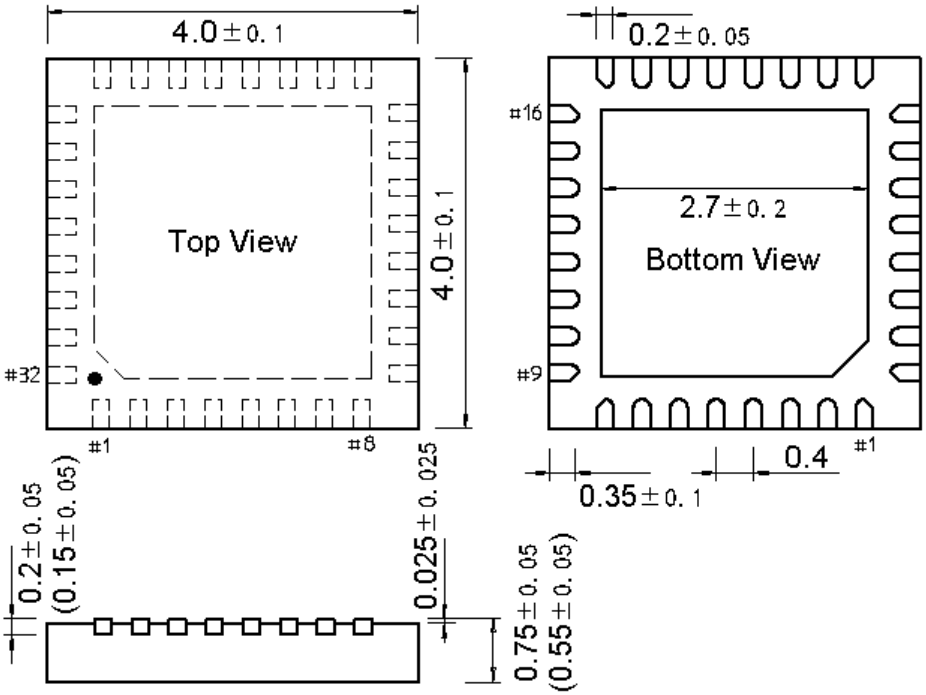
Note: A single 5V power supply scheme only consumes current from 5V; While the 3.3V+1.2V dual power supply scheme consumes current from 3.3V and 1.2V respectively.

7. Package Information

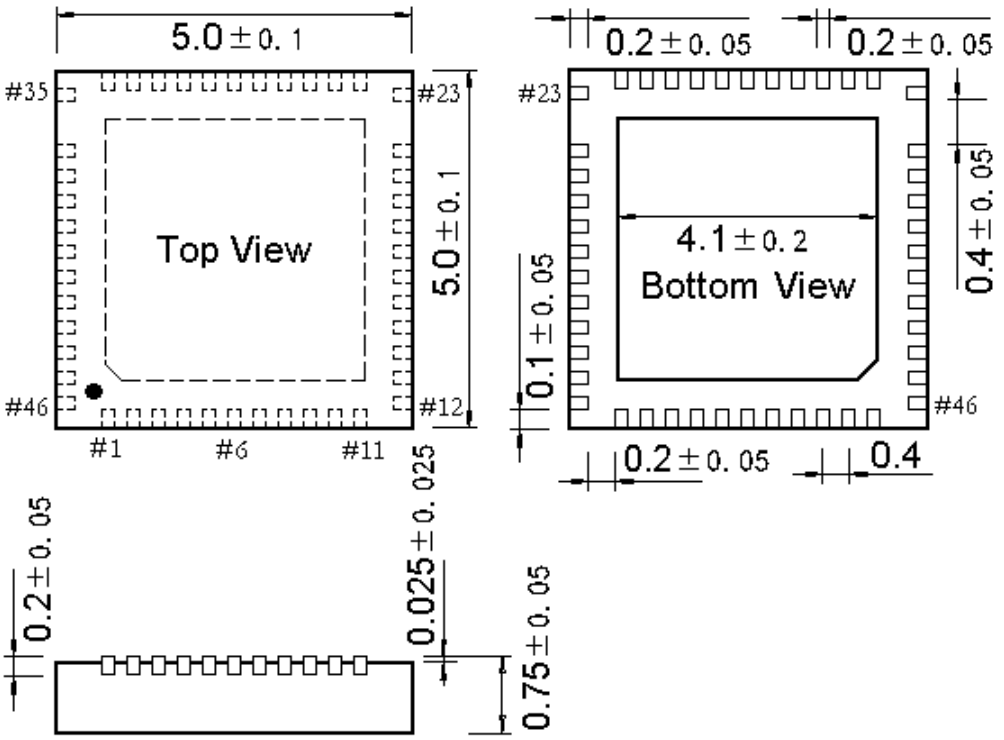
Note: All dimensions are in millimeters.

The pin center spacing values are nominal, without error. And the error of dimensions other than the pin center spacing values is not more than ±0.2mm.

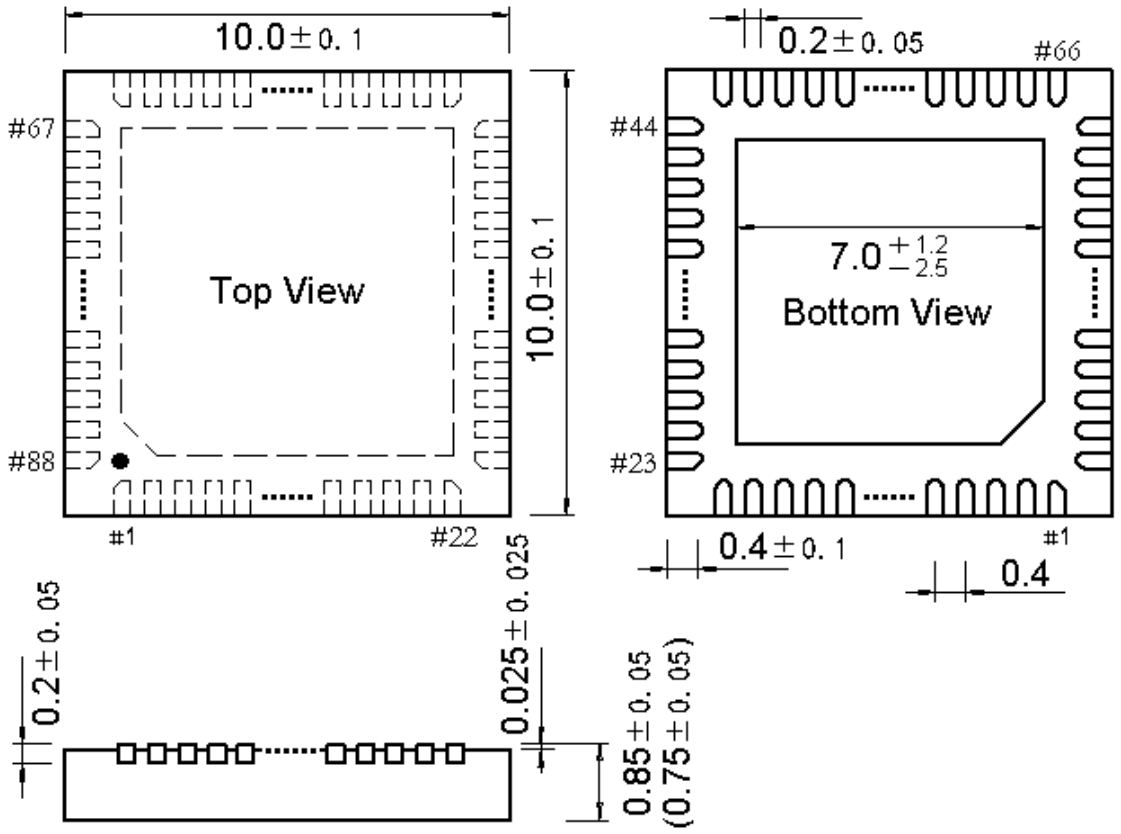
7.1 QFN32



7.2 QFN46C5



7.3 QFN88



8. Applications

8.1 CH634W8G Chip Reference Circuit Diagram

Figure 8-1 below shows the reference circuit diagram of CH634W8G chip working in mode 0. P1-P4 are the four downstream USB ports of the HUB, among which P1 and P2 are Type-C interfaces, which are compatible with USB-C cables and connection specifications, and native support for Type-C forward and backward insertion adaptation; P3 and P4 are Type-A interfaces, P5 is the upstream USB port of the HUB, and P6 is the external power supply Type-C interface.

U3 is an ideal diode CH213 with low voltage drop, which has simple over-current and short-circuit protection functions and faster protection response, and can replace Fuse. It is mainly used to avoid backflow of external power supply of P6 to VDD5 of upstream port P5, especially when the upstream port, such as computer, is turned off and the external power supply of P6 is still available. Theoretically, U3 can be replaced by Schottky diode, but it is necessary to choose a device with low voltage drop, otherwise it will reduce the output voltage of the downstream port VBUS. At a load current of 300mA, the voltage drop of Schottky diode is about 0.3V, and the voltage drop of ideal diode is about 0.05V. Because P6 itself and external power supply usually have no load, the backward flow from P5 to P6 is generally not considered.

CH634W8G chip works in independent power distribution control and independent overcurrent detection mode by default, and can be configured into overall power distribution control and overall overcurrent detection through GANG_EN pin. U4-U7 is a USB distribution switch chip CH217 that supports overcurrent protection. In the figure, R17, R19, R22 and R25 set current limiting thresholds according to the power supply capacity, and the FLAG# pin of the USB current-limiting power switch chip can generate over-current or over-temperature alarm signals to inform the HUB controller and computer, and the OVCUR# pin of CH634W8G has built-in pull-up resistors.

P1 and P2 ports of CH634W8G chip can also be used as type-A interfaces. If the USB3.0 signal line uses PxC_SS_RXA, PxC_SS_RXB, PxC_SS_TXA and PxC_SS_TXB, the Px_CC2 pin needs to be grounded through a 5.1K resistor; If the USB3.0 signal line uses Px_SS_RXA, Px_SS_RXB, Px_SS_TXA and Px_SS_TXB, the Px_CC1 pin needs to be grounded through a 5.1K resistor.

When designing PCB, the actual working current carrying capacity should be considered. The PCB of GND routing paths of VDD5, VBUS_OUT*, 5V and P6 of each port should be as wide as possible. If there are vias, it is recommended to connect them in parallel.

At the instant when the USB device in the downstream port is hot-plugged, the dynamic load may cause the voltage of VBUS and 5V to drop instantly, which may lead to the low-voltage reset of LVR, thus causing the phenomenon that the whole HUB is disconnected and reconnected. Improvement methods: ① Increase the electrolytic capacitance of 5V power supply (increase C14 capacity as shown in the figure) within the scope permitted by the specification to alleviate the drop; ② Increase the capacitance of the power input terminal of the HUB chip (increase the capacity of C37 as shown in the figure, for example, 22uf); ③ Enhance the 5V power supply capacity or change to self-power supply. In addition, improving the quality of USB wire will also improve the power supply capacity.

It is recommended to add 5V overvoltage protection devices, and all USB signals should be added with ESD protection devices, such as CH412K, whose VCC should be connected to 3.3V.

Figure 8-1 CH634W8G Chip reference circuit diagram