USB PD Fast Charging Protocol Chip CH233

Datasheet

Version: 1A

https://wch-ic.com

1. Overview

CH233A/CH233K is a Type-C single port fast charging protocol chip in SOT23-6 package, which supports PD3.0/2.0 and PPS fast charging protocols from 3.3V~21V. It supports various types of voltage references such as TL431 or FB filling current regulation for DC-DC system.

CH233P comes with I2C slave function and hardware configurable 6 communication addresses on the base function of CH233A, which can use MCU to configure the protocol power and read the working status parameters of multiple CH233P through I2C to realize flexible power allocation control.

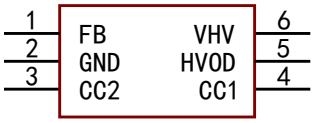
2. Features

- Support 3.3V-22V wide voltage input
- Support PD2.0/3.0 and PPS fast charging protocols.
- Support FB irrigation current regulation of TL431 and DC-DC devices with 20mV regulation accuracy.

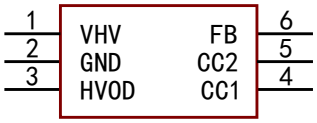
3. Applications

- AC Power Adapter
- Car Charger
- UPS
- Mobile Power

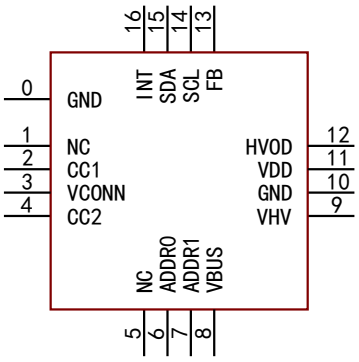
4. Package



CH233A (SOT23-6)



CH233K (SOT23-6)



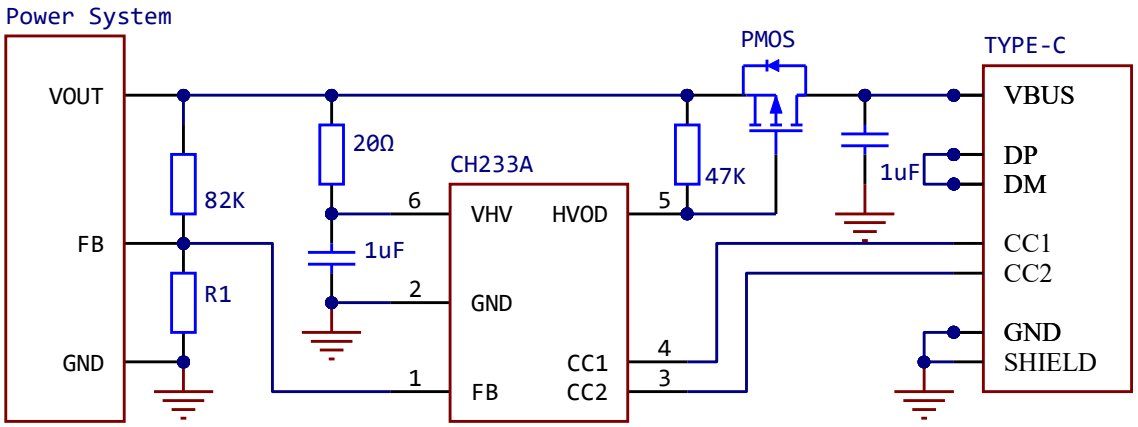
CH233P（QFN16）

5. Pins

Pin No.			Pin Name	Pin Description
CH233K	CH233A	CH233P		
1	6	9	VHV	The chip internal LDO input pin, series resistor to the high voltage power supply, and connect 1uF decoupling capacitor
2	2	0/10	GND	Common ground
6	1	13	FB	Adjustable sink current input for voltage feedback adjustment
3	5	12	HVOD	Power supply path PMOS control pin, need to be pulled up externally
4	4	2	CC1	Type-C PD fast charging protocol communication bus
5	3	4	CC2	
-	-	6/7	ADDR0/ADDR1	2-wire I2C slave address setting bit
-	-	14/15/16	SCL/SDA/INT	Clock pin, data pin and interrupt pin of 2-wire I2C slave
-	-	3	VCONN	Auxiliary power supply end, used for supplying power to type-C PD Cable Marker.
-	-	11	VDD	Internal power regulator LDO output and internal working power supply input, external capacity 1uF decoupling capacitor.
-	-	8	VBUS	VBUS discharge port, supporting high voltage
-	-	1/5	NC	Pin not defined, need to float.

6. Typical Application

CH233A Reference circuit



7. Function Description

7.1 VHV Pin

The VHV pin of CH233A/CH233K/CH233P is internally integrated with LDO. When in use, it needs to connect the series resistor to the power supply and connect the 1uF decoupling capacitor to GND. The connected series resistance is recommended to be 20R.

7.2 FB Pin

The FB pin of CH233A/CH233K/CH233P has controllable pouring current, and the output voltage of power supply system can be controlled by matching with voltage reference such as TL431 or FB pin of DC-DC system. When in use, the upper bias resistance on FB pin should be fixed at 82K, and the lower bias resistance should be calculated according to FB voltage, so that the default output voltage of power supply system is 3.3V. 1% or higher accuracy should be used for the upper and lower bias resistors of FB pin.

For CH233A/CH233K/CH233P, an example of calculation of R1 resistance value in a typical application:

For TL431 with FB voltage of 2.5V, the upper bias is 82K and the lower bias resistor R1 is taken as 255K, the default output voltage is:

$$((82/255)+1) * 2.5 \approx 3.3V$$

For a DC-DC system with an FB voltage of 0.8V, the upper bias is 82K and the lower bias resistor R1 is taken to be 26.1K, and the default output voltage is:

$$((82/26.1)+1) * 0.8 \approx 3.3V$$

7.3 HVOD Pin

HVOD is an open-drain output pin, which is used to drive the power path PMOS and control the VHV power output. HVOD pin has no internal pull-up resistor and needs to be added externally.

When there is no equipment in the Type-C interface, the HVOD pin is high impedance state to control PMOS to turn off;

When there is equipment in the Type-C interface, the HVOD pin outputs a low level to control PMOS conduction;

If you want not to use the power channel PMOS, you can directly suspend the HVOD pin.

7.4 CC1/CC2 Pin

The CC1/CC2 pin is used for equipment access detection and PD protocol handshake. CH233A/CH233K/CH233P supports the current broadcast of 500mA, 1.5A or 3A in DFP mode defined by Type-C protocol, and the default is 3A current broadcast.

7.5 SCL/SDA 2-wire Interface and INT Interrupt Pin

CH233P has an I2C slave interface, which can be configured by ADDR0/ADDR1 to select the address (even and odd address), and can be used for PDO configuration modification, related flag bit reading and voltage reading.

INT is high by default, and when the device inserts or removes INT, it will generate an interrupt.

ADDR1	ADDR0	Remarks	7-bit address (Even-even double address)
1	1	$V_{ADDR1}<V_{ADDR0}$	0b0101110 or 0b0101111
1	1	$V_{ADDR1}>V_{ADDR0}$	0b0100110 or 0b0100111
1	0		0b0100100 or 0b0100101
0	1		0b0100010 or 0b0100011
0	0	$V_{ADDR1}<V_{ADDR0}$	0b0101000 or 0b0101001
0	0	$V_{ADDR1}>V_{ADDR0}$	0b0100000 or 0b0100001

Register address, name and function description:

Address	Name	Function	R/W
0x8F	PDO select register	Use to select PDO	RW
0x8D	Flag status register	Used to read the flag bit	RO
0x09	FB data register	Used to read voltage data.	RO

The following is a detailed introduction:

0x8F PDO select register
Write corresponding numerical value to modify PDO
0:10W 1:20W 2:25W 3:30W 4:35W 5:45W 6:65W 7:100W
When configured to 100W, if the cable has no eMarker function when the device is connected, the PDO will be reduced to 65W, and the register will be modified at the same time.

0x8D flag status register:

Bit	7	6	5~3	2~0
Name	PD connection flag bit	eMarker flag bit	Reserved	Current NDO selection
Default value	0	0	XXX	000

[0~2]: Current device NDO selection gears
[6] eMarker flag bit: this flag bit is 1 when the cable is an eMarker cable, and 0 in other cases.
[7] PD connection flag bit: 1 for successful PD connection, 0 for no PD or disconnection.
[3~5]: Reserved

0x09 FB data register.
This bit saves the current FB data, range 0~255, FB is converted to output voltage conversion formula
V_{out} = FB * 0.08 + 3.3
For example, if the FB value is 0x17, the converted voltage is 5.14V.

7.6 VCONN and VDD Pin

VCONN is usually connected directly to the VDD pin and is used to supply power to the type-C PD Cable Marker.

8. Function Description

8.1 Absolute Maximum Value (Critical or exceeding the absolute maximum value will probably cause the chip to work improperly or even be damaged)

Symbol	Parameter	Min.	Max.	Unit
TA	Ambient temperature during operation	-40	105	℃
TS	Ambient temperature during storage	-55	125	℃
VHV	Operating power supply voltage (The VHV pin is connected to the power supply, and the GND pin is grounded)	-0.5	25.0	V
VDD	Operating power supply voltage (The VDD pin is connected to the power supply, and the GND pin is grounded)	-0.5	6.0	V
VIOCC	Voltage on non-high voltage pins CC1, CC2	-0.5	25.0	V
VIOUX	Voltage on non-high voltage pin FB	-0.5	6.5	V
VIOHV	Voltage at the high voltage pin HVOD	-0.5	27.0	V
PD	Maximum power consumption of the entire chip (VHV voltage * current + VHV discharge power consumption)		300	mW

8.2 Electrical Parameters (Test condition: TA = 25℃)

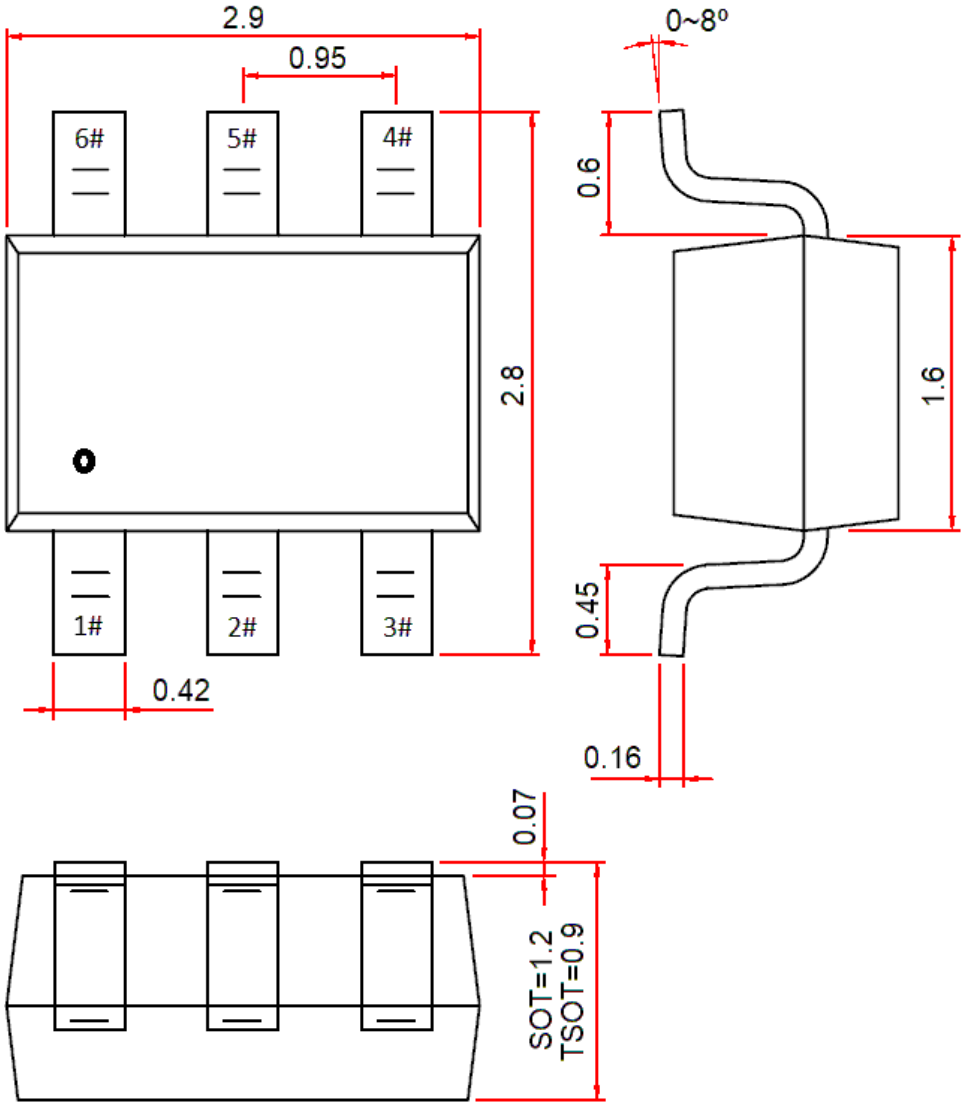
Symbol	Parameter		Min.	Typ.	Max.	Unit
VHV	High voltage supply voltage VHV		0	3~20	22	V
VDD	Power supply voltage VDD		2.7	3.3	3.7	V
VILIIC	I2C active low voltage		0		0.8	V
VIHIIC	I2C active high voltage		2		VDD	V
ICC	Power current during operation	VHV=20V		1.9	12	mA
		VHV=5V		1.7	8	
IFB	Sink current on FB pin			1~255		uA
VR	Power-on reset voltage threshold		2.35	2.4	2.7	V

9. Package Information

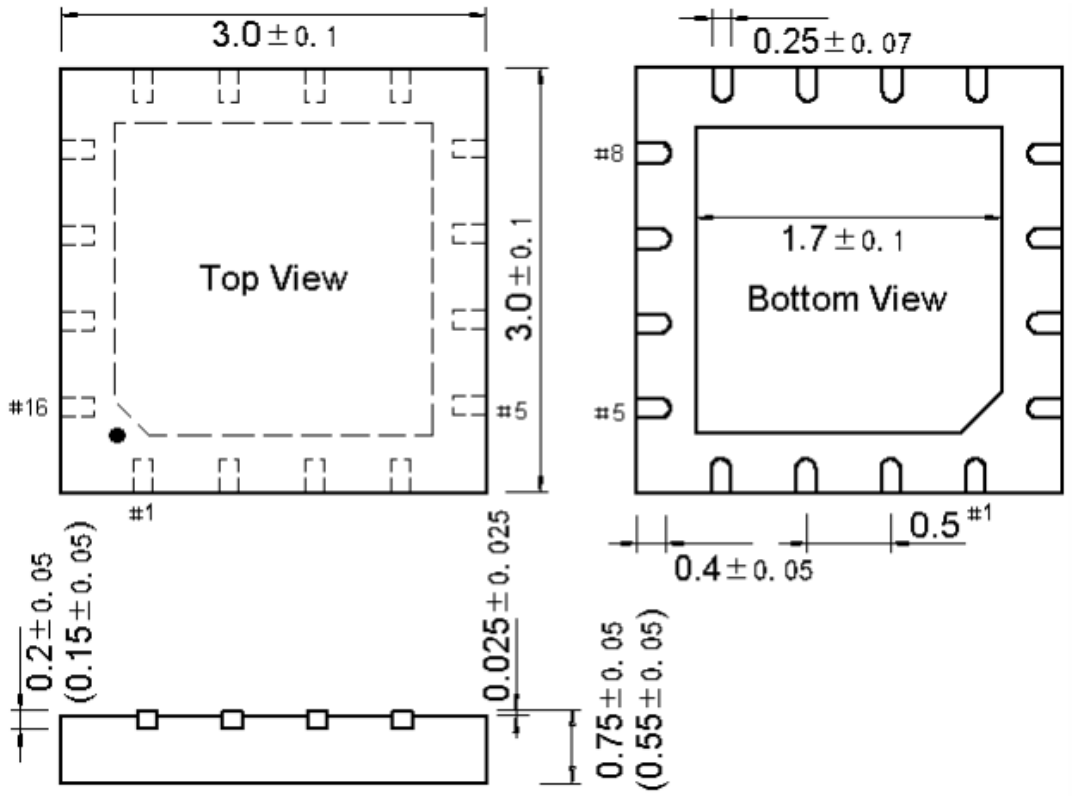
Package Form	Body Size	Pin Pitch		Order Model
SOT23-6	1.6mm	0.95mm	37mil	CH233A
SOT23-6	1.6mm	0.95mm	37mil	CH233K
QFN16	3*3mm	0.50mm	19.7mil	CH233P

Note: The dimensioning unit is mm.

9.1 SOT23-6



9.2 QFN16


3.0±0.1
Top View
3.0±0.1
#16
#5
#1
0.2±0.05
(0.15±0.05)
0.025±0.025
0.75±0.05
(0.55±0.05)
0.25±0.07
#8
1.7±0.1
Bottom View
#5
0.5
#1
0.4±0.05